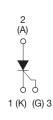
# VS-12TTS08PbF, VS-12TTS08-M3

Vishay Semiconductors

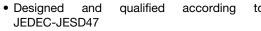
# **High Voltage Phase Control Thyristor, 12 A**

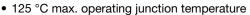


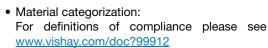


PRODUCT SUMMARY				
Package	TO-220AB			
Diode variation	Single SCR			
I <sub>T(AV)</sub>	8 A			
V <sub>DRM</sub> /V <sub>RRM</sub>	800 V			
$V_{TM}$	1.2 V			
I <sub>GT</sub>	15 mA			
T <sub>J</sub>	- 40 °C to 125 °C			

#### **FEATURES**











# ROHS COMPLIANT HALOGEN FREE Available

#### **APPLICATIONS**

 Typical usage is in input rectification crowbar (soft start) and AC switch in motor control, UPS, welding, and battery charge.

#### **DESCRIPTION**

The VS-12TTS08... high voltage series of silicon controlled rectifiers are specifically designed for medium power switching and phase control applications. The glass passivation technology used has reliable operation up to 125 °C junction temperature.

OUTPUT CURRENT IN TYPICAL APPLICATIONS						
APPLICATIONS SINGLE-PHASE BRIDGE THREE-PHASE BRIDGE UNITS						
Capacitive input filter $T_A = 55$ °C, $T_J = 125$ °C, common heatsink of 1 °C/W 13.5						

MAJOR RATINGS AND CHARACTERISTICS					
PARAMETER	TEST CONDITIONS	UNITS			
I <sub>T(AV)</sub>	Sinusoidal waveform	Sinusoidal waveform 8			
I <sub>T(RMS)</sub>		12.5	А		
V <sub>DRM</sub> /V <sub>RRM</sub>		800	V		
I <sub>TSM</sub>		110	Α		
V <sub>T</sub>	8 A, T <sub>J</sub> = 25 °C	1.2	V		
dV/dt		150	V/μs		
dl/dt		100	A/μs		
T <sub>J</sub>	Range	- 40 to 125	°C		

VOLTAGE RATINGS							
PART NUMBER	V <sub>RRM</sub> , MAXIMUM PEAK VOLTAGE V	V <sub>DRM</sub> , MAXIMUM PEAK DIRECT VOLTAGE V	I <sub>RRM</sub> /I <sub>DRM</sub> AT 125 °C mA				
VS-12TTS08PbF, VS-12TTS08-M3	800	800	1.0				



# VS-12TTS08PbF, VS-12TTS08-M3

# Vishay Semiconductors

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average on-state current	I <sub>T(AV)</sub>	T 100 °C 100° conduction half sine ways	8	
Maximum RMS on-state current	I <sub>T(RMS)</sub>	T <sub>C</sub> = 108 °C, 180° conduction, half sine wave	12.5	^
Maximum peak, one-cycle,	,	10 ms sine pulse, rated V <sub>RRM</sub> applied, T <sub>J</sub> = 125 °C	95	Α
non-repetitive surge current	I <sub>TSM</sub>	10 ms sine pulse, no voltage reapplied, T <sub>J</sub> = 125 °C	110	
Maximum 12t for fucing	l <sup>2</sup> t	10 ms sine pulse, rated V <sub>RRM</sub> applied, T <sub>J</sub> = 125 °C	45	A <sup>2</sup> s
Maximum I <sup>2</sup> t for fusing	I <sup>2</sup> t	10 ms sine pulse, no voltage reapplied, T <sub>J</sub> = 125 °C	64	A-S
Maximum I <sup>2</sup> √t for fusing	I <sup>2</sup> √t	$t = 0.1$ ms to 10 ms, no voltage reapplied, $T_J = 125$ °C	640	A²√s
Maximum on-state voltage drop	V <sub>TM</sub>	8 A, T <sub>J</sub> = 25 °C	1.2	V
On-state slope resistance	r <sub>t</sub>	T 105 °C	16.2	mΩ
Threshold voltage	V <sub>T(TO)</sub>	T <sub>J</sub> = 125 °C	0.87	V
Maximum reverse and direct leakage	1 /1	T <sub>J</sub> = 25 °C	0.05	
current	I <sub>RM</sub> /I <sub>DM</sub>	$V_R = \text{Rated } V_{RRM}/V_{DRM}$	1.0	
Typical holding current	I <sub>H</sub>	Anode supply = 6 V, resistive load, initial $I_T$ = 1 A, $T_J$ = 25 °C	30	mA
Maximum latching current	ΙL	Anode supply = 6 V, resistive load, T <sub>J</sub> = 25 °C	50	
Maximum rate of rise of off-state voltage	dV/dt	$T_J = T_J \text{ max., linear to } 80 ^{\circ}\text{C, } V_{DRM} = R_g ^{-}\text{k} = \text{Open}$	150	V/µs
Maximum rate of rise of turned-on current	dl/dt		100	A/µs

TRIGGERING							
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS			
Maximum peak gate power	$P_{GM}$		8.0	W			
Maximum average gate power	P <sub>G(AV)</sub>		2.0	VV			
Maximum peak positive gate current	+ I <sub>GM</sub>		1.5	Α			
Maximum peak negative gate voltage	- V <sub>GM</sub>		10	V			
		Anode supply = 6 V, resistive load, T <sub>J</sub> = - 65 °C	20	mA			
Maximum required DC gate current to trigger	$I_{GT}$	Anode supply = 6 V, resistive load, T <sub>J</sub> = 25 °C	15				
119901		Anode supply = 6 V, resistive load, T <sub>J</sub> = 125 °C	10				
		Anode supply = 6 V, resistive load, T <sub>J</sub> = - 65 °C	1.2				
Maximum required DC gate voltage to trigger	$V_{GT}$	Anode supply = 6 V, resistive load, T <sub>J</sub> = 25 °C	1	.,			
voltage to trigger		Anode supply = 6 V, resistive load, T <sub>J</sub> = 125 °C	0.7	V			
Maximum DC gate voltage not to trigger	$V_{GD}$	T 105 °C V Poted value	0.2				
Maximum DC gate current not to trigger	I <sub>GD</sub>	T <sub>J</sub> = 125 °C, V <sub>DRM</sub> = Rated value	0.1	mA			

SWITCHING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Typical turn-on time	t <sub>gt</sub>	T <sub>J</sub> = 25 °C	0.8			
Typical reverse recovery time	t <sub>rr</sub>	T _ 105 °C	3	μs		
Typical turn-off time	t <sub>q</sub>	T <sub>J</sub> = 125 °C	100			



#### www.vishay.com

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THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER		SYMBOL	SYMBOL TEST CONDITIONS		UNITS	
Maximum junction and storage temperature range		T <sub>J</sub> , T <sub>Stg</sub>		- 40 to 125	°C	
Maximum thermal resistance, junction to case		R <sub>thJC</sub>	DC operation	1.5		
Maximum thermal resistance, junction to ambient		R <sub>thJA</sub>		62	°C/W	
Typical thermal resistance, case to heatsink		R <sub>thCS</sub>	Mounting surface, smooth and greased	0.5		
Approximate weight				2	g	
Approximate weight				0.07	OZ.	
Mounting torque -	minimum			6 (5)	kgf · cm	
iviounting torque	maximum			12 (10)	(lbf · in)	
Marking device Case style TO-220AB 12T		12TT	S08			

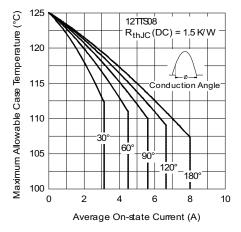


Fig. 1 - Current Ratings Characteristics

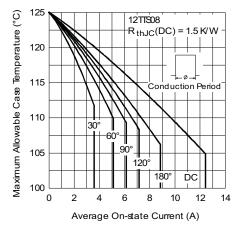


Fig. 2 - Current Ratings Characteristics

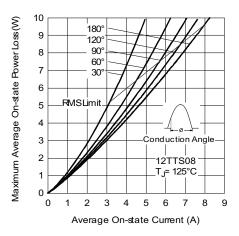


Fig. 3 - On-State Power Loss Characteristics

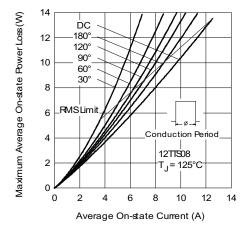


Fig. 4 - On-State Power Loss Characteristics

# Vishay Semiconductors

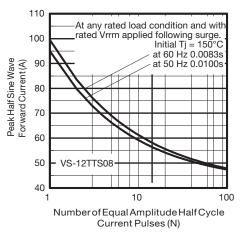


Fig. 5 - Maximum Non-Repetitive Surge Current

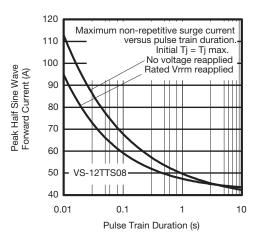


Fig. 6 - Maximum Non-Repetitive Surge Current

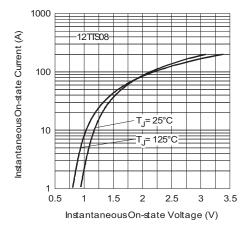


Fig. 7 - On-State Voltage Drop Characteristics

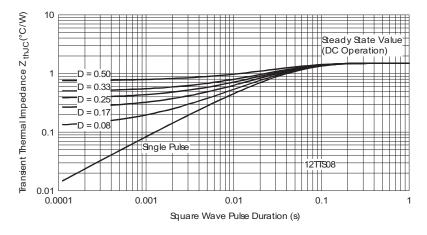


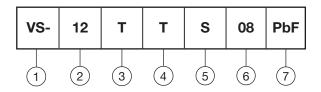
Fig. 8 - Thermal Impedance Z<sub>thJC</sub> Characteristics

# VS-12TTS08PbF, VS-12TTS08-M3

Vishay Semiconductors

#### **ORDERING INFORMATION TABLE**

Device code



1 - Vishay Semiconductors product

Current ratings (12 = 12.5 A)

3 - Circuit configuration:

T = Single thyristor

4 - Package:

T = TO-220

5 - Type of silicon

S = Standard recovery rectifier

6 - Voltage rating (08 = 800 V)

PbF = Lead (Pb)-free and RoHS compliant

-M3 = Halogen-free, RoHS compliant, and terminations lead (Pb)-free

ORDERING INFORMATION (Example)						
PREFERRED P/N QUANTITY PER T/R MINIMUM ORDER QUANTITY PACKAGING DESCRIPTION						
VS-12TTS08PbF	50	1000	Antistatic plastic tubes			
VS-12TTS08-M3	50	1000	Antistatic plastic tubes			

LINKS TO RELATED DOCUMENTS				
Dimensions <u>www.vishay.com/doc?95222</u>				
Dort marking information	TO-220AB PbF	www.vishay.com/doc?95225		
Part marking information	TO-220AB -M3	www.vishay.com/doc?95028		



### Vishay Semiconductors

#### **TO-220AB**

#### **DIMENSIONS** in millimeters and inches



#### Lead assignments

#### **Diodes**

- 1. Anode/open
- 2. Cathode
- 3. Anode

#### Conforms to JEDEC outline TO-220AB

SYMBOL MILLIMETER		IETERS	INC	HES	NOTES
STMBOL	MIN.	MAX.	MIN.	MAX.	NOTES
Α	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
С	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6

SYMBOL	MILLIM	METERS INCHES		NOTES	
STIMBOL	MIN.	MAX.	MIN.	MAX.	NOTES
E	10.11	10.51	0.398	0.414	3, 6
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
е	2.41	2.67	0.095	0.105	
e1	4.88	5.28	0.192	0.208	
H1	6.09	6.48	0.240	0.255	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
ØΡ	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	
θ	90° to 93°		90° t	o 93°	
		•	•	•	

#### Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimensions: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimensions E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, except A2 (maximum) and D2 (minimum) where dimensions are derived from the actual package outline

Lead tip



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