## V40D100C-M3, V40D100CHM3

Vishay General Semiconductor

COMPLIANT

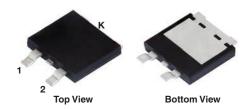
**HALOGEN** 

FREE

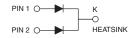
## **Dual High-Voltage Trench MOS Barrier Schottky Rectifier**

Ultra Low  $V_F = 0.40 \text{ V}$  at  $I_F = 5 \text{ A}$ 

### TMBS® eSMP® Series TO-263AC (SMPD)



#### V40D100C



PRIMARY CHARACTERISTICS				
I <sub>F(AV)</sub>	2 x 20 A			
$V_{RRM}$	100 V			
I <sub>FSM</sub>	250 A			
V <sub>F</sub> at I <sub>F</sub> = 20 A (T <sub>A</sub> = 125 °C)	0.63 V			
T <sub>J</sub> max.	150 °C			
Package	TO-263AC (SMPD)			
Diode variations	Dual common cathode			

### **FEATURES**

- Trench MOS Schottky technology
- Very low profile typical height of 1.7 mm
- · Ideal for automated placement
- Low forward voltage drop, low power losses
- · High efficiency operation
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- AEC-Q101 qualified available:
  - Automotive ordering code: base P/NHM3
- Material categorization: for definitions of compliance please see <a href="https://www.vishav.com/doc?99912"><u>www.vishav.com/doc?99912</u></a>

### **TYPICAL APPLICATIONS**

For use in high frequency DC/DC converters, switching power supplies, freewheeling diodes, OR-ing diode, and reverse battery protection in commercial, inductrial, and automotive application.

### **MECHANICAL DATA**

Case: TO-263AC (SMPD)

Molding compound meets UL 94 V-0 flammability rating

Base P/N-M3 - halogen-free, RoHS-compliant

Base P/NHM3 - halogen-free, RoHS-compliant, and

AEC-Q101 qualified

Terminals: Matte tin plated leads, solderable per

J-STD-002 and JESD 22-B102

M3 and HM3 suffix meets JESD 201 class 2 whisker test

Polarity: As marked

MAXIMUM RATINGS (T <sub>A</sub> = 25 °C unless otherwise noted)					
PARAMETER		SYMBOL	V40D100C	UNIT	
Maximum repetitive peak reverse voltage		$V_{RRM}$	100	V	
Maximum average forward rectified current (fig. 1)	per device	I <sub>F(AV)</sub>	40	А	
	per diode		20		
Peak forward surge current 10 ms single half sine-wave superimposed on rated load		I <sub>FSM</sub>	250	А	
Voltage rate of change (rated V <sub>R</sub> )		dV/dt	10 000	V/µs	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>STG</sub>	-40 to +150	°C	



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<b>ELECTRICAL CHARACTERISTICS</b> (T <sub>A</sub> = 25 °C unless otherwise noted)							
PARAMETER	TEST CONDITIONS		SYMBOL	TYP.	MAX.	UNIT	
Instantaneous forward voltage per diode	I <sub>F</sub> = 5 A	T <sub>A</sub> = 25 °C	V <sub>F</sub> <sup>(1)</sup>	0.48	-	V	
	I <sub>F</sub> = 10 A			0.56	-		
	I <sub>F</sub> = 20 A			0.71	0.75		
	I <sub>F</sub> = 5 A	T <sub>A</sub> = 125 °C		0.40	-		
	I <sub>F</sub> = 10 A			0.51	-		
	I <sub>F</sub> = 20 A			0.63	0.69		
Reverse current at rated V <sub>R</sub> per diode	V <sub>R</sub> = 70 V	T <sub>A</sub> = 25 °C	I <sub>R</sub> <sup>(2)</sup>	11	-	μA	
		T <sub>A</sub> = 125 °C		11	-	mA	
	V - 1 1 1 1 V	T <sub>A</sub> = 25 °C		-	1000	μA	
		T <sub>A</sub> = 125 °C		24	80	mA	

#### **Notes**

(1) Pulse test: 300 µs pulse width, 1 % duty cycle

(2) Pulse test: Pulse width ≤ 5 ms

THERMAL CHARACTERISTICS (T <sub>A</sub> = 25 °C unless otherwise noted)				
PARAMETER		SYMBOL	V40D100C	UNIT
	per diode	$R_{ heta JC}$	1.9	
Typical thermal resistance	per device		1.0	°C/W
	per device	R <sub>0JA</sub> (1)(2)	45	

#### Notes

(1) The heat generated must be less than the thermal conductivity from junction-to-ambient: dP<sub>D</sub>/dT<sub>J</sub> < 1/R<sub>6JA</sub>

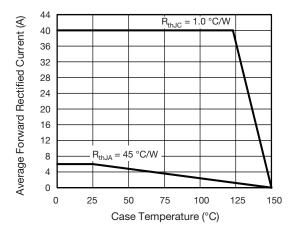
(2) Free air, without heatsink

ORDERING INFORMATION (Example)					
PACKAGE	PREFERRED P/N	UNIT WEIGHT (g)	PACKAGE CODE	BASE QUANTITY	DELIVERY MODE
SMPD	V40D100C-M3/I	0.55	I	2000/reel	13" diameter plastic tape and reel
SMPD	V40D100CHM3/I (1)	0.55	I	2000/reel	13" diameter plastic tape and reel

#### Note

(1) AEC-Q101 qualified

### RATINGS AND CHARACTERISTICS CURVES (T<sub>A</sub> = 25 °C unless otherwise noted)





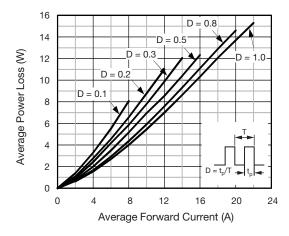


Fig. 2 - Forward Power Loss Characteristics Per Diode

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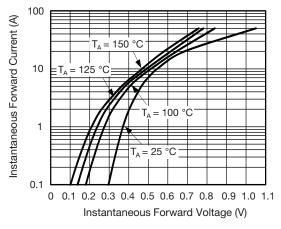


Fig. 3 - Typical Instantaneous Forward Characteristics Per Diode

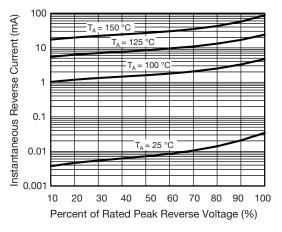


Fig. 4 - Typical Reverse Characteristics Per Diode

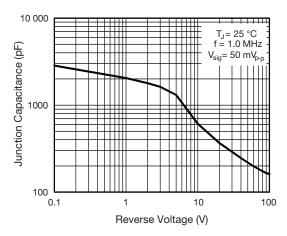


Fig. 5 - Typical Junction Capacitance Per Diode

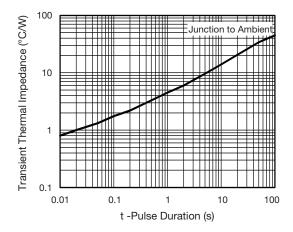


Fig. 6 - Typical Transient Thermal Impedance Per Device

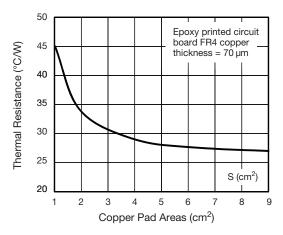
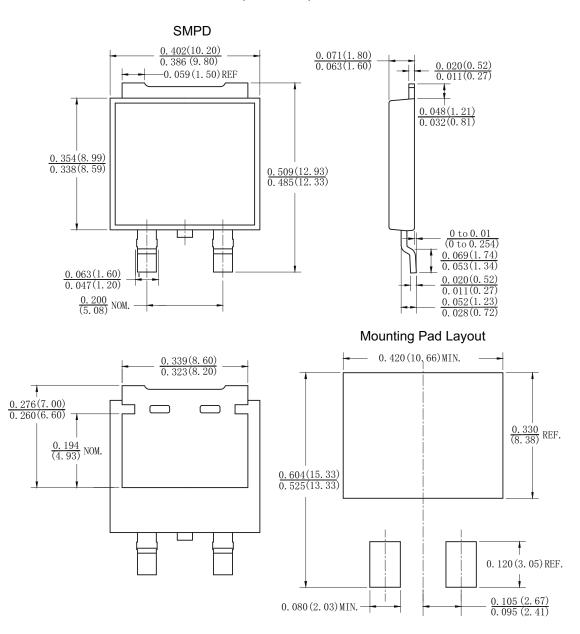


Fig. 7 - Thermal Resistance Junction-to-Ambient vs. Copper Pad Areas



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### PACKAGE OUTLINE DIMENSIONS in inches (millimeters)





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