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Vishay Siliconix

P-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^d			
-40	0.0042 at V _{GS} = -10 V	-110			
-40	0.0062 at V _{GS} = -4.5 V	-110			

FEATURES

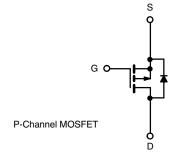
- TrenchFET® Power MOSFET
- Low thermal resistance











Ordering Information:

SUM110P04-04L-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS (T _C =	= 25 °C, unless otherw	rise noted)		
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	-40	V
Gate-Source Voltage	V _{GS}	± 20	v	
Continuous Drain Current (T,I = 175 °C) d	T _C = 25 °C		-110	A
Continuous Drain Current (1) = 175 C) °	T _C = 125 °C	l l ^D	-110	
Pulsed Drain Current		I _{DM}	-240	_ A
Avalanche Current	L = 0.1 mH	I _{AS}	-75	
Single Pulse Avalanche Energy ^a	L = 0.1 IIII	E _{AS}	281	mJ
Dower Discinstion	T _C = 25 °C	PD	375 ^c	w
Power Dissipation	T _A = 25 °C b		3.75	vv
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 175	°C

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction-to-Ambient PCB Mount ^b	R _{thJA}	40	°C/W		
Junction-to-Case	R_{thJC}	0.4			

Notes

- a. Duty cycle ≤ 1 %.
- b. When mounted on 1" square PCB (FR-4 material).
- c. See SOA curve for voltage derating.
- d. Limited by package.



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static	•						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-40		V		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-1		-3	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current		V _{DS} = -40 V, V _{GS} = 0 V			-1	μА	
	I _{DSS}	V _{DS} = -40 V, V _{GS} = 0 V, T _J = 125 °C			-50		
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 175 °C			-250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-120			Α	
		V _{GS} = -10 V, I _D = -30 A		0.0034	0.0042	Ω	
Drain Cauras On State Besistance 3		V _{GS} = -10 V, I _D = -30 A, T _J = 125 °C			0.0063		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = -10 V, I _D = -30 A, T _J = 175 °C			0.0076		
		$V_{GS} = -4.5 \text{ V}, I_D = -20 \text{ A}$		0.005	0.0062		
Forward Transconductance ^a	9fs	V _{DS} = -15 V, I _D = -30 A	20			S	
Dynamic ^b							
Input Capacitance	C _{iss}			11 200		pF	
Output Capacitance	Coss	$V_{GS} = 0 \text{ V}, V_{DS} = -25 \text{ V}, f = 1 \text{ MHz}$		1650			
Reverse Transfer Capacitance	C _{rss}			1200			
Total Gate Charge ^c	Qg			235	350	nC	
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = -20 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -110 \text{ A}$		45			
Gate-Drain Charge ^c	Q_{gd}			65			
Gate Resistance	R_g			3		Ω	
Turn-On Delay Time ^c	t _{d(on)}			25	40		
Rise Time ^c	t _r	$V_{DD} = -20 \text{ V}, R_1 = 0.18 \Omega$		30	45		
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong -110 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 2.5 \Omega$		190	300	ns	
Fall Time ^c	t _f			110	165		
Source-Drain Diode Ratings and Cha	racteristics	(T _C = 25 °C) ^b					
Continuous Current	I _S				-110		
Pulsed Current	I _{SM}	I _{SM}			-240	Α	
Forward Voltage ^a	V_{SD}	$I_F = -85 \text{ A}, V_{GS} = 0 \text{ V}$		-1	-1.5	V	
Reverse Recovery Time	t _{rr}			65	100	ns	
Peak Reverse Recovery Current	I _{RM(REC)}	I _F = -85 A, dl/dt = 100 A/μs		-3.7	-5.6	Α	
Reverse Recovery Charge	Q _{rr}			0.12	0.28	μC	

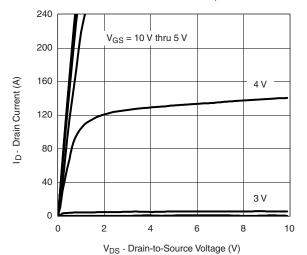
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

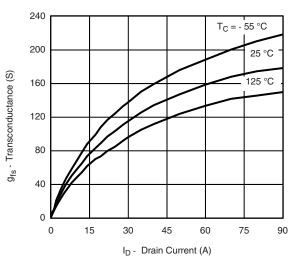
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



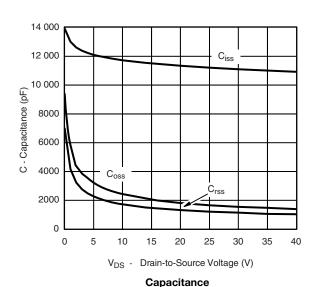
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

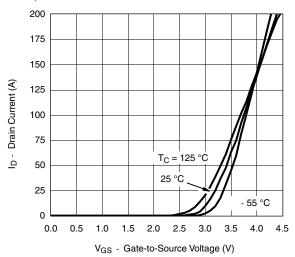


Output Characteristics

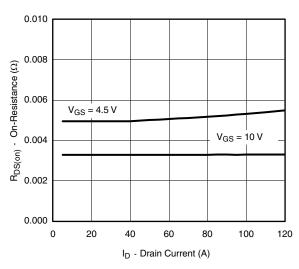


Transconductance

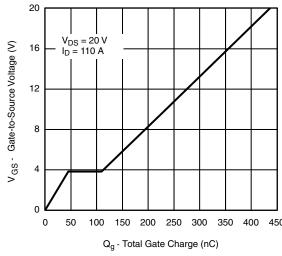




Transfer Characteristics

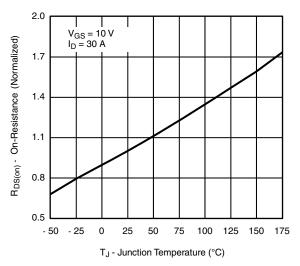


On-Resistance vs. Drain Current

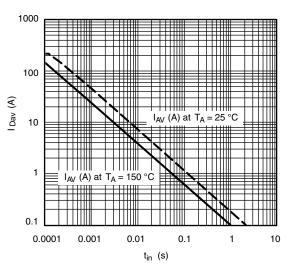




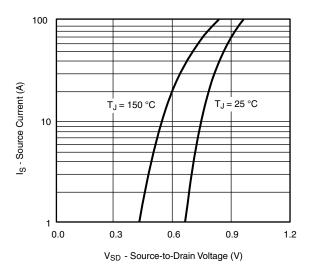
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



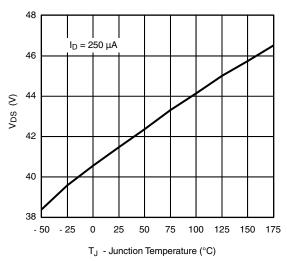
On-Resistance vs. Junction Temperature



Avalanche Current vs. Time



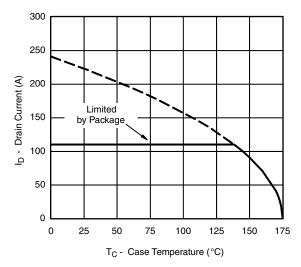
Source-Drain Diode Forward Voltage



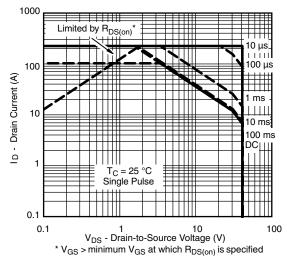
Drain Source Breakdown vs. Junction Temperature



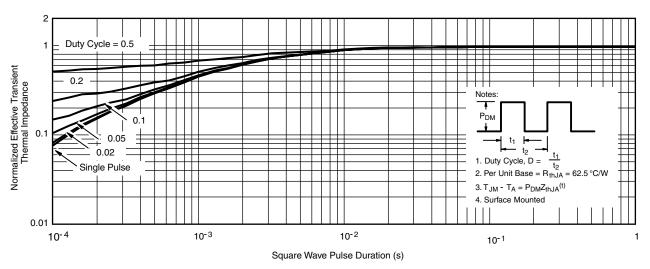
THERMAL RATINGS



Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72437.



TO-263 (D²PAK): 3-LEAD









DETAIL A (ROTATED 90°)



_ - b1 , , ,	
≥ 	- -

- 1. Plane B includes maximum features of heat sink tab and plastic.
- 2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- 3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB. Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

6. This feature is for thick lead.

DIM. MIN.		HES	MILLIMETERS			
		MIN.	MAX.	MIN.	MAX.	
Α		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
	D4	0.044	0.052	1.118	1.321	
	Е	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	=	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
е		0.100	00 BSC 2.54 BSC		BSC	
K		0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
	L2	0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
	L4	0.010) BSC	0.254	54 BSC	
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13						

DWG: 5843





RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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Revision: 13-Jun-16 1 Document Number: 91000

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