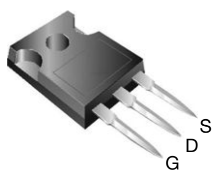
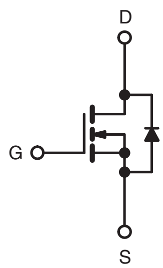
D Series Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	V_{GS} = 10 V	0.4
Q_g (Max.) (nC)	58	
Q_{gs} (nC)	8	
Q_{gd} (nC)	14	
Configuration	Single	

TO-247AC





N-Channel MOSFET

FEATURES

- Optimal Design
  - Low Area Specific On-Resistance
  - Low Input Capacitance (C_{iss})
  - Reduced Capacitive Switching Losses
  - High Body Diode Ruggedness
  - Avalanche Energy Rated (UIS)
- Optimal Efficiency and Operation
  - Low Cost
  - Simple Gate Drive Circuitry
  - Low Figure-of-Merit (FOM): R_{on} x Q_g
  - Fast Switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS* COMPLIANT
HALOGEN FREE Available

Note

* Lead (Pb)-containing terminations are not RoHS-compliant. Exemptions may apply.

APPLICATIONS

- Consumer Electronics
  - Displays (LCD or Plasma TV)
- Server and Telecom Power Supplies
  - SMPS
- Industrial
  - Welding, Induction Heating, Motor Drives
- Battery Chargers

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free	SiHG14N50D-E3
Lead (Pb)-free and Halogen-free	SiHG14N50D-GE3

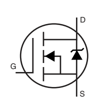
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Gate-Source Voltage AC (f > 1 Hz)				30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	14	A
		T_C = 100 °C		9	
Pulsed Drain Current[a]			I_{DM}	38	
Linear Derating Factor				1.6	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	56	mJ
Maximum Power Dissipation			P_D	208	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	24	V/ns
Reverse Diode dV/dt[d]				0.4	
Soldering Recommendations (Peak Temperature)	for 10 s			300[c]	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.3 mH, R_g = 25 Ω, I_{AS} = 7 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.6	°C/W

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 250 μA	-	0.58	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	3.0	-	5.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	10	μA
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7 A	-	0.320	0.40	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = 50 V, I_D = 7 A	-	5.2	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	1144	-	pF
Output Capacitance	C_{oss}		-	100	-	pF
Reverse Transfer Capacitance	C_{rss}		-	12	-	pF
Effective Output Capacitance, Energy related[a]	$C_{o(er)}$	V_{GS} = 0 V, V_{DS} = 0 V to 400 V	-	87	-	pF
Effective Output Capacitance, Time related[b]	$C_{o(tr)}$		-	125	-	pF
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 7 A, V_{DS} = 400 V	-	29	58	nC
Gate-Source Charge	Q_{gs}		-	8	-	nC
Gate-Drain Charge	Q_{gd}		-	14	-	nC
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 7 A, R_g = 9.1 Ω, V_{GS} = 10 V	-	16	32	ns
Rise Time	t_r		-	27	54	ns
Turn-Off Delay Time	$t_{d(off)}$		-	29	58	ns
Fall Time	t_f		-	26	52	ns
Gate Input Resistance	R_g	f = 1 MHz, open drain	-	1.7	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	14	A
Pulsed Diode Forward Current	I_{SM}		-	-	56	A
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 7 A, V_{GS} = 0 V	-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 7 A, dI/dt = 100 A/μs, V_R = 20 V	-	319	-	ns
Reverse Recovery Charge	Q_{rr}		-	3.0	-	μC
Reverse Recovery Current	I_{RRM}		-	18	-	A

Note

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

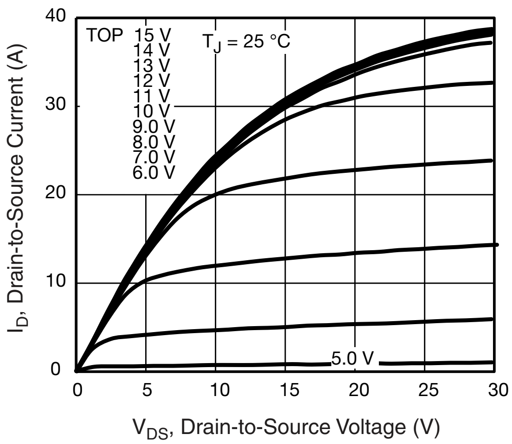


Fig. 1 - Typical Output Characteristics

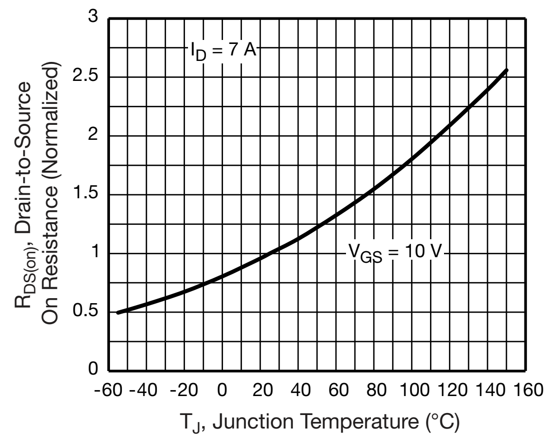


Fig. 4 - Normalized On-Resistance vs. Temperature

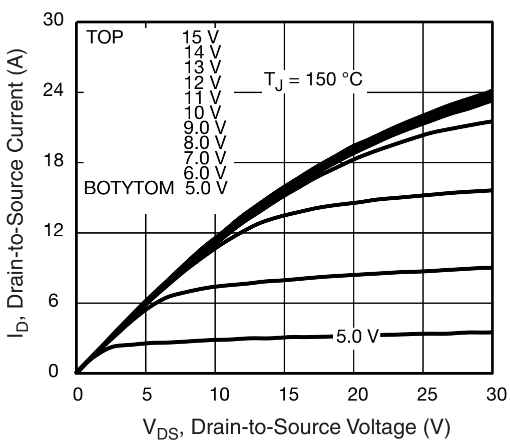


Fig. 2 - Typical Output Characteristics

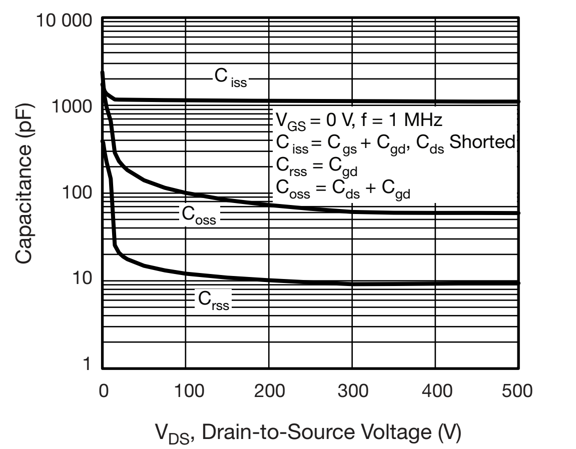


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

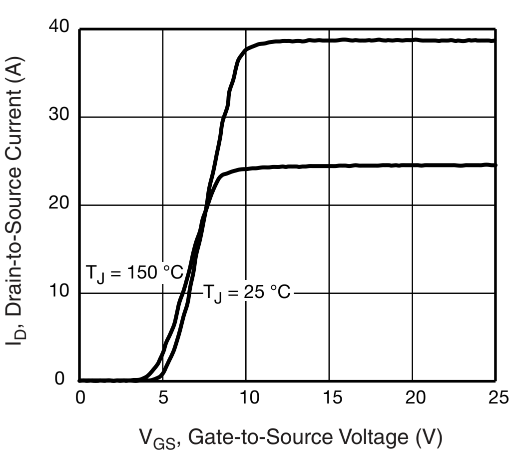


Fig. 3 - Typical Transfer Characteristics

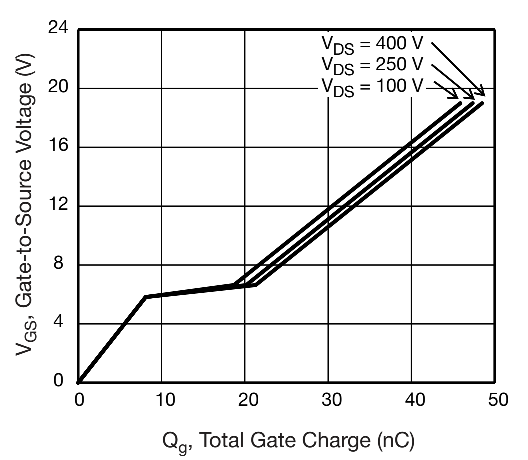


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

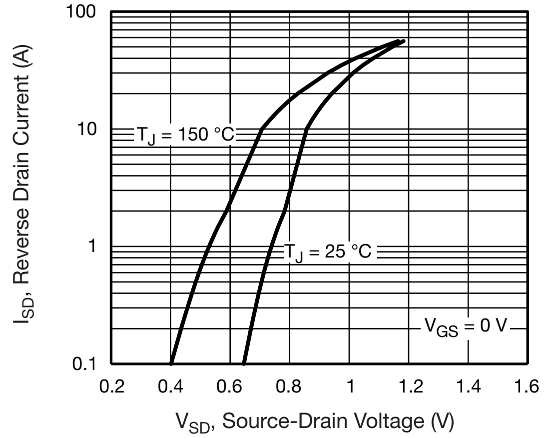


Fig. 7 - Typical Source-Drain Diode Forward Voltage

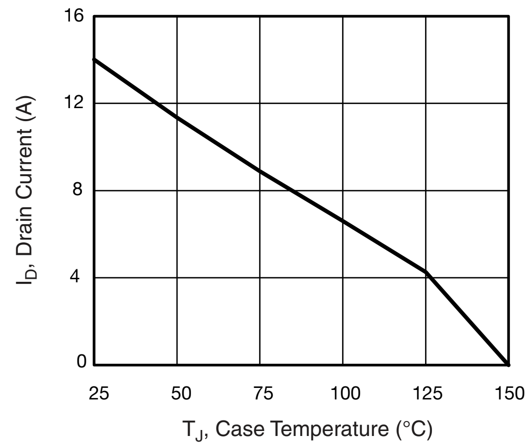


Fig. 9 - Maximum Drain Current vs. Case Temperature

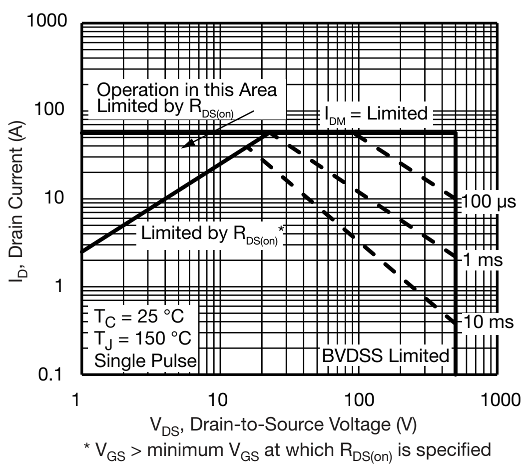


Fig. 8 - Maximum Safe Operating Area

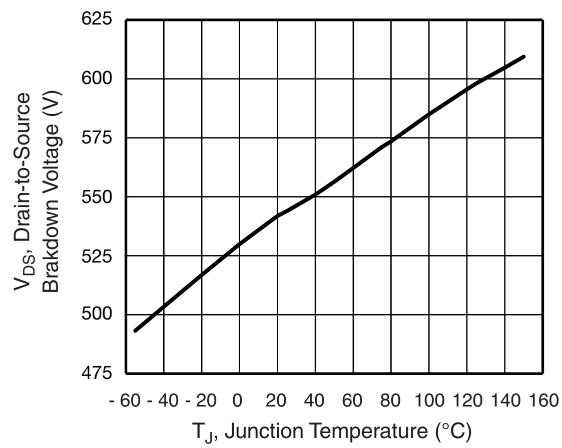


Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

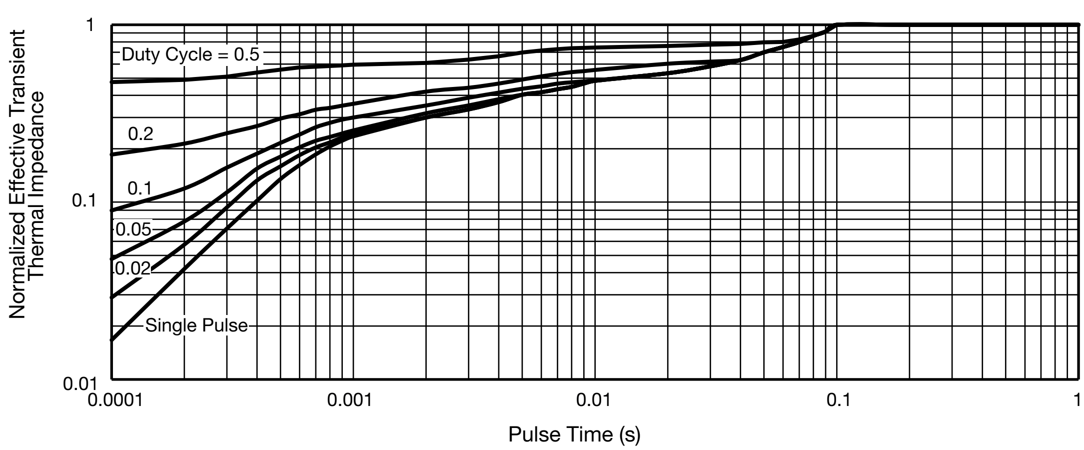


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

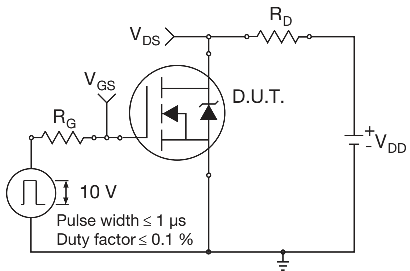


Fig. 12 - Switching Time Test Circuit

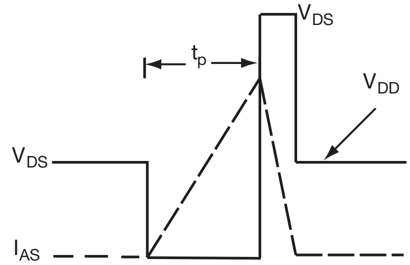


Fig. 15 - Unclamped Inductive Waveforms

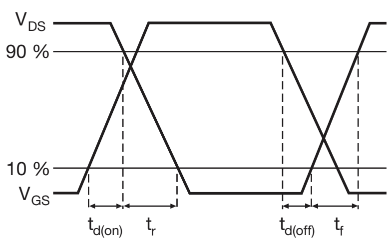


Fig. 13 - Switching Time Waveforms

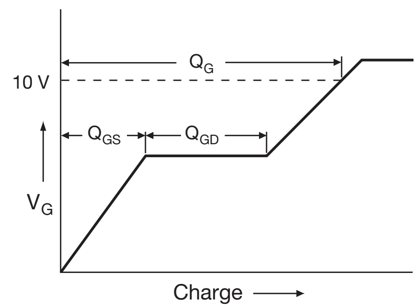


Fig. 16 - Basic Gate Charge Waveform

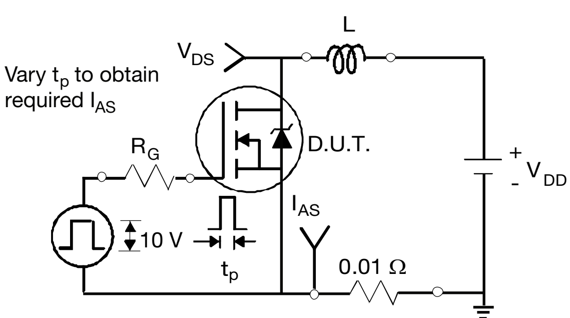


Fig. 14 - Unclamped Inductive Test Circuit

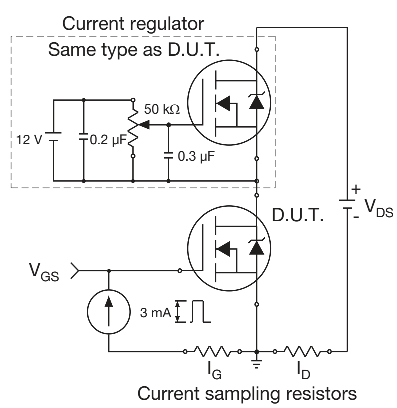
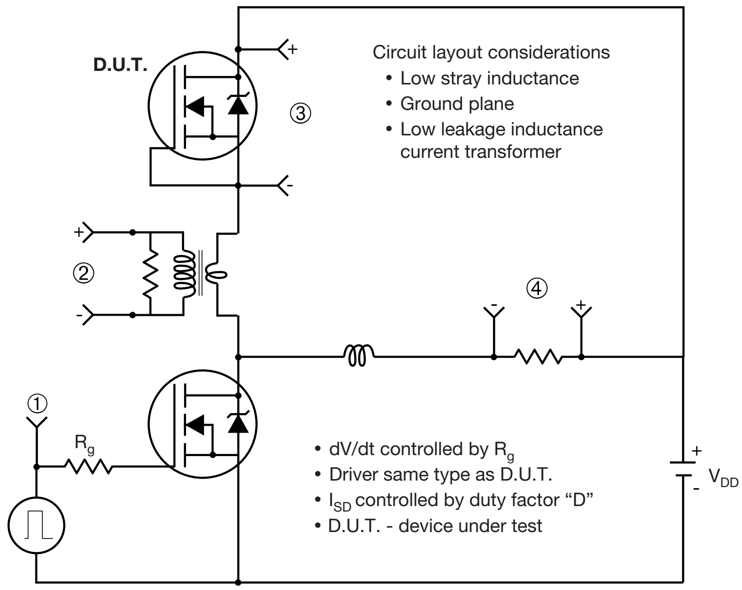
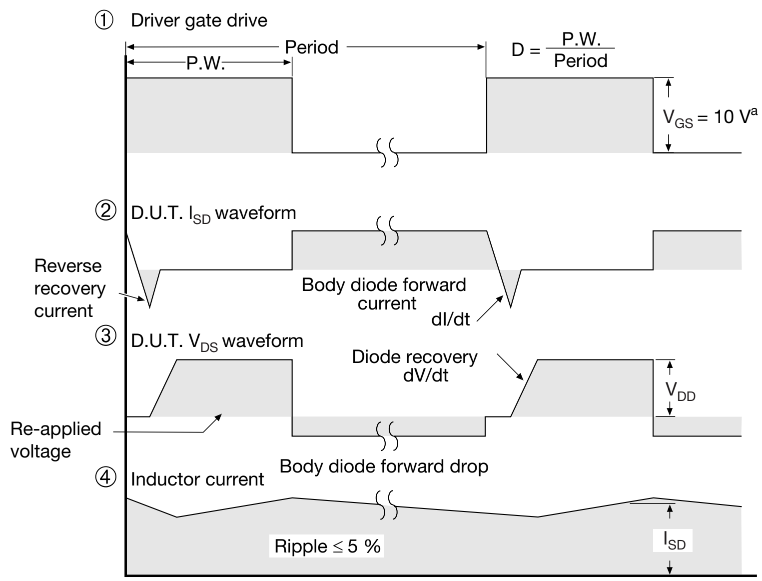


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





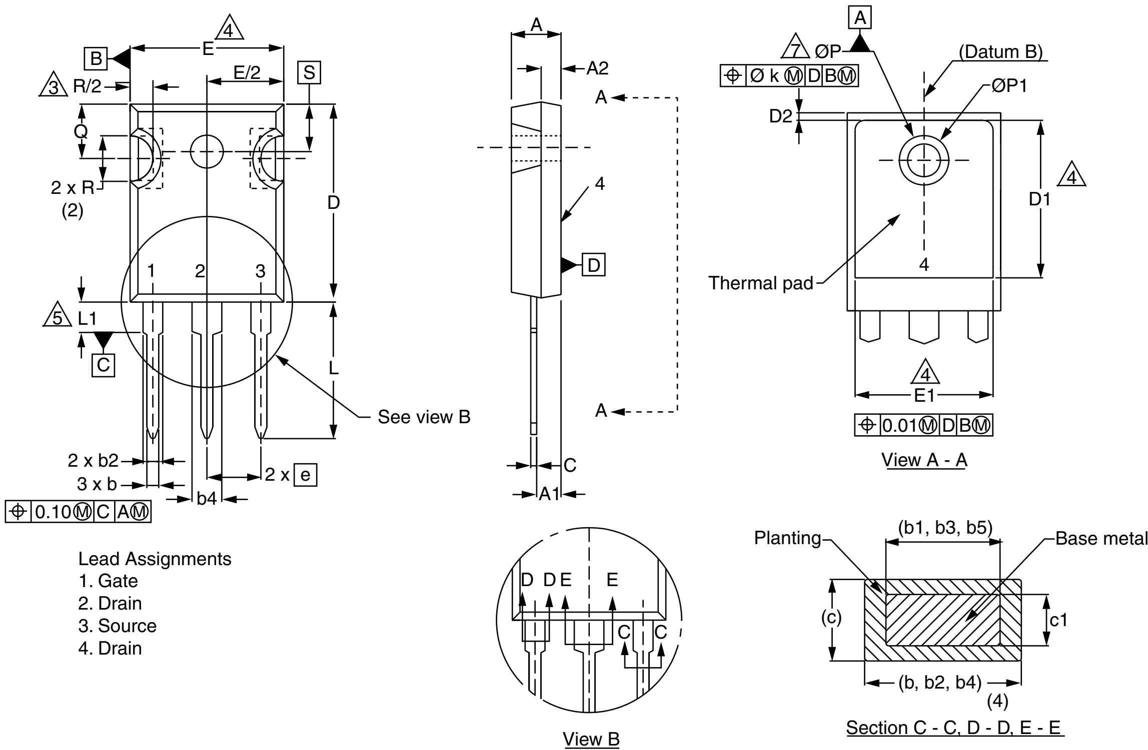
Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91513.

TO-247AC (High Voltage)



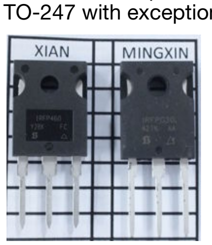
	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
A	4.58	5.31	0.180	0.209
A1	2.21	2.59	0.087	0.102
A2	1.17	2.49	0.046	0.098
b	0.99	1.40	0.039	0.055
b1	0.99	1.35	0.039	0.053
b2	1.53	2.39	0.060	0.094
b3	1.65	2.37	0.065	0.093
b4	2.42	3.43	0.095	0.135
b5	2.59	3.38	0.102	0.133
c	0.38	0.86	0.015	0.034
c1	0.38	0.76	0.015	0.030
D	19.71	20.82	0.776	0.820
D1	13.08	-	0.515	-

	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D2	0.51	1.30	0.020	0.051
E	15.29	15.87	0.602	0.625
E1	13.72	-	0.540	-
e	5.46 BSC		0.215 BSC	
Ø k	0.254		0.010	
L	14.20	16.25	0.559	0.640
L1	3.71	4.29	0.146	0.169
N	7.62 BSC		0.300 BSC	
Ø P	3.51	3.66	0.138	0.144
Ø P1	-	7.39	-	0.291
Q	5.31	5.69	0.209	0.224
R	4.52	5.49	0.178	0.216
S	5.51 BSC		0.217 BSC	

ECN: X13-0103-Rev. D, 01-Jul-13
DWG: 5971

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Contour of slot optional.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions D1 and E1.
5. Lead finish uncontrolled in L1.
6. Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154").
7. Outline conforms to JEDEC outline TO-247 with exception of dimension c.
8. Xian and Mingxin actually photo.



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