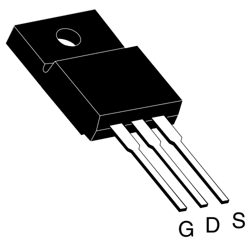
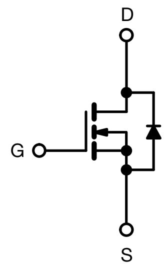
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	400	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.55
Q_g max. (nC)	66	
Q_{gs} (nC)	10	
Q_{gd} (nC)	33	
Configuration	Single	

TO-220 FULLPAK





N-Channel MOSFET

FEATURES

- Isolated package
- High voltage isolation = 2.5 kV_{RMS} (t = 60 s; f = 60 Hz)
- Sink to lead creepage distance = 4.8 mm
- Dynamic dV/dt rating
- Low thermal resistance
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Available
RoHS*
Available

Note
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non-RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details.

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.
The TO-220 FULLPAK eliminates the need for additional insulating hardware in commercial-industrial applications. The molding compound used provides a high isolation capability and a low thermal resistance between the tab and external heatsink. The isolation is equivalent to using a 100 micron mica barrier with standard TO-220 product. The FULLPAK is mounted to a heatsink using a single clip or by a single screw fixing.

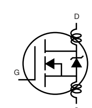
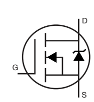
ORDERING INFORMATION	
Package	TO-220 FULLPAK
Lead (Pb)-free	IRFI740GPbF
	SiHFI740G-E3
SnPb	IRFI740G
	SiHFI740G

ABSOLUTE MAXIMUM RATINGS TC = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	400	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	5.4	A
		T_C = 100 °C		3.4	
Pulsed Drain Current [a]			I_{DM}	22	
Linear Derating Factor				0.32	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	390	mJ
Repetitive Avalanche Current [a]			I_{AR}	5.4	A
Repetitive Avalanche Energy [a]			E_{AR}	4.0	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	40	W
Peak Diode Recovery dV/dt [c]			dV/dt	4.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak temperature) [d]	for 10 s			300	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 23 mH, R_g = 25 Ω, I_{AS} = 5.4 A (see fig. 12).
c. $I_{SD} \leq$ 10 A, dI/dt $\leq$ 120 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	65	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	3.1	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	400	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA	-	0.49	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 400 V, V_{GS} = 0 V	-	-	25	μA
		V_{DS} = 320 V, V_{GS} = 0 V, T_J = 125 °C	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 3.2 A [b]	-	-	0.55	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 3.2 A [b]	3.6	-	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 5	-	1370	-	pF
Output Capacitance	C_{oss}		-	380	-	
Reverse Transfer Capacitance	C_{rss}		-	140	-	
Drain to Sink Capacitance	C	f = 1.0 MHz	-	12	-	
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 10 A, V_{DS} = 320 V, see fig. 6 and 13 [b]	-	-	66	nC
Gate-Source Charge	Q_{gs}		-	-	10	
Gate-Drain Charge	Q_{gd}		-	-	33	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 200 V, I_D = 10 A, R_g = 9.1 Ω, R_D= 20 Ω, see fig. 10 [b]	-	14	-	ns
Rise Time	t_r		-	25	-	
Turn-Off Delay Time	$t_{d(off)}$		-	54	-	
Fall Time	t_f		-	24	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Gate Input Resistance	R_g	f = 1 MHz, open drain	0.2	-	1.3	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	5.4	A
Pulsed Diode Forward Current [a]	I_{SM}		-	-	22	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 5.4 A, V_{GS} = 0 V [b]	-	-	2.0	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 10 A, dI/dt = 100 A/μs [b]	-	330	730	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	2.8	6.6	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

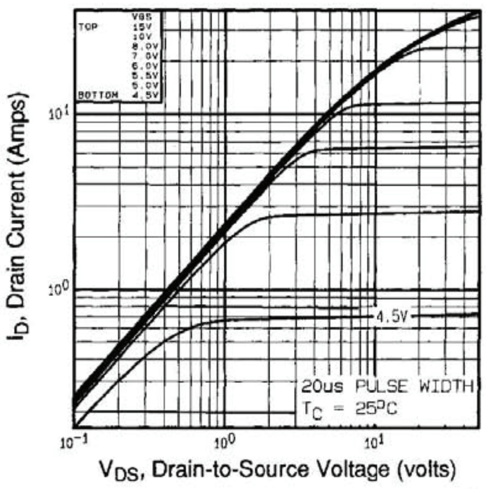


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

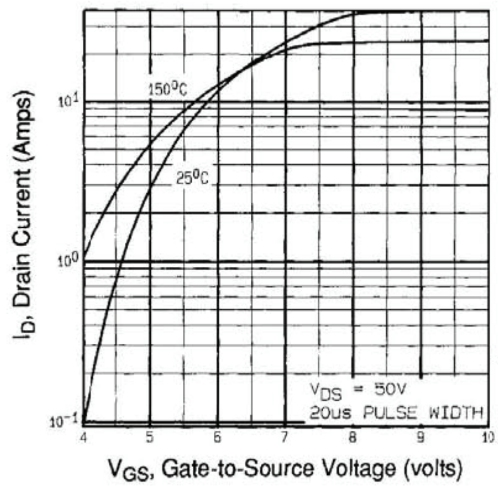


Fig. 3 - Typical Transfer Characteristics

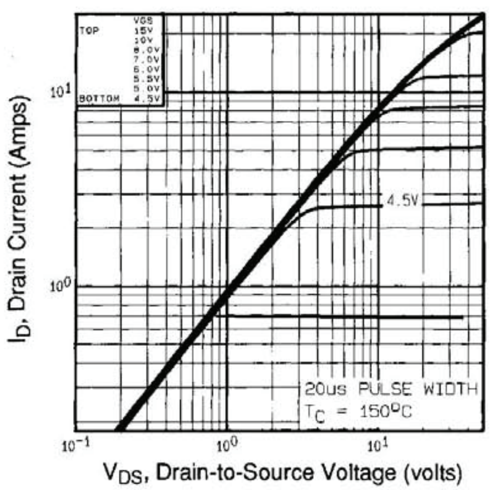


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

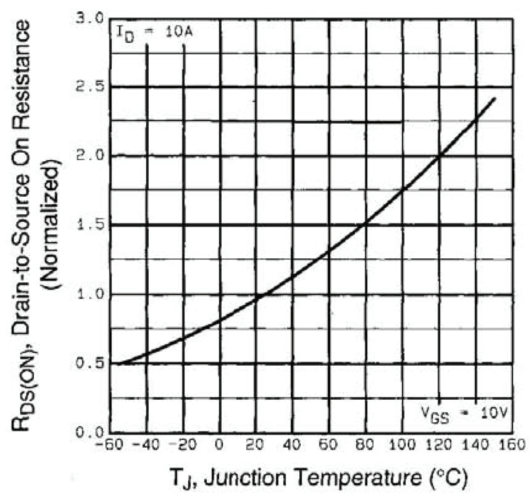


Fig. 4 - Normalized On-Resistance vs. Temperature

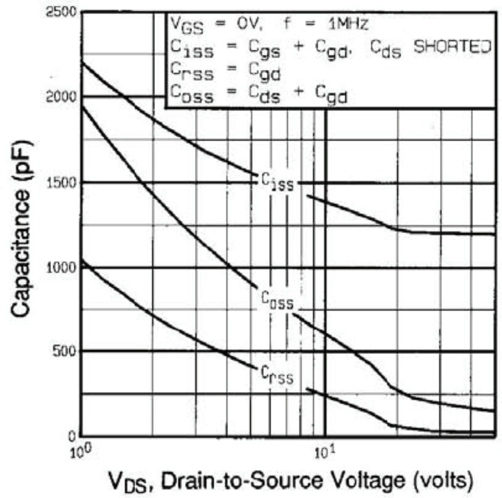


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

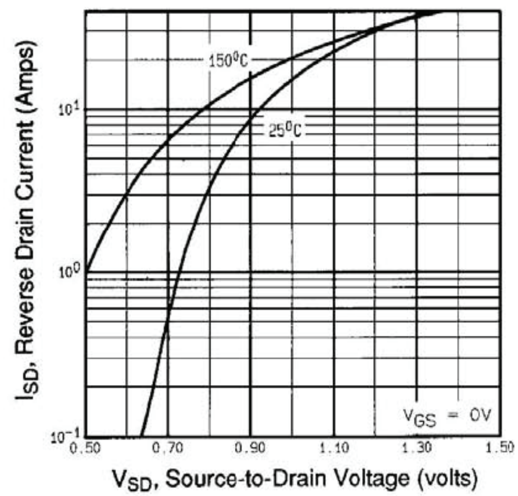


Fig. 7 - Typical Source-Drain Diode Forward Voltage

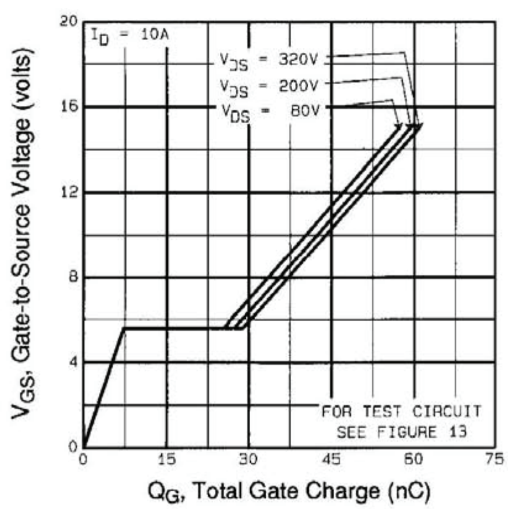


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

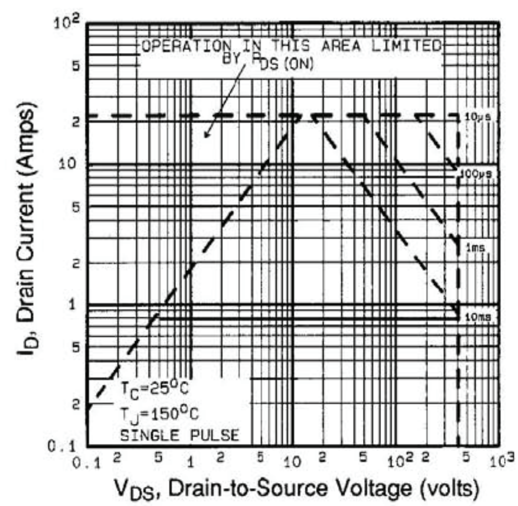


Fig. 8 - Maximum Safe Operating Area

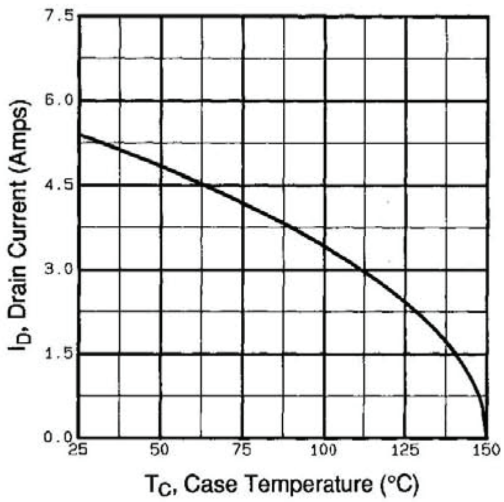


Fig. 9 - Maximum Drain Current vs. Case Temperature

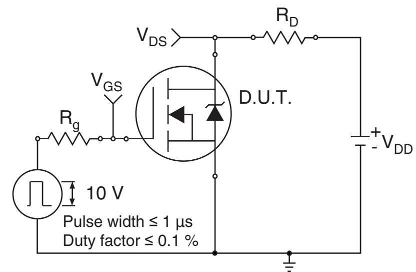


Fig. 10a - Switching Time Test Circuit

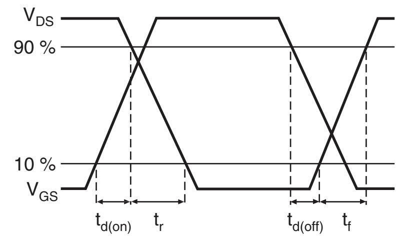


Fig. 10b - Switching Time Waveforms

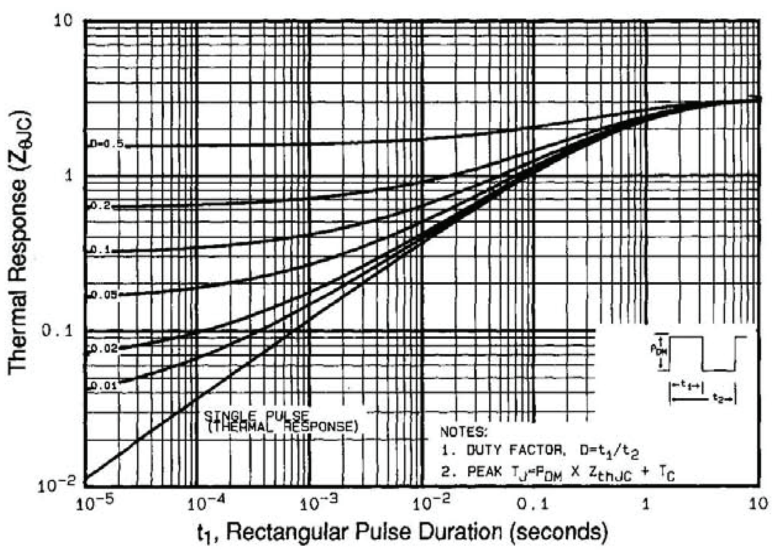


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

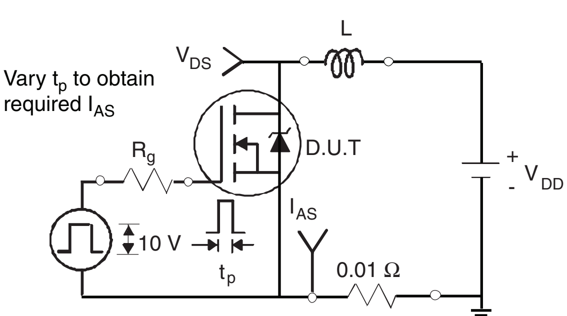


Fig. 12a - Unclamped Inductive Test Circuit

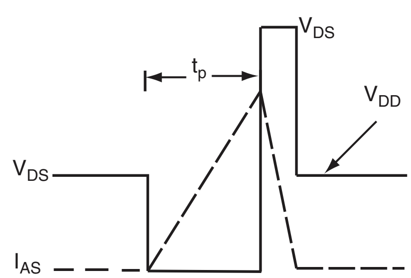


Fig. 12b - Unclamped Inductive Waveforms

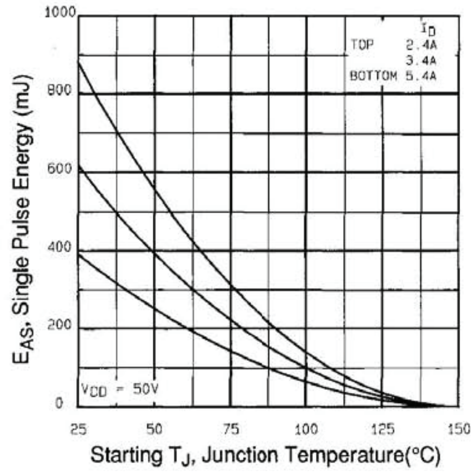


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

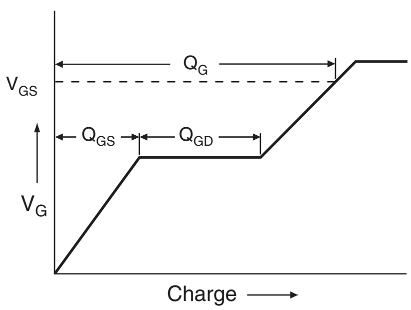


Fig. 13a - Basic Gate Charge Waveform

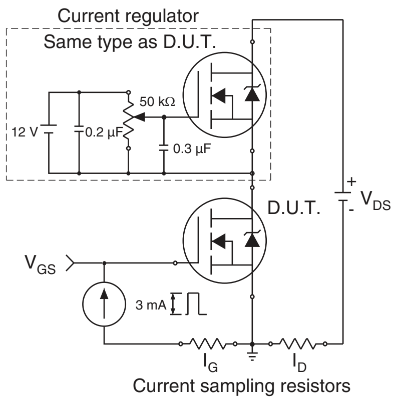
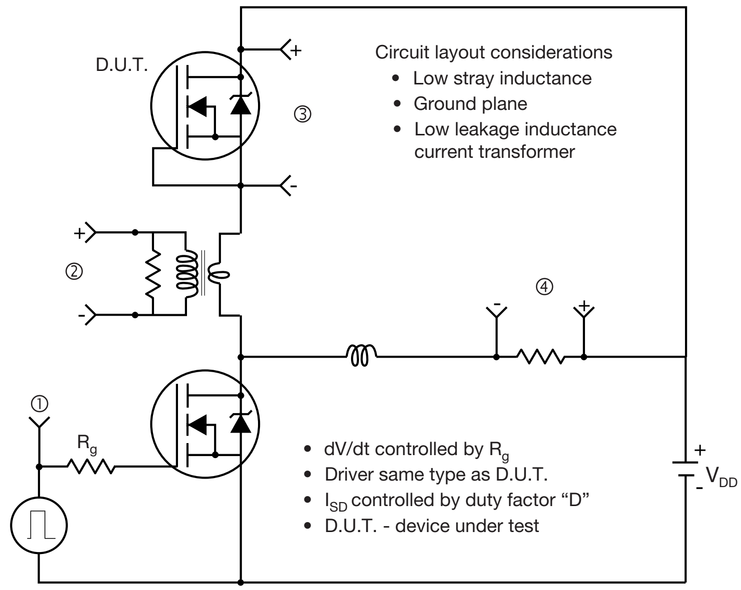
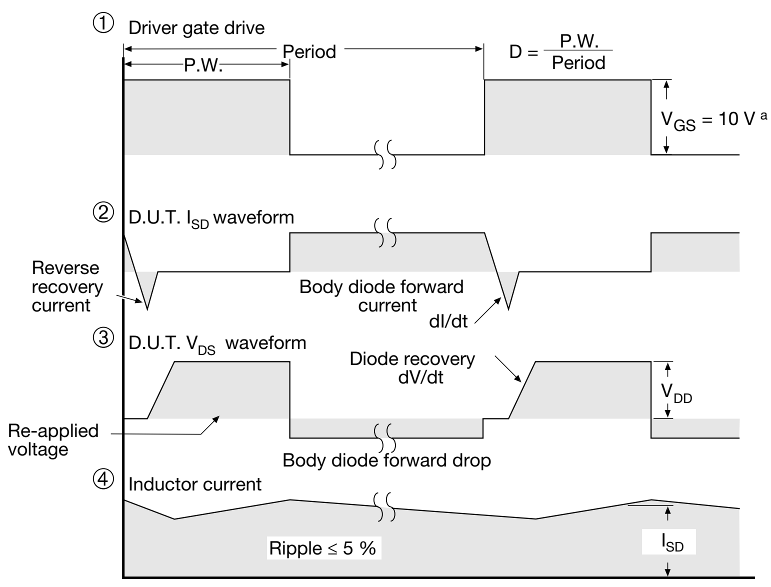


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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