

Vishay Siliconix

N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY									
V _{DS} (V)	$R_{DS(on)}$ (Ω) Max.	I _D (A) ^a	Q _g (Typ.)						
	0.0150 at V _{GS} = 4.5 V	12							
20	0.0166 at V _{GS} = 2.5 V	12	13 nC						
20	0.0200 at V _{GS} = 1.8 V	12	13110						
	0.0324 at V _{GS} = 1.5 V	12							

FEATURES

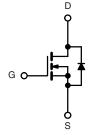
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

COMPLIANT HALOGEN

FREE

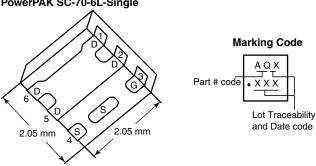
APPLICATIONS

- For Smart Phones and Mobile Computing
 - Load Switches
 - DC/DC Converters



N-Channel MOSFET

PowerPAK SC-70-6L-Single



Ordering Information:

SiA448DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	(T _A = 25 °C, unle	ss otherwise i	noted)		
Parameter	•	Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	20	V	
Gate-Source Voltage		V_{GS}	± 8	V	
	T _C = 25 °C		12 ^a		
Oasting - Paris Oastat (T. 150.00)	T _C = 70 °C		12 ^a		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	Ι _D	12 ^{a, b, c}		
	T _A = 70 °C		9.9 ^{b, c}	Α	
Pulsed Drain Current (t = 300 μs)	"	I _{DM}	30		
Continuous Source-Drain Diode Current	T _C = 25 °C	-	12 ^a		
Continuous Source-Diain Diode Current	T _A = 25 °C	I _S	2.9 ^{b, c}		
	T _C = 25 °C		19.2		
Maximum Dawar Dissination	T _C = 70 °C	В	12.3	W	
Maximum Power Dissipation	T _A = 25 °C	P_{D}	3.5 ^{b, c}	VV	
	T _A = 70 °C		2.2 ^{b, c}		
Operating Junction and Storage Temperature Ran	nge	T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature)	d, e		260	C	

THERMAL RESISTANCE RATINGS										
Parameter		Symbol	Typical	Maximum	Unit					
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	28	36	°C/W					
Maximum Junction-to-Case (Drain)	Steady State	R _{th.IC}	5.3	6.5	O/ VV					

Notes:

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 80 °C/W.

Document Number: 63918 S12-1138-Rev. A, 21-May-12 For technical questions, contact: pmostechsupport@vishav.com

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)									
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit			
Static				_					
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			V			
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		21		mV/°C			
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	10 = 230 μΑ		- 3					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.4		1	V			
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 8 V$			± 100	nA			
Zero Gate Voltage Drain Current	lana	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$		1					
Zero Gate voltage Diain Guirent	DSS	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	μΑ			
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le 5 V$, $V_{GS} = 4.5 V$	12			Α			
		$V_{GS} = 4.5 \text{ V}, I_D = 12.4 \text{ A}$		0.0125 0.0150					
	D D	$V_{GS} = 2.5 \text{ V}, I_D = 11.8 \text{ A}$		0.0138	0.0166	Ω			
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 1.8 \text{ V}, I_D = 10.8 \text{ A}$		0.0160	0.0200				
		$V_{GS} = 1.5 \text{ V}, I_D = 3 \text{ A}$		0.0180	0.0324	ا ا			
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 12.4 A		70		S			
Dynamic ^b				l					
Input Capacitance	C _{iss}			1380		pF			
Output Capacitance	C _{oss}	$V_{DS} = 1 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		190					
Reverse Transfer Capacitance	C _{rss}			75					
T. 10 . 0	Qg	V _{DS} = 10 V, V _{GS} = 8 V, I _D = 12.4 A		23	35	nC			
Total Gate Charge				13	20				
Gate-Source Charge	Q_{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 12.4 \text{ A}$		2.1					
Gate-Drain Charge	Q_{gd}			1.4					
Gate Resistance	R_{g}	f = 1 MHz	0.6	3.3	6.6	Ω			
Turn-On Delay Time	t _{d(on)}			7	14				
Rise Time	t _r	V_{DD} = 10 V, R_L = 1 Ω		10	20				
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 8 \text{ V}, R_g = 1 \Omega$		27	41				
Fall Time	t _f			6	12				
Turn-On Delay Time	t _{d(on)}			8	16	ns			
Rise Time	t _r	V_{DD} = 10 V, R_L = 1 Ω		13	20				
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		30	45				
Fall Time	t _f			7	14				
Drain-Source Body Diode Characterist	ics				L	L			
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			12 ^c	Α			
Pulse Diode Forward Current	I _{SM}				30				
Body Diode Voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V		0.8	1.2	V			
Body Diode Reverse Recovery Time	t _{rr}			8	16	ns			
Body Diode Reverse Recovery Charge	Q _{rr}	1 10 A 41/44 100 A/ - T 05 20		1	3	nC			
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		4.5					
Reverse Recovery Rise Time	t _b			3.5		ns			

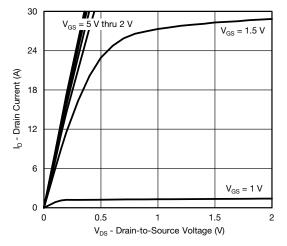
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Package limited

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

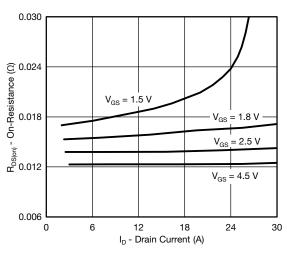


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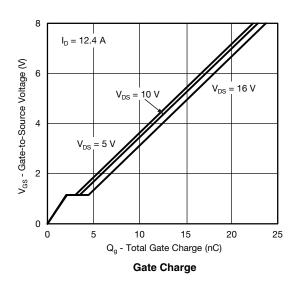
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

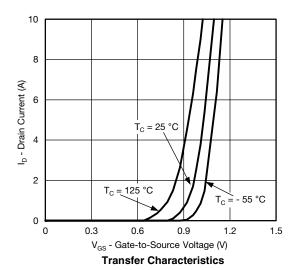


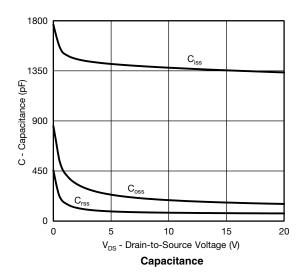
Output Characteristics

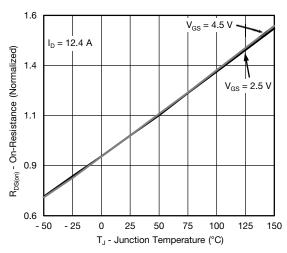


On-Resistance vs. Drain Current and Gate Voltage





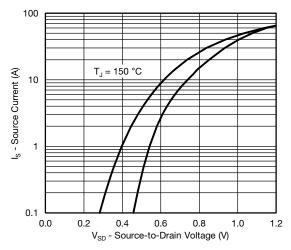




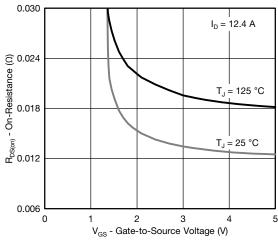
On-Resistance vs. Junction Temperature

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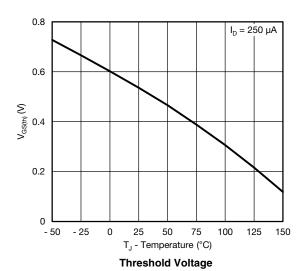
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

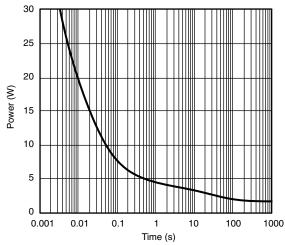


Soure-Drain Diode Forward Voltage

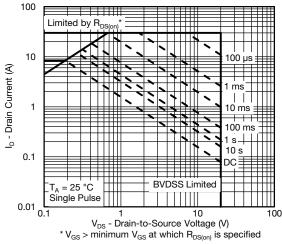


On-Resistance vs. Gate-to-Source Voltage





Single Pulse Power, Junction-to-Ambient

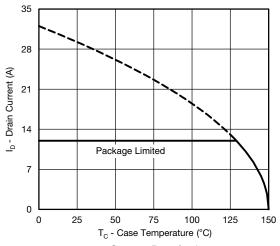


Safe Operating Area, Junction-to-Ambient

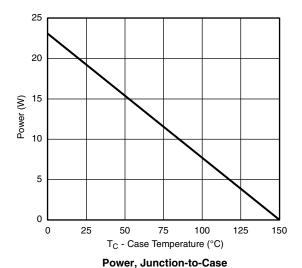


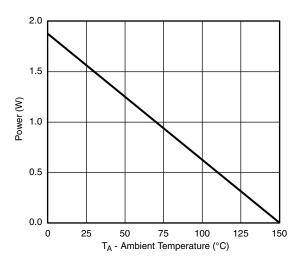
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*



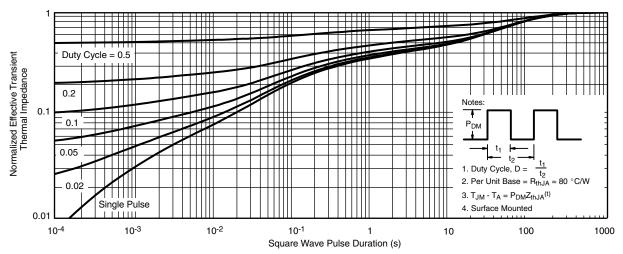


Power, Junction-to-Ambient

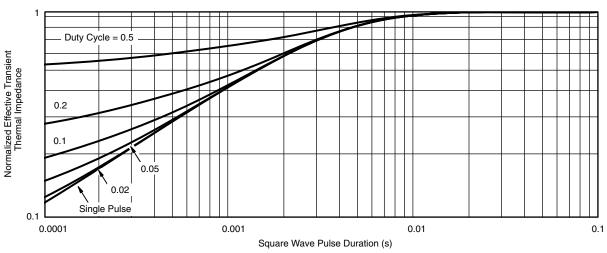
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

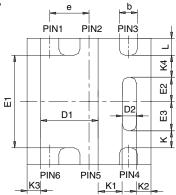
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63918.





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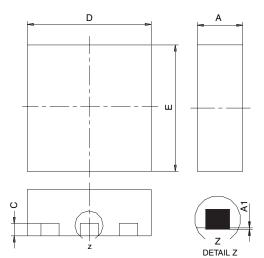
PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

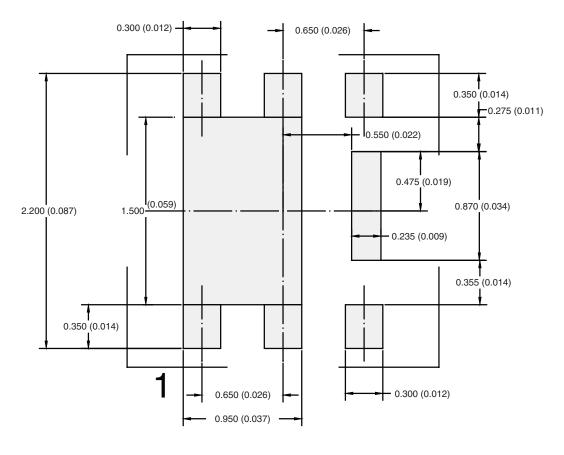
	SINGLE PAD						DUAL PAD					
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A 1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC		
K		0.275 TYP	١		0.011 TYP		0.275 TYP			0.011 TYP		
K1		0.400 TYP	١	0.016 TYP			0.320 TYP			0.013 TYP		
K2		0.240 TYP 0.009 TYP		0.252 TYP			0.010 TYP					
К3		0.225 TYP	1	0.009 TYP								
K4		0.355 TYP		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
Т							0.05	0.10	0.15	0.002	0.004	0.006
FCN: C-07431 - Rev. C. 06-Aug-07												

DWG: 5934

Document Number: 73001 06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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