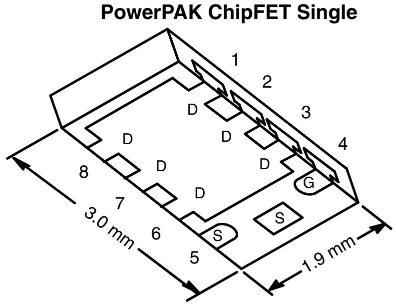
P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) (Max.)	I_D (A)[a]	Q_g (Typ.)
- 20	0.0096 at V_{GS} = - 4.5 V	- 25	43 nC
	0.0132 at V_{GS} = - 2.5 V	- 25	
	0.0220 at V_{GS} = - 1.8 V	- 7	

PowerPAK ChipFET Single



Bottom View

Ordering Information:
Si5415AEDU-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

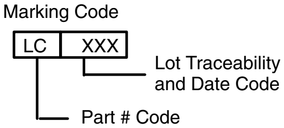
- TrenchFET® Power MOSFET
- Thermally Enhanced PowerPAK® ChipFET Package
  - Small Footprint Area
  - Low On-Resistance
- 100 % R_g and UIS Tested
- Typical ESD Protection: 5500 V (HBM)
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

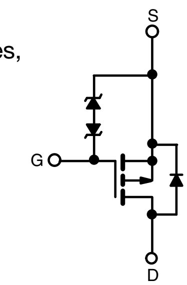
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Portable Devices such as Smart Phones, Tablet PCs and Mobile Computing
  - Battery Switch
  - Load Switch
  - Power Management

Marking Code





P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 20	V
Gate-Source Voltage		V_{GS}	± 8	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	- 25[a]	A
	T_C = 70 °C		- 25[a]	
	T_A = 25 °C		- 15[b, c]	
	T_A = 70 °C		- 12[b, c]	
Pulsed Drain Current (t = 100 μs)		I_{DM}	- 70	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	- 25[a]	
	T_A = 25 °C		- 2.6[b, c]	
Single Avalanche Current	L = 0.1 mH	I_{AS}	- 15	
Single Avalanche Energy		E_{AS}	11	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	31	W
	T_C = 70 °C		20	
	T_A = 25 °C		3.1[b, c]	
	T_A = 70 °C		2[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature)[d, e]			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[b, f]	t ≤ 5 s	R_{thJA}	34	40	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	3	4	

Notes

a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state conditions is 90 °C/W.

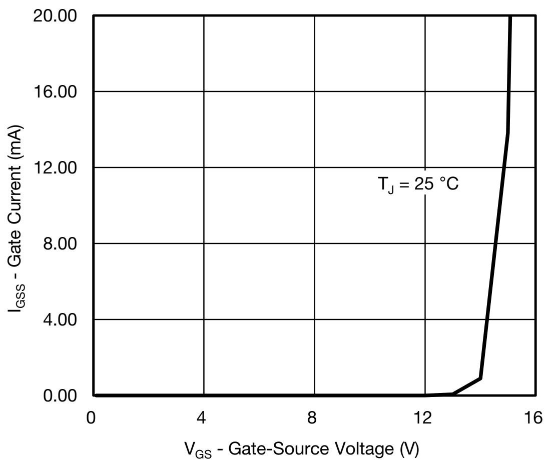
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 µA	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = - 250 µA		- 11		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			2.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 µA	- 0.4		- 1	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 2	µA
		V_{DS} = 0 V, V_{GS} = ± 4.5 V			± 0.2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 20 V, V_{GS} = 0 V			- 1	
		V_{DS} = - 20 V, V_{GS} = 0 V, T_J = 55 °C			- 10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 10			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 10 A		0.0081	0.0096	Ω
		V_{GS} = - 2.5 V, I_D = - 5 A		0.0110	0.0132	
		V_{GS} = - 1.8 V, I_D = - 2 A		0.0170	0.0220	
Forward Transconductance[a]	g_{fs}	V_{GS} = - 10 V, I_D = - 10 A		47		S
Dynamic[b]						
Input Capacitance	C_{iss}	V_{DS} = - 10 V, V_{GS} = 0 V, f = 1 MHz		4300		pF
Output Capacitance	C_{oss}			445		
Reverse Transfer Capacitance	C_{rss}			400		
Total Gate Charge	Q_g	V_{DS} = - 10 V, V_{GS} = - 8 V, I_D = - 14 A		80	120	nC
		V_{DS} = - 10 V, V_{GS} = - 4.5 V, I_D = - 14 A		43	65	
Gate-Source Charge	Q_{gs}			7		
Gate-Drain Charge	Q_{gd}			11.4		
Gate Resistance	R_g	f = 1 MHz	0.6	3.3	6.6	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 1 Ω $I_D \cong$ - 10 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		30	60	ns
Rise Time	t_r			45	90	
Turn-Off Delay Time	$t_{d(off)}$			75	150	
Fall Time	t_f			25	50	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 10 V, R_L = 1 Ω $I_D \cong$ - 10 A, V_{GEN} = - 8 V, R_g = 1 Ω		12	25	
Rise Time	t_r			5	10	
Turn-Off Delay Time	$t_{d(off)}$			80	160	
Fall Time	t_f			20	40	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			- 25	A
Pulse Diode Forward Current (t = 100 µs)	I_{SM}				- 70	
Body Diode Voltage	V_{SD}	I_S = - 10 A, V_{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = - 10 A, dI/dt = 100 A/µs, T_J = 25 °C		35	70	ns
Body Diode Reverse Recovery Charge	Q_{rr}			21	40	nC
Reverse Recovery Fall Time	t_a			20		ns
Reverse Recovery Rise Time	t_b			15		

Notes

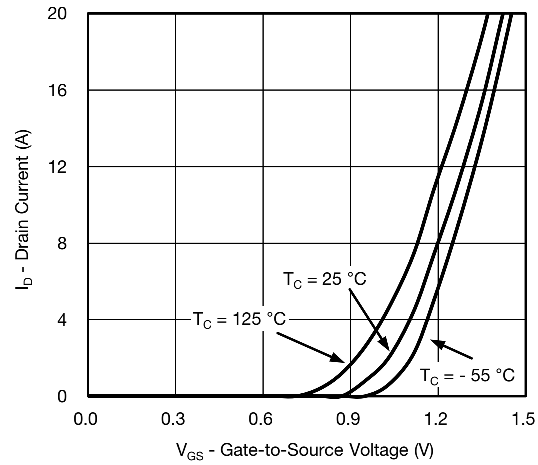
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

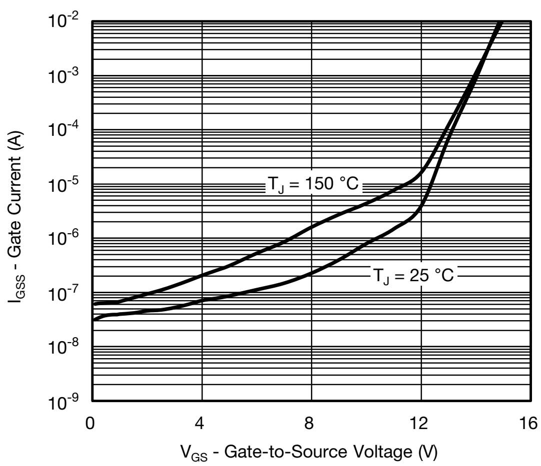
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



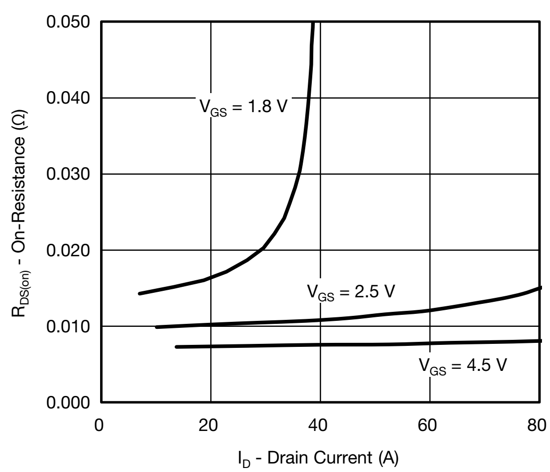
Gate Current vs. Gate-Source Voltage



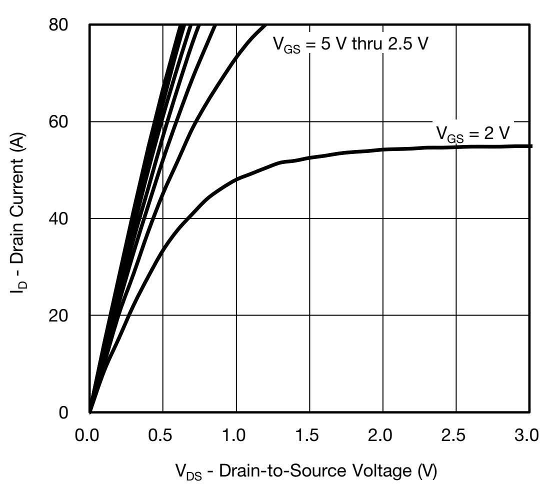
Transfer Characteristics



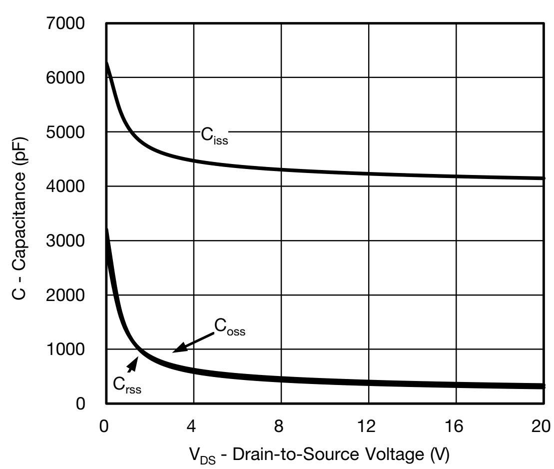
Gate Current vs. Gate-Source Voltage



On-Resistance vs. Drain Current and Gate Voltage

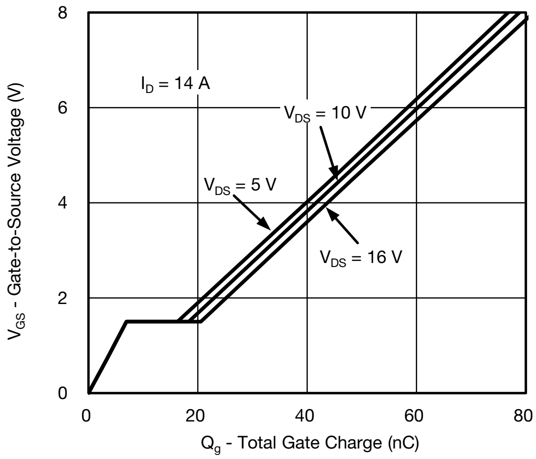


Output Characteristics

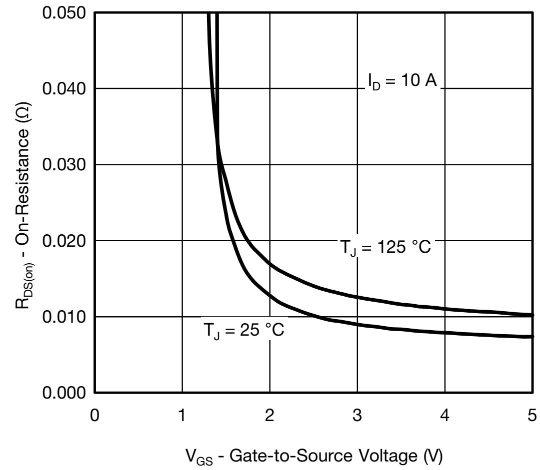


Capacitance

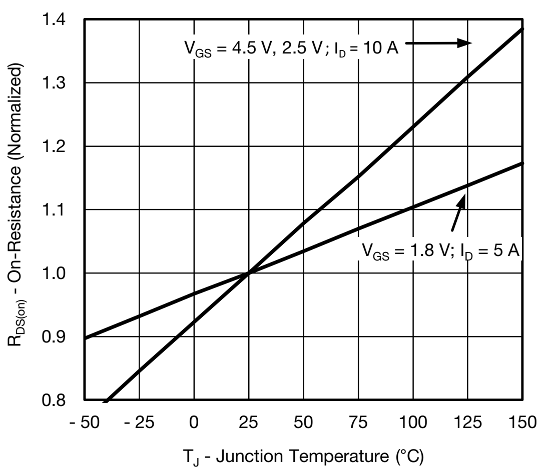
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



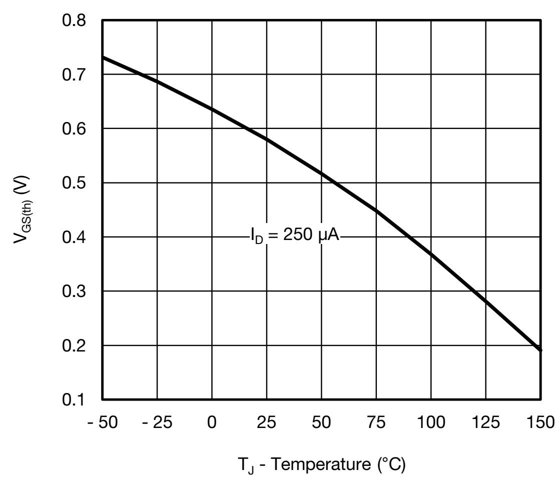
Gate Charge



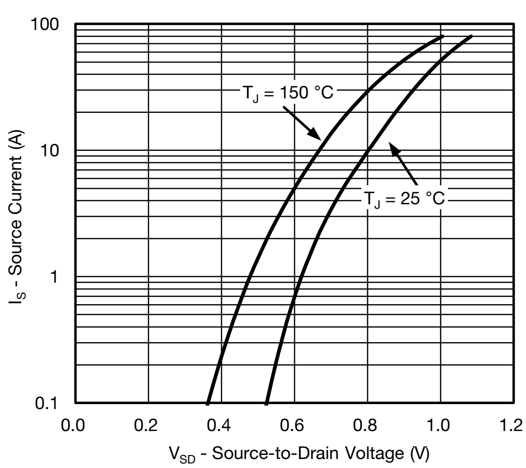
On-Resistance vs. Gate-to-Source Voltage



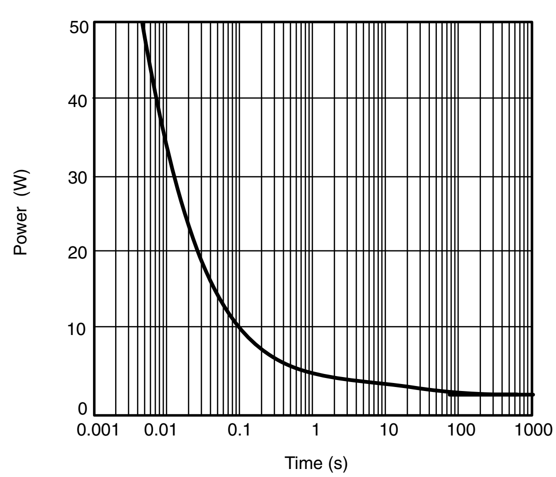
On-Resistance vs. Junction Temperature



Threshold Voltage

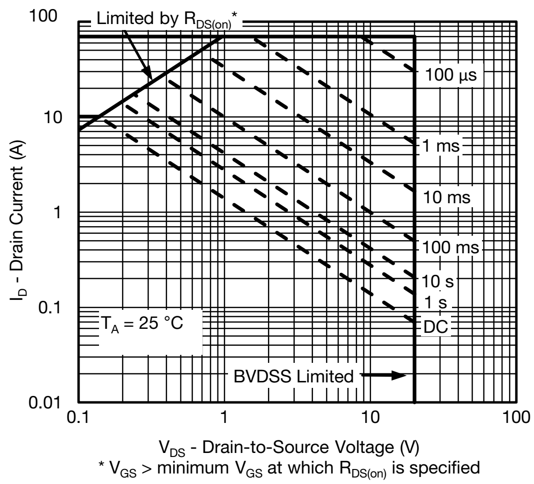


Soure-Drain Diode Forward Voltage

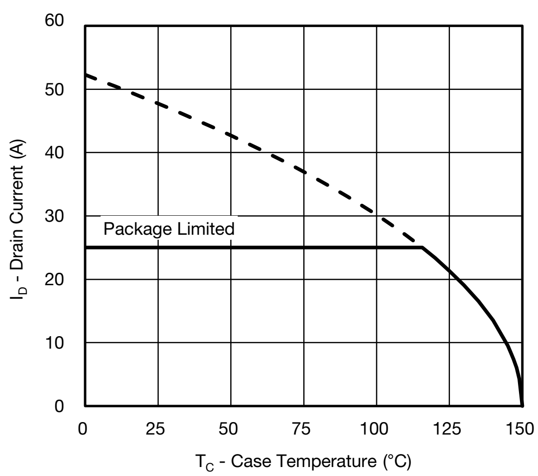


Single Pulse Power, Junction-to-Ambient

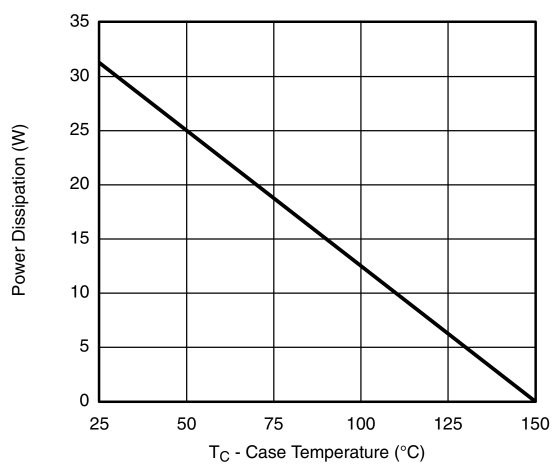
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



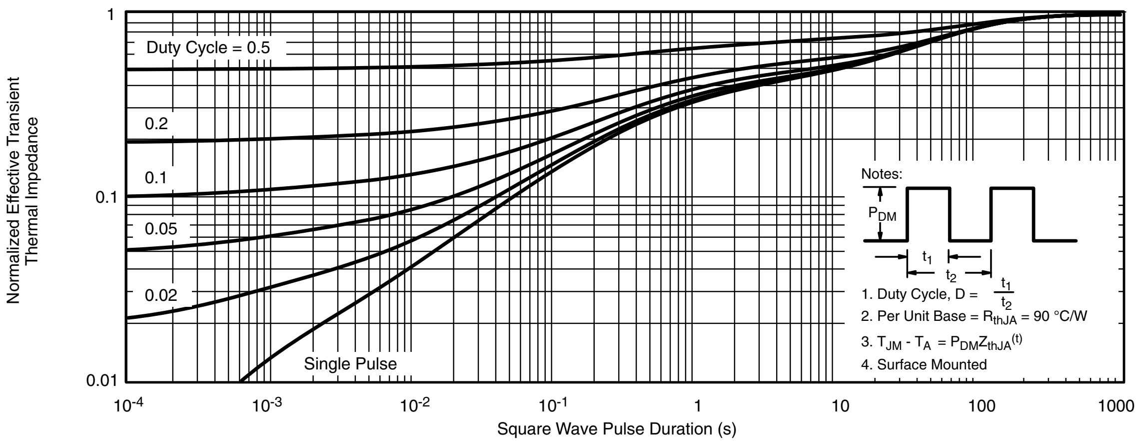
Current Derating*



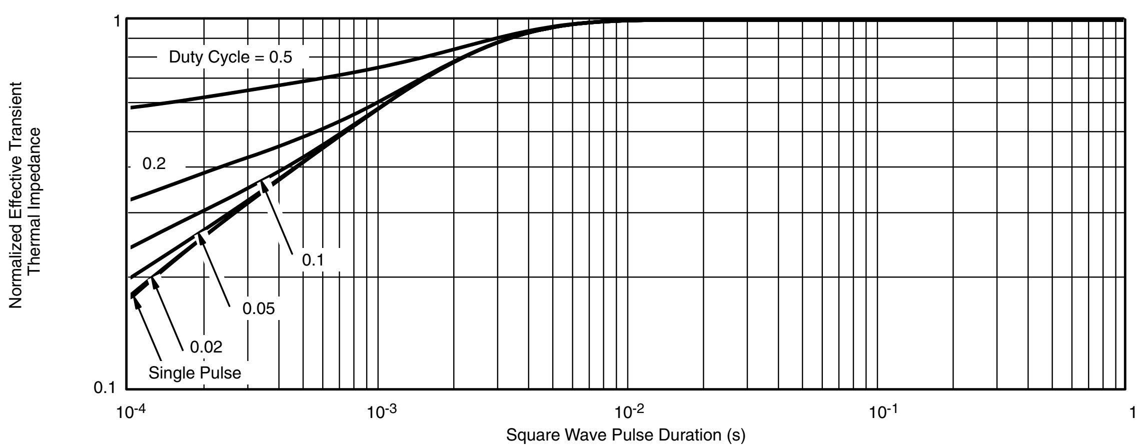
Power Derating

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

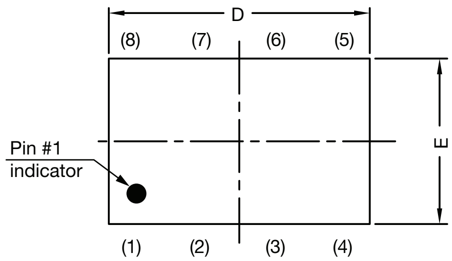


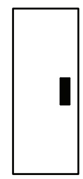
Normalized Thermal Transient Impedance, Junction-to-Ambient



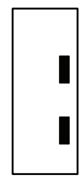
Normalized Thermal Transient Impedance, Junction-to-Case

PowerPAK® ChipFET® Case Outline

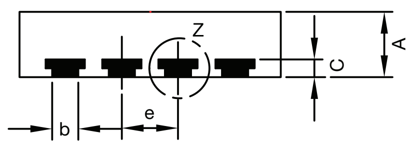


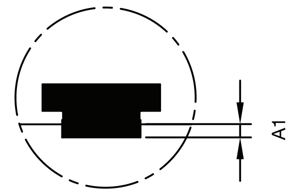


Side view of single

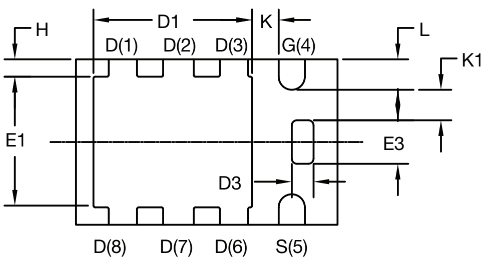


Side view of dual

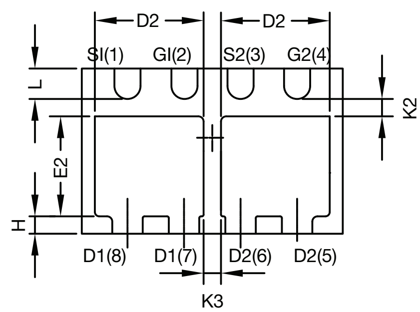




Detail Z



Backside view of single pad



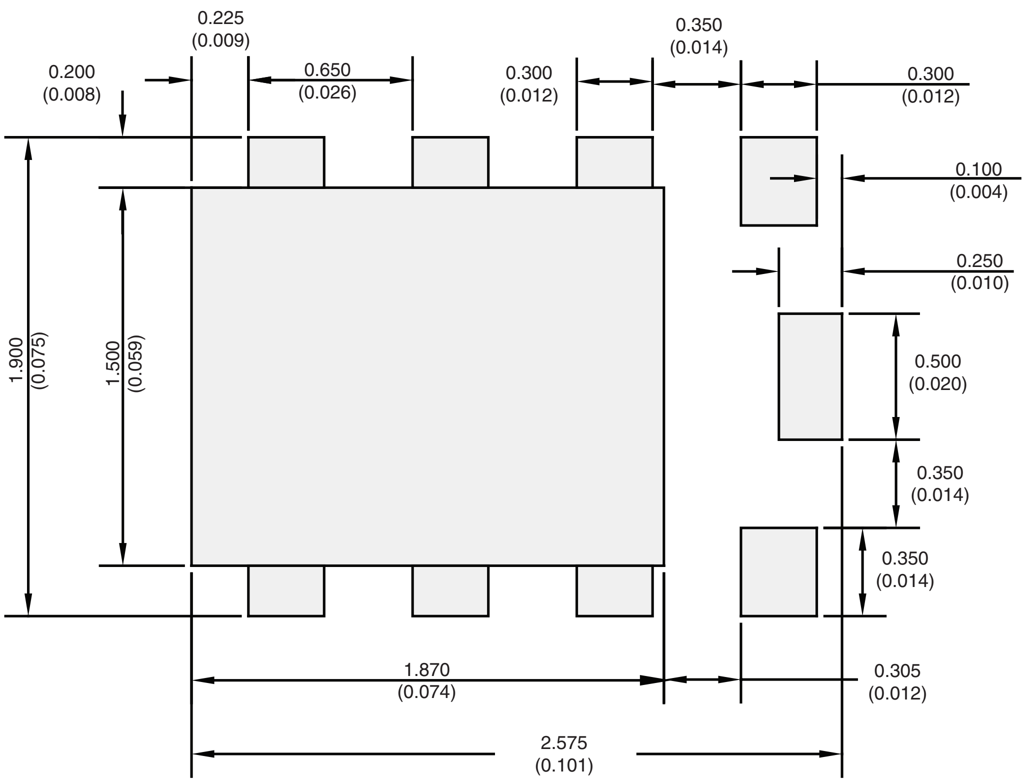
Backside view of dual pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e		0.65 BSC			0.026 BSC	
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0630-Rev. E, 21-Jul-14 DWG: 5940						

Note

- Millimeters will govern

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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APPLICATION NOTE

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