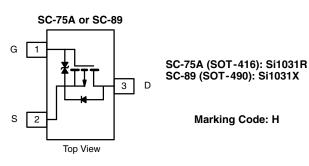


**Vishay Siliconix** 

# P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	<b>R<sub>DS(on)</sub> (</b> Ω <b>)</b>	l <sub>D</sub> (mA)			
- 20	8 at V <sub>GS</sub> = - 4.5 V	- 150			
	12 at V <sub>GS</sub> = - 2.5 V	- 125			
	15 at V <sub>GS</sub> = - 1.8 V	- 100			
	20 at V <sub>GS</sub> = - 1.5 V	- 30			



#### Ordering Information:

Si1031R-T1-GE3 (SC-75A, Lead (Pb)-free and Halogen-free) Si1031X-T1-GE3 (SC-89, Lead (Pb)-free and Halogen-free)

### **FEATURES**

- Halogen-free According to IEC 61249-2-21
  Definition
- High-Side Switching
- Low On-Resistance: 8  $\Omega$
- Low Threshold: 0.9 V (typ.)
- Fast Switching Speed: 45 ns
- TrenchFET<sup>®</sup> Power MOSFETs: 1.5 V Rated
- ESD Protected: 2000 V
- Compliant to RoHS Directive 2002/95/EC

#### **APPLICATIONS**

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

#### BENEFITS

- Ease in Driving Switches
- · Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

			Si1031R		Si1031X		
Parameter		Symbol	5 s	Steady State	5 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	- 20				v
Gate-Source Voltage		V <sub>GS</sub>	± 6				
	T <sub>A</sub> = 25 °C	L	- 150	- 140	- 165	- 155	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 85 °C	D	- 110	- 100	- 150	- 125	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	- 500 - 600		600	mA	
Continuous Source Current (Diode Conduction) <sup>a</sup>		۱ <sub>S</sub>	- 250	- 200	- 340	- 240	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	280	250	340	300	mW
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 85 °C		145	130	170	150	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150				°C
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000				V

Notes:

a. Surface mounted on FR4 board.

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Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = -250 \ \mu A$	- 0.40		- 1.2	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 2.8 V$		± 0.5	± 1.0	± 1.0 ± 2.0 μA	
		$V_{DS} = 0 V, V_{GS} = \pm 4.5 V$		± 1.0	± 2.0		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 16 V, V <sub>GS</sub> = 0 V		- 1	- 500	nA	
		$V_{DS} = -16 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 85 ^{\circ}\text{C}$			- 10	μA	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 V, V_{GS} = -4.5 V$	- 200			mA	
	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 150 mA			8		
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 125 mA		12	0		
Drain-Source On-State Resistance <sup>a</sup>		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 100 mA			15	Ω	
		V <sub>GS</sub> = - 1.5 V, I <sub>D</sub> = - 30 mA			20		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = - 10 V, I <sub>D</sub> = 150 mA		0.4		S	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = - 150 mA, V <sub>GS</sub> = 0 V			- 1.2	V	
Dynamic <sup>b</sup>	•	· · ·					
Total Gate Charge	Qg			1500			
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = - 10 V, $V_{GS}$ = - 4.5 V, $I_{D}$ = - 150 mA		150		рС	
Gate-Drain Charge	Q <sub>gd</sub>			450			
Turn-On Delay Time	t <sub>d(on)</sub>				55	-	
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 65 $\Omega$			30		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_{D}\cong$ - 150 mA, $V_{GEN}$ = - 4.5 V, $R_{g}$ = 10 $\Omega$			60	ns	
Fall Time	t <sub>f</sub>	1			30	]	

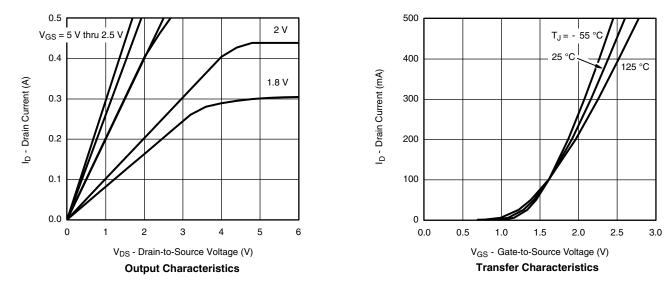
Notes:

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

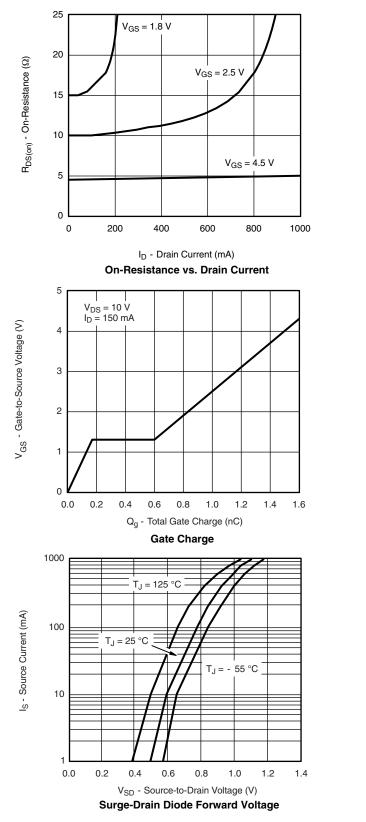
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

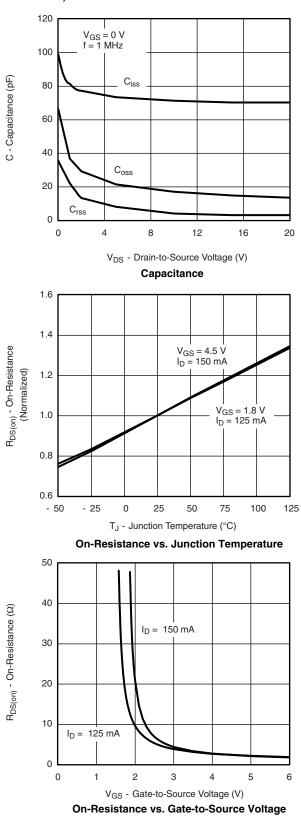






### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)

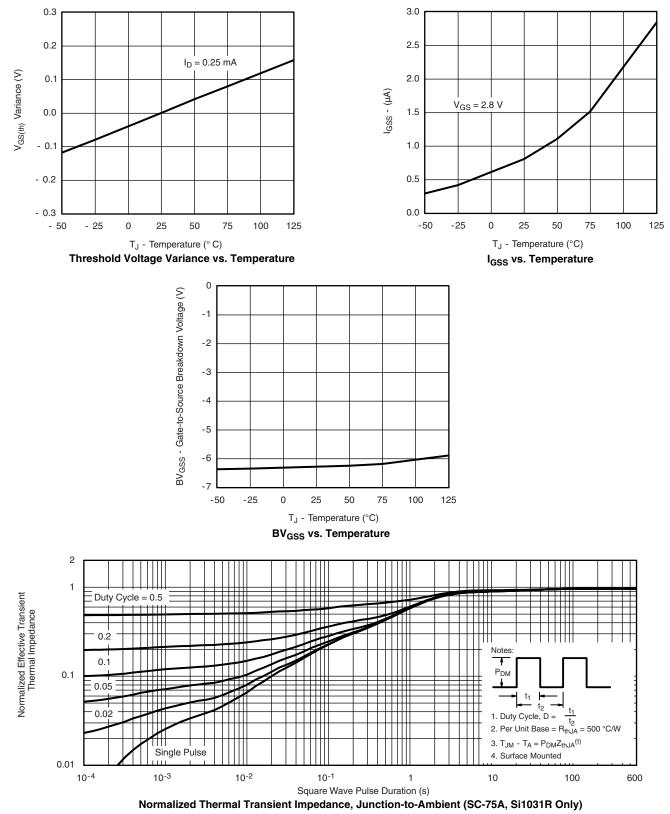




# Si1031R/X

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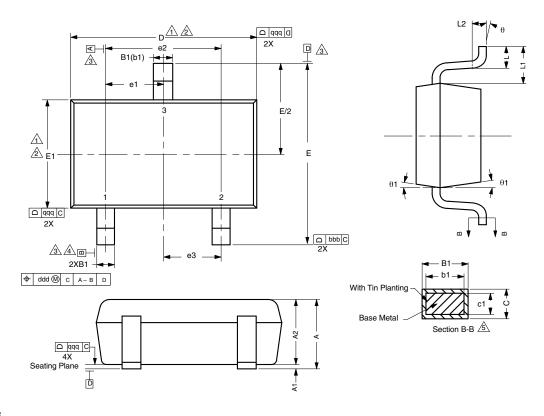
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### SC-75A: 3 Leads



#### DWG: 5868

#### Notes

Dimensions in millimeters will govern.

- ⚠Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.
- 2 Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
- A Datums A, B and D to be determined 0.10 mm from the lead tip.

A Terminal positions are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES		
aaa	0.10		
bbb	0.10		
ссс	0.10		
ddd	0.10		

DIM.	P	NOTE		
Divi.	MIN.	NOM.	MAX.	NOTE
А	-	-	0.80	
A1	0.00	-	0.10	
A2	0.65	0.70	0.80	
B1	0.19	-	0.24	5
b1	0.17	-	0.21	
с	0.13	-	0.15	5
c1	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
E	1.50	1.60	1.70	
E1	0.66	0.76	0.86	1, 2
e1	0.50 BSC			
e2				
e3				
L	0.15	0.205	0.30	
L1				
L2				
q	0°	-	8°	
q1	4°	-	10°	

C15-1445-Rev. F, 23-Nov-15

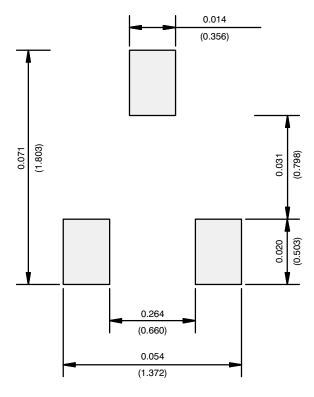
1



# Application Note 826

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### **RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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