



Dual P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)		
- 20	0.756 at $V_{GS} = -4.5 \text{ V}$	- 0.35			
	1.038 at V _{GS} = - 2.5 V	- 0.35	1 nC		
	1.44 at V _{GS} = - 1.8 V	- 0.1	TITC		
	2.4 at V _{GS} = - 1.5 V	- 0.05			

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- Typical ESD protection: 1000 V (HBM)
- Fast Switching Speed
- Compliant to RoHS Directive 2002/95/EC

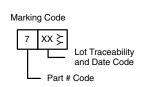
HALOGEN

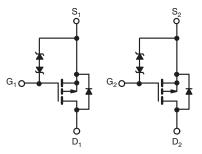
FREE

APPLICATIONS

- Load and Small Signal Switch for Portable Devices
- Drivers: Relays, Solenoids, Displays, Lamps
- **Battery Operated Systems**
- Smart Phones, Tablet PCs

SC-89 (6-LEADS) D_1 5 G_2 D_2 3 Top View





Ordering Information: Si1023CX-T1-GE3 (Lead (Pb)-free and Halogen-free)

Dual P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	- 20	.,		
Gate-Source Voltage		V _{GS}	± 8	V		
Continuous Proin Current /T = 150 °C\	T _A = 25 °C		- 0.45 ^{b, c}			
Continuous Drain Current (T _J = 150 °C)	T _A = 70 °C	l _D	- 0.36 ^{b, c}	٨		
Pulsed Drain Current (t = 300 μs)		I _{DM}	- 1.5	A		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S - 0.18 ^{b, c}				
Marian In David Discipation	T _A = 25 °C	В	0.22 ^{b, c}	W		
Maximum Power Dissipation	T _A = 70 °C	P _D	0.14 ^{b, c}			
Operating Junction and Storage Temperature Ra	ange	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
	t ≤ 5 s	R _{thJA}	470	565	°C/W	
Maximum Junction-to-Ambient ^{a, b}	Steady State State		560	675		

Notes:

- a. Maximum under steady state conditions is 675 $^{\circ}\text{C/W}.$
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.

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Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	J 050 v.A		- 12		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		1.8			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu A$	- 0.4		- 1	V	
Oaks Oassac Lanks as	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 30		
Gate-Source Leakage		$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$			± 1	1 .	
Zana Oata Walkana Busin Oamant	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μΑ	
Zero Gate Voltage Drain Current		$V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			- 10	1	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = \ge 5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 1.5			Α	
		V _{GS} = - 4.5 V, I _D = - 0.35 A		0.630	0.756	Ω	
	Б	V _{GS} = - 2.5 V, I _D = - 0.35 A		0.865	1.038		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 1.8 V, I _D = - 0.1 A		1.20	1.44		
		V _{GS} = - 1.5 V, I _D = - 0.05 A		1.6	2.4		
Forward Transconductance	9 _{fs}	V _{DS} = - 10 V, I _D = - 0.4 A		1		S	
Dynamic ^b				•	1		
Input Capacitance	C _{iss}			45		pF	
Output Capacitance	C _{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		15			
Reverse Transfer Capacitance	C _{rss}			10			
Total Cata Charge		$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -0.4 \text{ A}$		1.65	2.50		
Total Gate Charge	yg	Q _g		1	2	1	
Gate-Source Charge	Q_{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -2.5 \text{ V}, I_{D} = -0.4 \text{ A}$		0.2		nC	
Gate-Drain Charge	Q_{gd}			0.26			
Gate Resistance	R_g	f = 1 MHz	2.4	12	24	Ω	
Turn-On Delay Time	t _{d(on)}			9	18		
Rise Time	t _r	V_{DD} = - 10 V, R_L = 33.3 Ω		10	20	ns	
Turn-Off DelayTime	t _{d(off)}	$I_D\cong$ - 0.3 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		10	20		
Fall Time	t _f			8	16		
Turn-On Delay Time	t _{d(on)}			1	2		
Rise Time	t _r	V_{DD} = - 10 V, R_L = 33.3 Ω		8	16		
Turn-Off DelayTime	t _{d(off)}	$I_D\cong$ - 0.3 A, V_{GEN} = - 8 V, R_g = 1 Ω		9	18		
Fall Time	t _f	<u>1</u>		5	10		
Drain-Source Body Diode Characteris	tics						
Pulse Diode Forward Current ^a	I _{SM}				- 1.5	Α	
Body Diode Voltage	V_{SD}	I _S = - 0.3 A		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			16	24	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = - 0.3 A, dl/dt = 100 A/μs		8	16	nC	
Reverse Recovery Fall Time	ta	$_{\text{IF}} = -0.3 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{S}$		11			
Reverse Recovery Rise Time	t _b			5		ns	

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

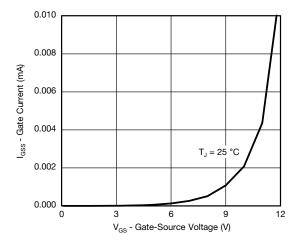
a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

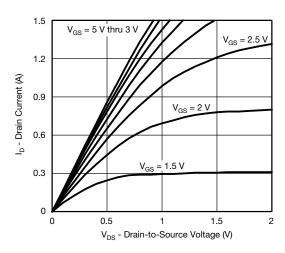




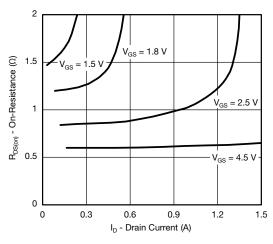
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



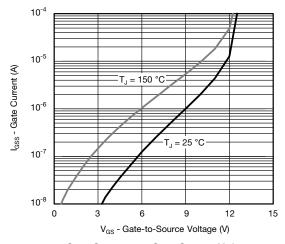
Gate Current vs. Gate-Source Voltage



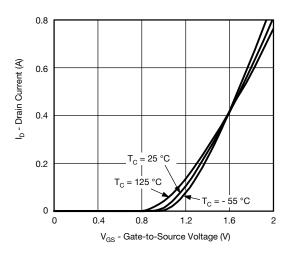
Output Characteristics



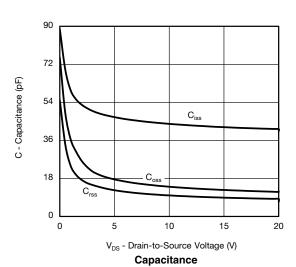
On-Resistance vs. Drain Current



Gate Current vs. Gate-Source Voltage

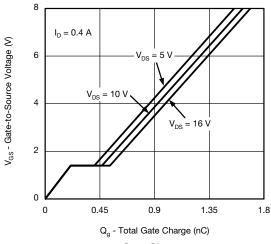


Transfer Characteristics

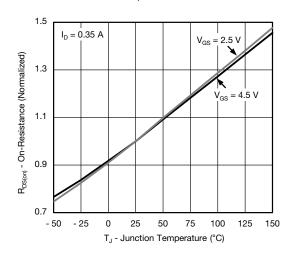


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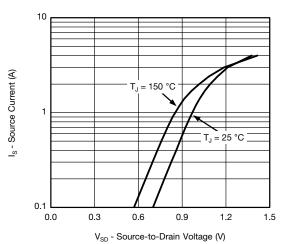
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



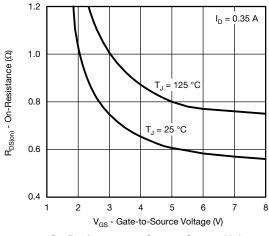
Gate Charge



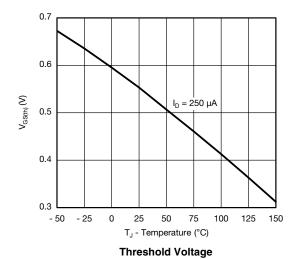
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



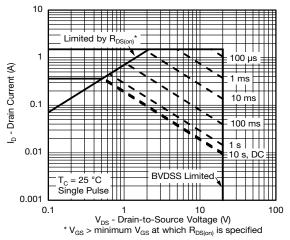
2.25 1.8 Power (W) 1.35 0.9 0.45 0 0.01 0.1 1 10 Time (s)

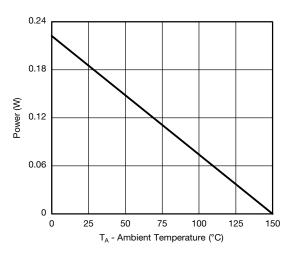
Single Pulse Power, Junction-to-Ambient

2.7



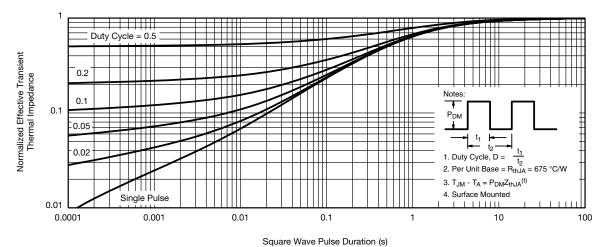
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Safe Operating Area, Junction-to-Ambient

Power Derating, Junction-to-Ambient

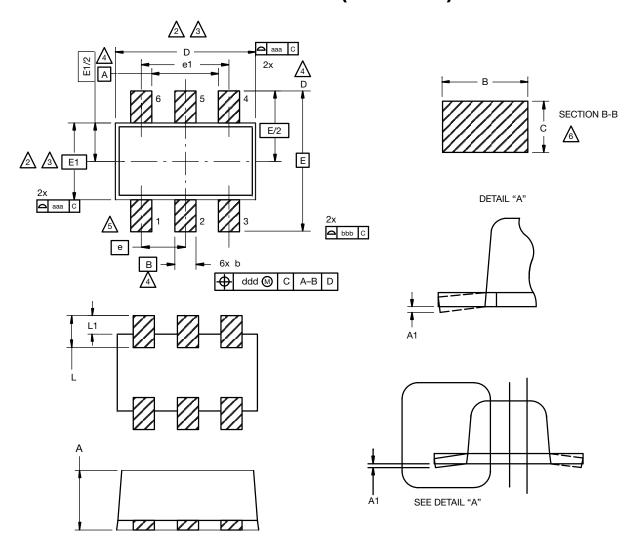


Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63303.



SC-89 6-Leads (SOT-563F)



Notes

1. Dimensions in millimeters.

Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.

Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.

ADatums A, B and D to be determined 0.10 mm from the lead tip.

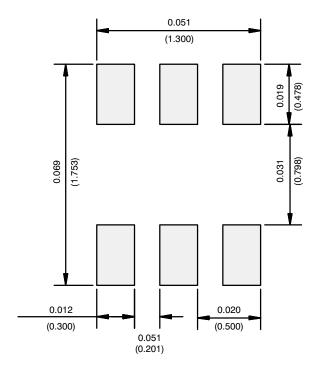
A Terminal numbers are shown for reference only.

These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS					
	MIN.	NOM.	MAX.			
Α	0.56	0.58	0.60			
A1	0	0.02	0.10			
b	0.15	0.22	0.30			
С	0.10	0.14	0.18			
D	1.50	1.60	1.70			
E	1.50	1.60	1.70			
E1	1.15	1.20	1.25			
е	0.45	0.50	0.55			
e1	0.95	1.00	1.05			
L	0.25	0.35	0.50			
L1	0.10	0.20	0.30			
C14-0439-Rev. C, 11-Aug-14 DWG: 5880						



RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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