



N-Channel 20-V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
20	0.0053 @ V _{GS} = 10 V	21.1	14
	0.0078 @ V _{GS} = 4.5 V	17.4	

FEATURES

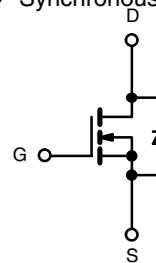
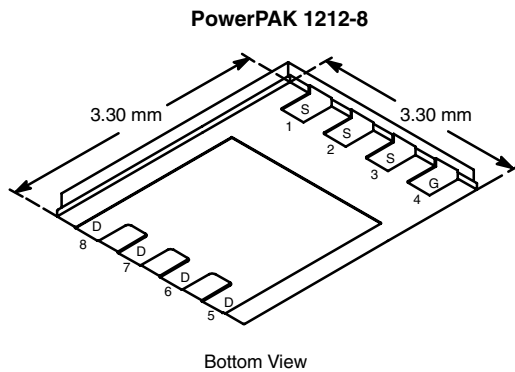
- TrenchFET® Gen II Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized
- 100% R_g Tested



RoHS
COMPLIANT

APPLICATIONS

- Synchronous Rectification
- Synchronous Buck



N-Channel MOSFET

Ordering Information: Si7110DN-T1—E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	20		V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current (T _J = 150°C) ^a	I _D	T _A = 25°C	21.1	13.5	A
		T _A = 70°C	16.9	10.8	
Pulsed Drain Current	I _{DM}	60			
Continuous Source Current (Diode Conduction) ^a	I _S	3.2	1.3		
Single Avalanche Current	L = 0.1 mH	35		A	
Single Avalanche Energy		E _{AS}	61		mJ
Maximum Power Dissipation ^a	P _D	T _A = 25°C	3.8	1.5	W
		T _A = 70°C	2.0	0.8	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b,c}		260			

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	24	33	°C/W
		Steady State	65	81	
Maximum Junction-to-Case (Drain)	R _{thJC}	1.9	2.4		

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

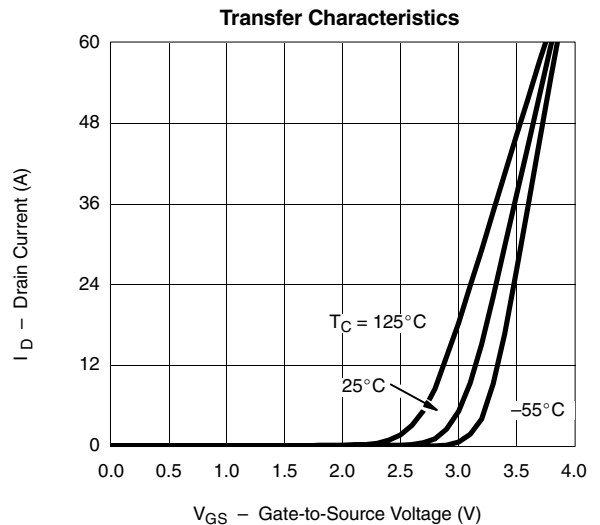
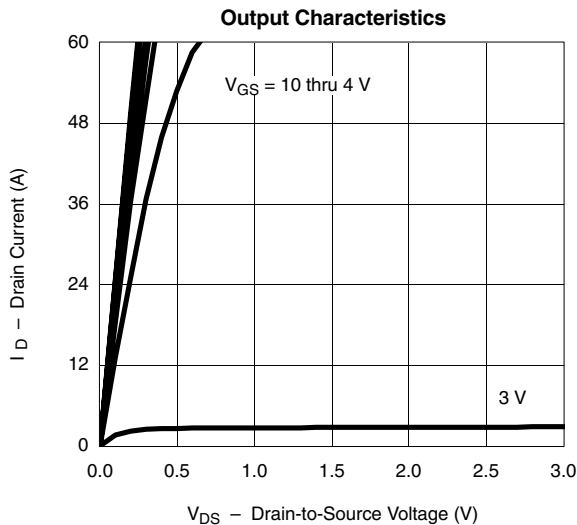
MOSFET SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5		2.5	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C			5	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	40			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 21.1 A		0.0044	0.0053	Ω
		V _{GS} = 4.5 V, I _D = 17.4 A		0.0064	0.0078	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 21.1 A		71		S
Diode Forward Voltage ^a	V _{SD}	I _S = 3.2 A, V _{GS} = 0 V		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 21.1 A		14	21	nC
Gate-Source Charge	Q _{gs}			7		
Gate-Drain Charge	Q _{gd}			4.5		
Gate-Resistance	R _g	f = 1 MHz	0.7	1.4	2.1	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 10 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω		12	20	ns
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			36	55	
Fall Time	t _f			10	15	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 3.2 A, di/dt = 100 A/μs		30	60	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

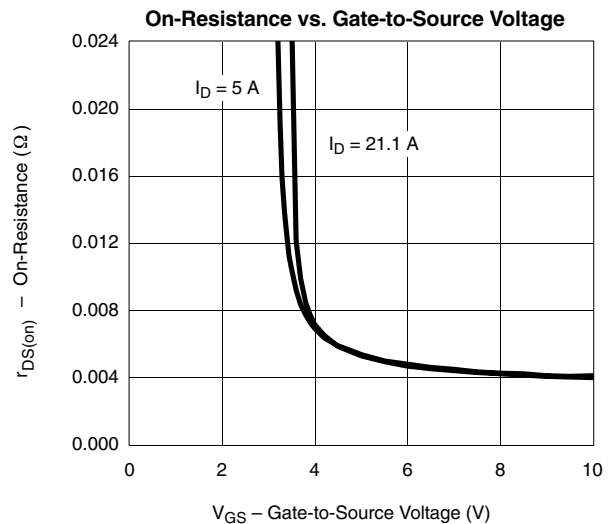
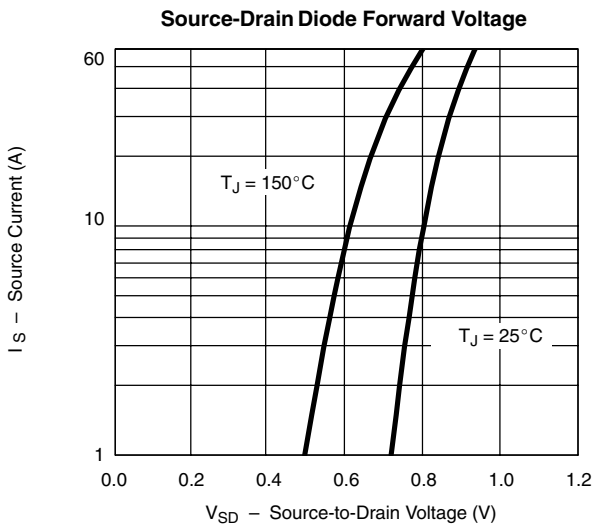
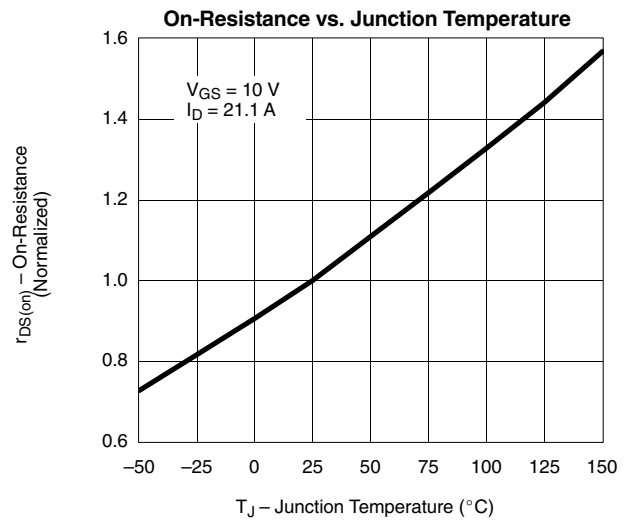
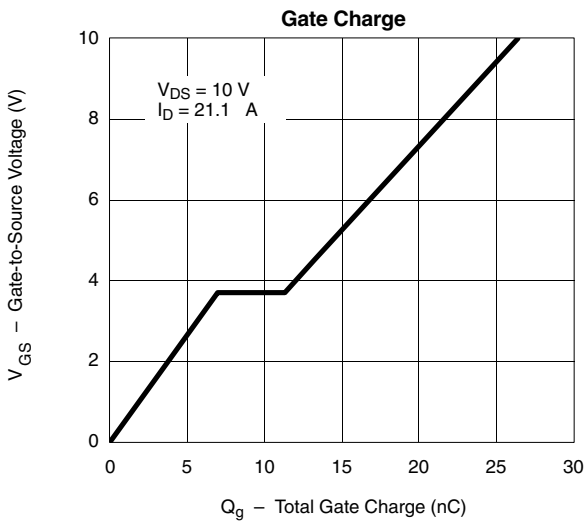
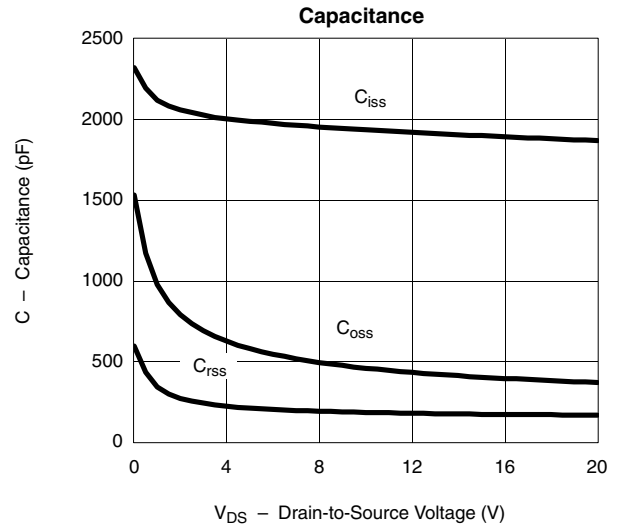
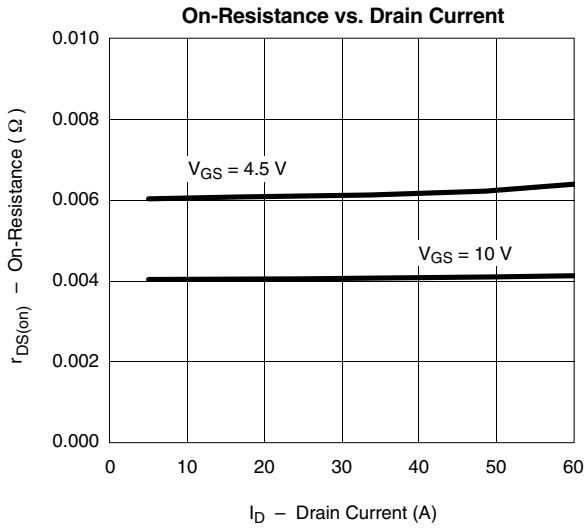
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

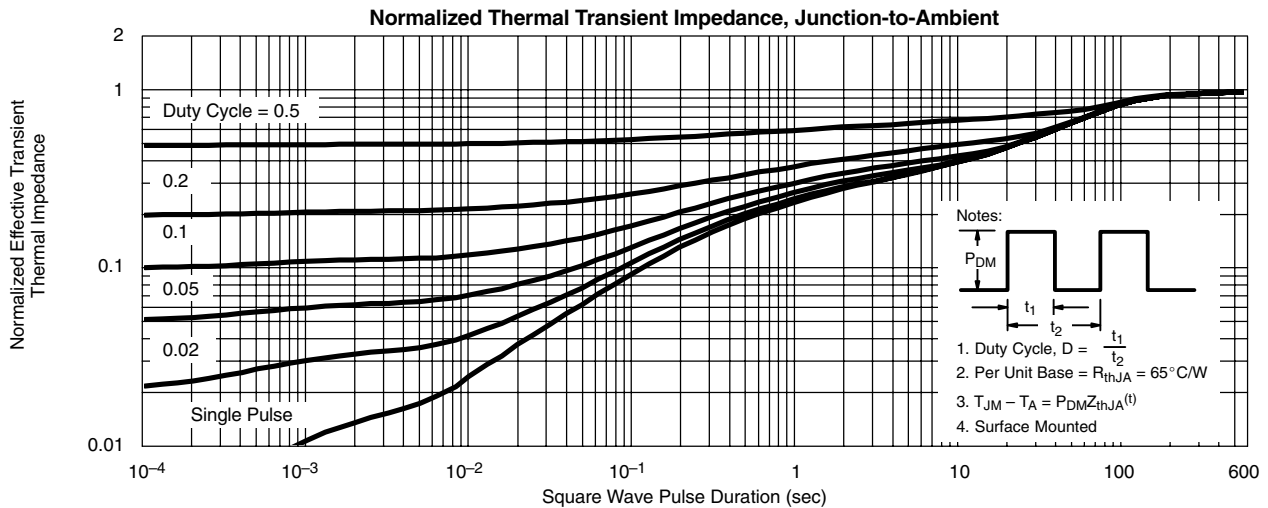
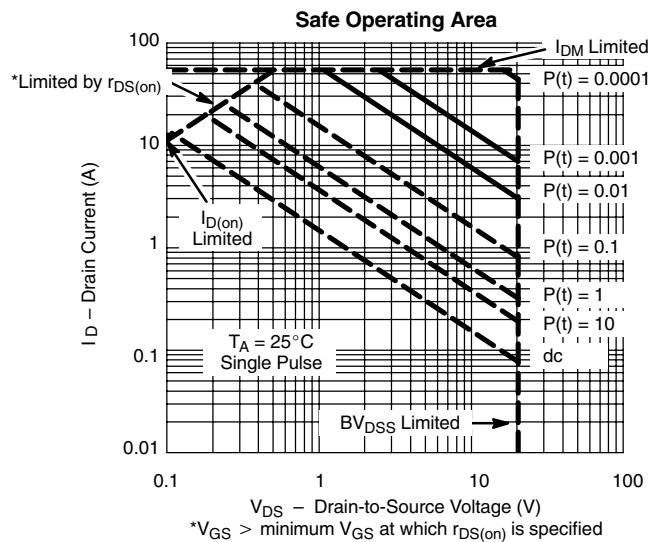
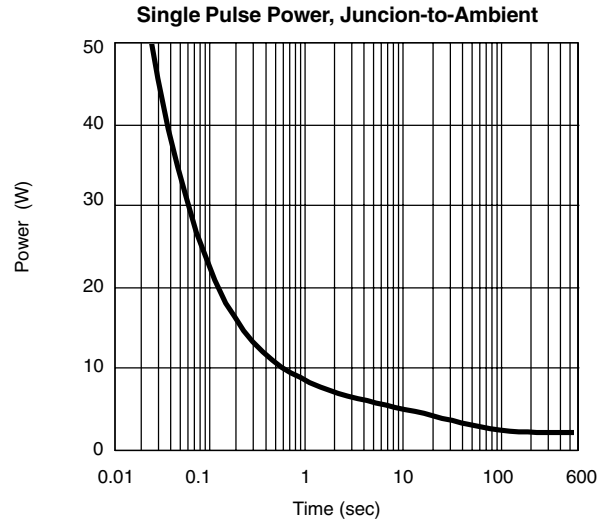
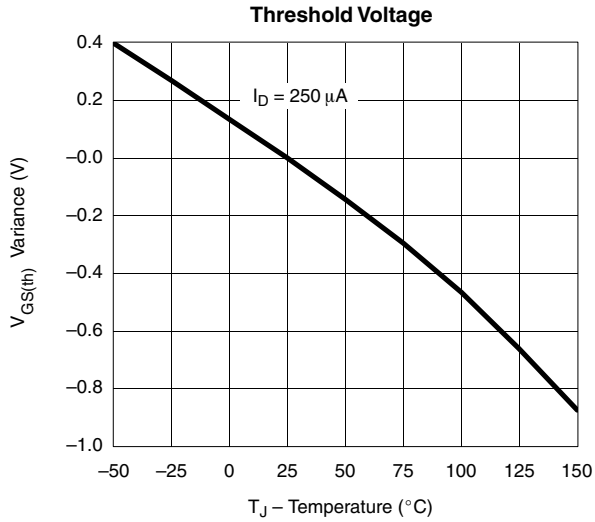




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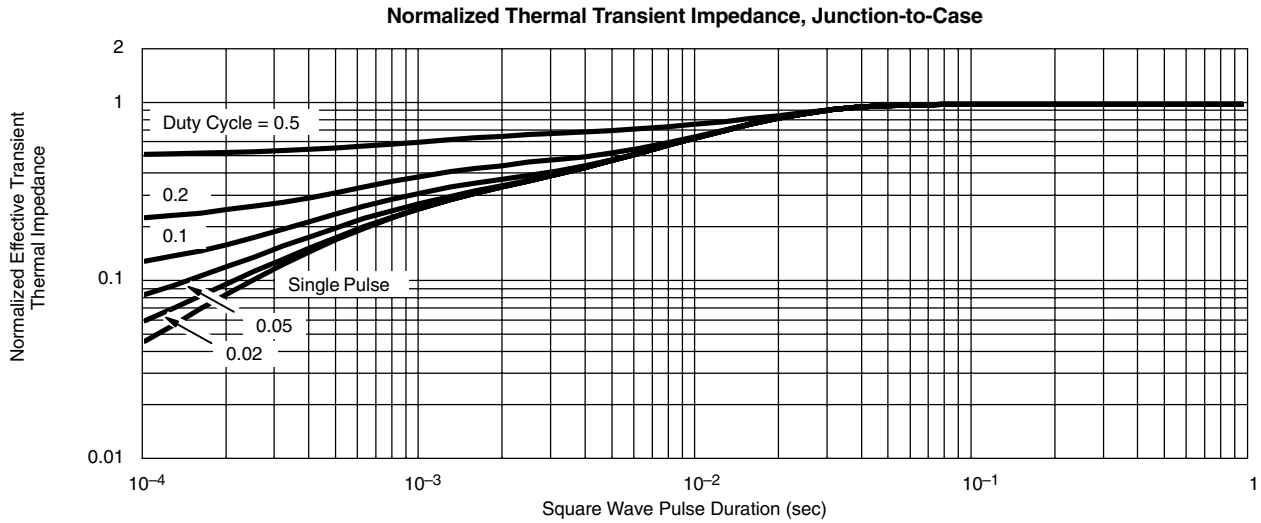


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TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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