

**Vishay Siliconix** 

### N-Channel 75-V (D-S) MOSFET

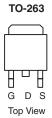
PRODUCT SUMMARY			
V <sub>(BR)DSS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ)
75	0.0062 at $V_{GS}$ = 10 V	90 <sup>d</sup>	75

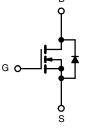
#### **FEATURES**

- TrenchFET<sup>®</sup> Power MOSFETS
- 175 °C Junction Temperature
- 100 % R<sub>q</sub> and UIS Tested

#### **APPLICATIONS**

- Power Supply - Secondary Synchronous Rectification
- Industrial





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Ordering Information: SUM90N08-6m2P-E3 (Lead (Pb)-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	$T_{C} = 25 ^{\circ}C$ , unless oth	erwise noted			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V <sub>DS</sub>	75	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current ( $T_J = 175 \ ^{\circ}C$ )	T <sub>C</sub> = 25 °C	L	90 <sup>d</sup>	А	
	T <sub>C</sub> = 70 °C	I <sub>D</sub>	90 <sup>d</sup>		
Pulsed Drain Current		I <sub>DM</sub>	240		
Avalanche Current		I <sub>AS</sub>	50		
Single Avalanche Energy <sup>a</sup>	L = 0.1 mH	E <sub>AS</sub>	125	mJ	
Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	D	272 <sup>b</sup>	w	
	T <sub>A</sub> = 25 °C <sup>c</sup>	– P <sub>D</sub>	3.75		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Junction-to-Ambient (PCB Mount) <sup>c</sup>	R <sub>thJA</sub>	40	°C/W	
Junction-to-Case (Drain)	R <sub>thJC</sub>	0.55		

Notes:

a. Duty cycle  $\leq$  1 %.

b. See SOA curve for voltage derating.

c. When Mounted on 1" square PCB (FR-4 material).

d. Package limited.



## SUM90N08-6m2P

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Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{DS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	75			v
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2.5		4.5	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 250	nA
Zero Gate Voltage Drain Current		$V_{DS} = 75 \text{ V}, V_{GS} = 0 \text{ V}$			1	μΑ
	I <sub>DSS</sub>	$V_{DS}$ = 75 V, $V_{GS}$ = 0 V, $T_{J}$ = 125 °C			50	
		$V_{DS}$ = 75 V, $V_{GS}$ = 0 V, $T_{J}$ = 150 °C			250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 10$ V, $V_{GS} = 10$ V	70			А
Drain-Source On-State Resistance <sup>a</sup>	r	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0051	0.0062	Ω
	<sup>r</sup> DS(on)	$V_{GS}$ = 10 V, $I_D$ = 20 A, $T_J$ = 125 °C		0.0082	0.0105	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		50		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 30 V, f = 1 MHz		4620		pF
Output Capacitance	C <sub>oss</sub>			517		
Reverse Transfer Capacitance	C <sub>rss</sub>			247		
Total Gate Charge <sup>c</sup>	Qg			75	115	nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{DS}$ = 30 V, $V_{GS}$ = 10 V, $I_{D}$ = 50 A		25.5		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			20		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		1.2	2.4	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			16	30	
Rise Time <sup>c</sup>	t <sub>r</sub>	$V_{DD}$ = 30 V, R <sub>L</sub> = 0.6 $\Omega$ I <sub>D</sub> $\cong$ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 $\Omega$		11	20	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			24	40	
Fall Time <sup>c</sup>	t <sub>f</sub>			10	20	
Source-Drain Diode Ratings and Cha	aracteristics T	<sub>C</sub> = 25 °C <sup>b</sup>				
Continuous Current	ا <sub>S</sub>				85	^
Pulsed Current	I <sub>SM</sub>				240	A
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{F} = 20 \text{ A}, \text{ V}_{GS} = 0 \text{ V}$		0.83	1.5	V
Reverse Recovery Time	t <sub>rr</sub>			60	100	ns
Peak Reverse Recovery Current	I <sub>RM(REC)</sub>	I <sub>F</sub> = 75 A, di/dt = 100 A/μs		3.3	5	А
Reverse Recovery Charge	Q <sub>rr</sub>			100	150	nC

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

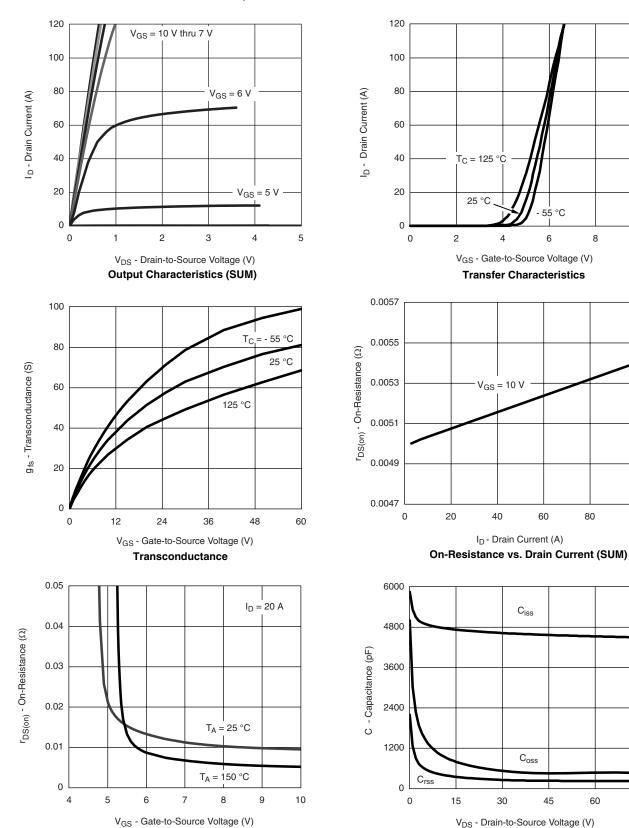
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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100



#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

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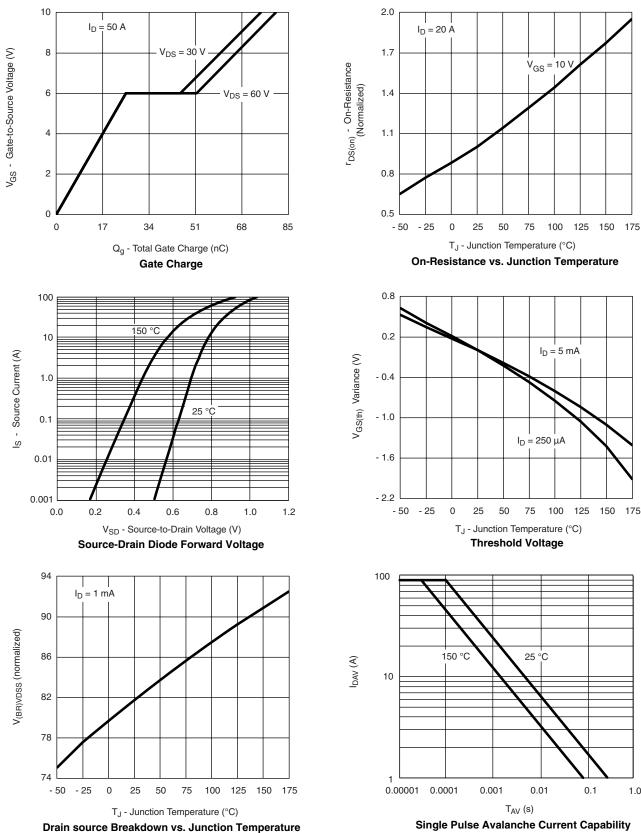
On-Resistance vs. Gate-to-Source Voltage (SUM)

Capacitance

75

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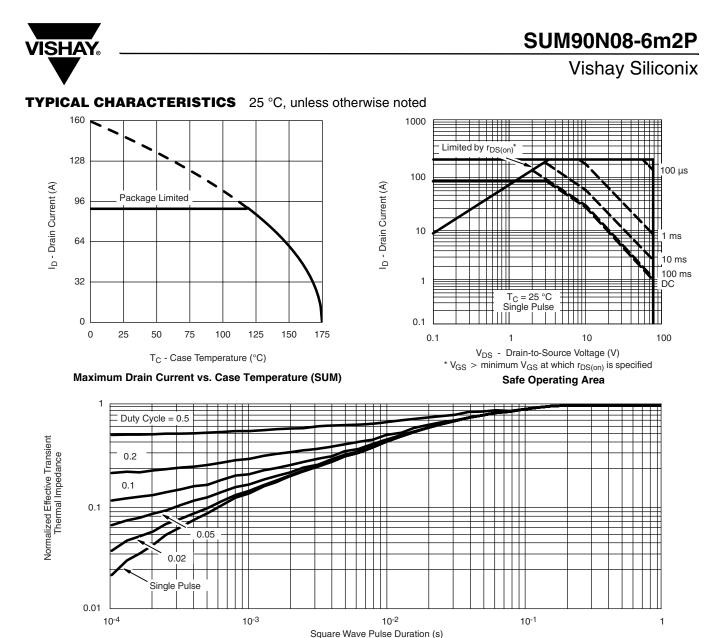
#### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



vs. Time

1.0

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Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?69552.



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