

### STW37N60DM2AG

# Automotive-grade N-channel 600 V, 0.094 $\Omega$ typ., 28 A MDmesh<sup>TM</sup> DM2 Power MOSFET in a TO-247 package

Datasheet - production data

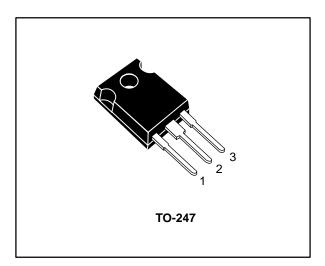
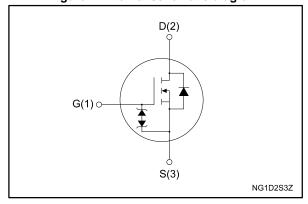


Figure 1: Internal schematic diagram



#### **Features**

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	Ртот
STW37N60DM2AG	600 V	0.110 Ω	28 A	210 W

- Designed for automotive applications and AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### **Applications**

Switching applications

### Description

This high voltage N-channel Power MOSFET is part of the MDmesh  $^{\text{TM}}$  DM2 fast recovery diode series. It offers very low recovery charge (Qrr) and time (trr) combined with low RDS(on), rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

**Table 1: Device summary** 

Order code	Marking	Package	Packing
STW37N60DM2AG	37N60DM2	TO-247	Tube

Contents STW37N60DM2AG

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STW37N60DM2AG Electrical ratings

# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>G</sub> S	Gate-source voltage	±25	V
1-	Drain current (continuous) at T <sub>case</sub> = 25 °C	28	۸
l <sub>D</sub>	Drain current (continuous) at T <sub>case</sub> = 100 °C	17	Α
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	112	А
Ртот	Total dissipation at T <sub>case</sub> = 25 °C	210	W
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	50	V/ns
dv/dt <sup>(3)</sup>	MOSFET dv/dt ruggedness	50	V/IIS
T <sub>stg</sub>	Storage temperature	-55 to 150	
Tj	Operating junction temperature	-55 (0 150	°C

#### Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	0.6	90044
R <sub>thj-amb</sub>	Thermal resistance junction-amb	50	°C/W

**Table 4: Avalanche characteristics** 

Symbol	Parameter	Value	Unit
lar	Avalanche current, repetitive or not repetitive	6	А
E <sub>AS</sub> <sup>(1)</sup>	Single pulse avalanche energy	650	mJ

#### Notes:

 $<sup>^{\</sup>left( 1\right) }$  Pulse width is limited by safe operating area.

 $<sup>^{(2)}</sup>$   $I_{SD} \leq 28$  A, di/dt=800 A/µs;  $V_{DS}$  peak <  $V_{(BR)DSS}, V_{DD}$  = 80%  $V_{(BR)DSS}.$ 

 $<sup>^{(3)}</sup>$  V<sub>DS</sub>  $\leq 480$  V.

 $<sup>^{(1)}</sup>$  starting  $T_j = 25~^{\circ}C,~I_D = I_{AR},~V_{DD} = 50~V.$ 

Electrical characteristics STW37N60DM2AG

### 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
Zara nata waltana dinain		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V			10	
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V, T <sub>case</sub> = 125 °C			100	μΑ
Igss	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±5	μΑ
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	3	4	5	V
R <sub>DS(on)</sub>	Static drain-source on- resistance	V <sub>G</sub> S = 10 V, I <sub>D</sub> = 14 A		0.094	0.11	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub>	Input capacitance		-	2400	ı	
Coss	Output capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz,	-	110	ı	pF
Crss	Reverse transfer capacitance	Ves = 0 V	-	2.8	-	μ.
Coss eq. (1)	Equivalent output capacitance	$V_{DS} = 0$ to 480 V, $V_{GS} = 0$ V	ı	190	ı	pF
$R_{G}$	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	4.3	-	Ω
Qg	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 28 \text{ A},$	-	54	ı	
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 10 V (see Figure 15: "Test circuit for gate charge	-	14.6	-	nC
$Q_{gd}$	Gate-drain charge	behavior")	-	24.2	-	

#### Notes:

**Table 7: Switching times** 

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 14 A	1	21.2	ı	
tr	Rise time	$R_G = 4.7 \Omega$ , $V_{GS} = 10 V$ (see Figure 14: "Test circuit for	ı	17	1	
$t_{d(off)}$	Turn-off delay time	resistive load switching times"	-	68	-	ns
t <sub>f</sub>	Fall time	and Figure 19: "Switching time waveform")	1	10.7	1	

 $<sup>^{(1)}</sup>$  C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current		ı		28	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		1		112	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 28 A	ı		1.6	<b>V</b>
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 28 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	ı	120		ns
Qrr	Reverse recovery charge	V <sub>DD</sub> = 60 V (see Figure 16: "Test circuit for inductive load	-	572		nC
I <sub>RRM</sub>	Reverse recovery current	switching and diode recovery times")	ı	10.2		Α
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 28 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	ı	215		ns
Qrr	Reverse recovery charge	$V_{DD}$ = 60 V, $T_j$ = 150 °C (see Figure 16: "Test circuit for	ı	1.89		μ
I <sub>RRM</sub>	Reverse recovery current	inductive load switching and diode recovery times")	-	17.7		Α

#### Notes:

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)</sub> GSO	Gate-source breakdown voltage	$I_{GS} = \pm 250 \ \mu A, \ I_{D} = 0 \ A$	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

<sup>&</sup>lt;sup>(1)</sup> Pulse width is limited by safe operating area.

 $<sup>^{(2)}</sup>$  Pulse test: pulse duration = 300  $\mu s,$  duty cycle 1.5%.

### 2.1 Electrical characteristics (curves)

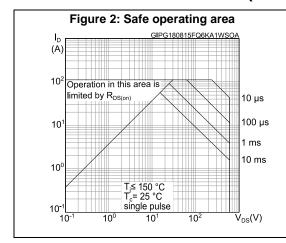
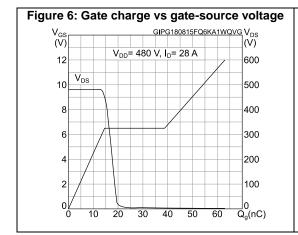
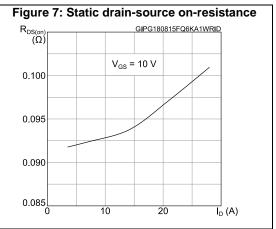


Figure 3: Thermal impedance K  $\delta = 0.5$   $\delta = 0.2$   $\delta = 0.05$   $\delta = 0.01$   $\delta = 0.01$ Single pulse  $\frac{b_1}{T}$   $\frac{b_1}{T}$   $\frac{10.3}{10.5}$   $\frac{10.4}{T}$   $\frac{10.3}{T}$   $\frac{10.3}{T}$   $\frac{10.4}{T}$   $\frac{10.3}{T}$ 





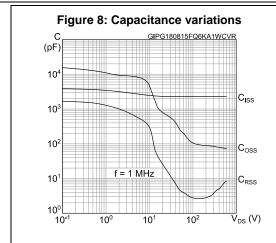


Figure 10: Normalized on-resistance vs temperature

R<sub>DS(on)</sub> GIPG180815FQ6KA1WRON (norm.)

2.2

1.8

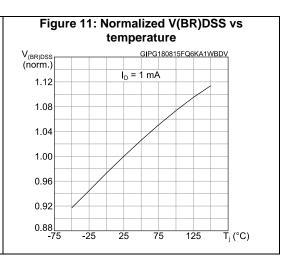
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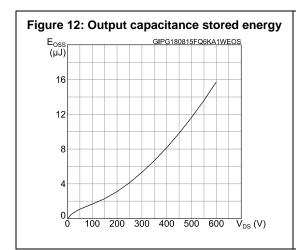
1.0

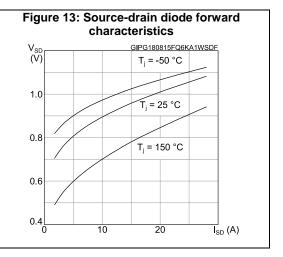
0.6

0.2

-75 -25 25 75 125 T<sub>j</sub> (°C)







Test circuits STW37N60DM2AG

### 3 Test circuits

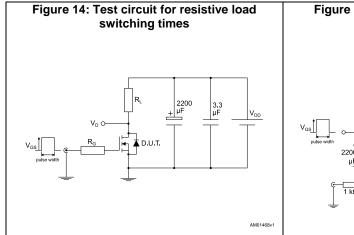


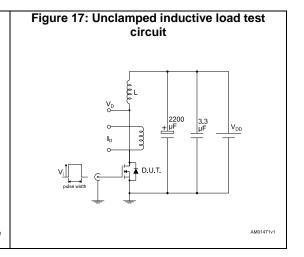
Figure 15: Test circuit for gate charge behavior

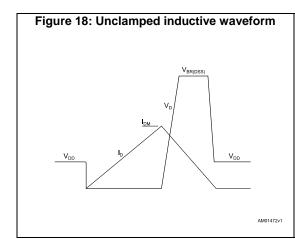
12 V 47 kΩ 100 nF D.U.T.

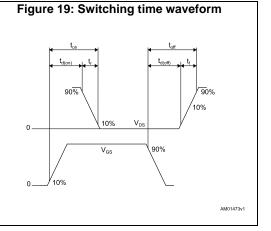
2200 VG

AM01469v1

Figure 16: Test circuit for inductive load switching and diode recovery times







### 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

### 4.1 TO-247 package information

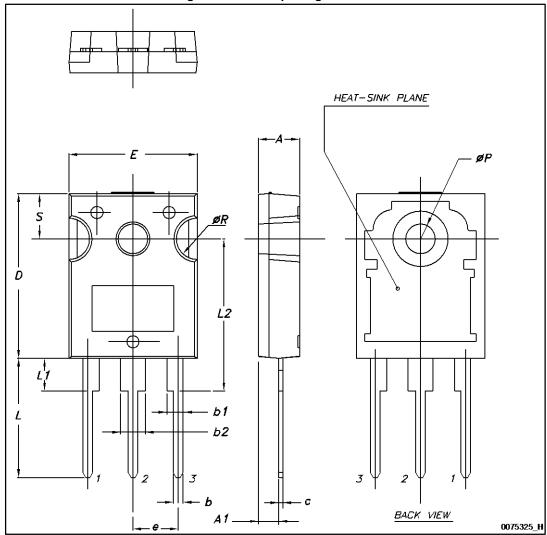


Figure 20: TO-247 package outline

Table 10: TO-247 package mechanical data

Dim	mm.				
Dim.	Min.	Тур.	Max.		
А	4.85		5.15		
A1	2.20		2.60		
b	1.0		1.40		
b1	2.0		2.40		
b2	3.0		3.40		
С	0.40		0.80		
D	19.85		20.15		
Е	15.45		15.75		
е	5.30	5.45	5.60		
L	14.20		14.80		
L1	3.70		4.30		
L2		18.50			
ØP	3.55		3.65		
ØR	4.50		5.50		
S	5.30	5.50	5.70		

STW37N60DM2AG Revision history

# 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
25-Aug-2015	1	Initial version

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