STP7N105K5, STU7N105K5, STW7N105K5

N-channel 1050 V, 1.4 Ω typ., 4 A Zener-protected SuperMESH™ 5 Power MOSFETs in TO-220, IPAK and TO-247 packages

Datasheet — preliminary data

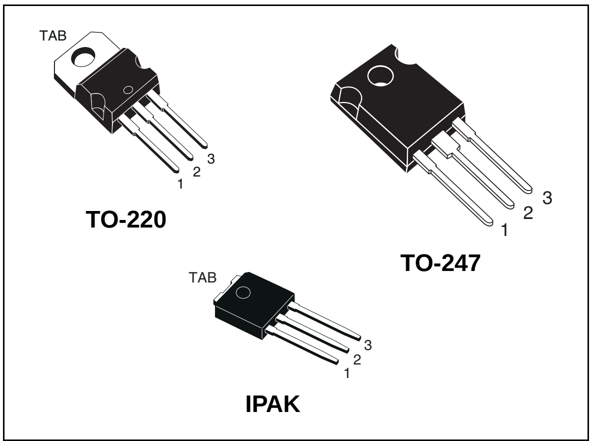
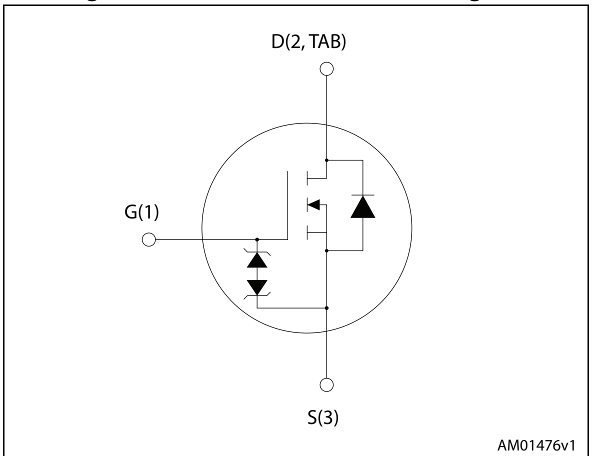


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STP7N105K5	1050 V	2 Ω	4 A	110 W
STU7N105K5				
STW7N105K5				

- IPAK 1050 V worldwide best $R_{DS(on)}$
- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These N-channel Zener-protected Power MOSFETs are designed using ST's revolutionary avalanche-rugged very high voltage SuperMESH™ 5 technology, based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance, and ultra-low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STP7N105K5	7N105K5	TO-220	Tube
STU7N105K5		IPAK	
STW7N105K5		TO-247	

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	4	A
I_D	Drain current (continuous) at T_C = 100 °C	3	A
I_{DM} (1)	Drain current (pulsed)	16	A
P_{TOT}	Total dissipation at T_C = 25 °C	110	W
I_{AR}	Max current during repetitive or single pulse avalanche	1.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	132	mJ
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_j	Operating junction temperature	- 55 to 150	°C
T_{stg}	Storage temperature		

1. Pulse width limited by safe operating area
2. $I_{SD} \leq$ 4 A, di/dt $\leq$ 100 A/μs, $V_{DS(peak)} \leq V_{(BR)DSS}$ $V_{SD} \leq$ 840 V
3. $V_{SD} \leq$ 840 V

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		TO-220	IPAK	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1.14			°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-amb max	62.5	100	50	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage, V_{GS}= 0	I_D = 1 mA	1050			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 1050 V			1	µA
		V_{DS} = 1050 V, Tc=125 °C			50	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 2 A		1.4	2	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	380	-	pF
C_{oss}	Output capacitance		-	40	-	pF
C_{rss}	Reverse transfer capacitance		-	0.65	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 840 V	-	47	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	17	-	pF
R_G	Intrinsic gate resistance	f = 1MHz open drain	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 840 V, I_D = 4 A V_{GS} =10 V *(see Figure 18)*	-	17	-	nC
Q_{gs}	Gate-source charge		-	2.5	-	nC
Q_{gd}	Gate-drain charge		-	12.5	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 525V, I_D = 2 A, R_G=4.7 Ω, V_{GS}=10 V (*see Figure 20*)	-	17.5	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time		-	43	-	ns
t_f	Fall time		-	25	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)		-		4 16	A A
V_{SD}(1)	Forward on voltage	I_{SD}= 4 A, V_{GS}=0	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD}= 4 A, V_{DD}= 60 V di/dt = 100 A/μs, (*see Figure 19*)	-	370		ns
Q_{rr}	Reverse recovery charge		-	3		μC
I_{RRM}	Reverse recovery current		-	16.5		A
t_{rr}	Reverse recovery time	I_{SD}= 4 A,V_{DD}= 60 V di/dt=100 A/μs, Tj=150 °C (*see Figure 19*)	-	600		ns
Q_{rr}	Reverse recovery charge		-	4.4		μC
I_{RRM}	Reverse recovery current		-	14.5		A

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ± 1mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance the device's ESD capability. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220 and TO-247

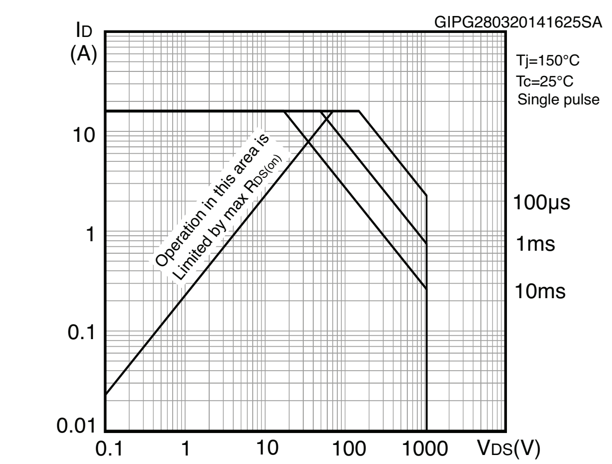


Figure 3. Thermal impedance for TO-220 and TO-247

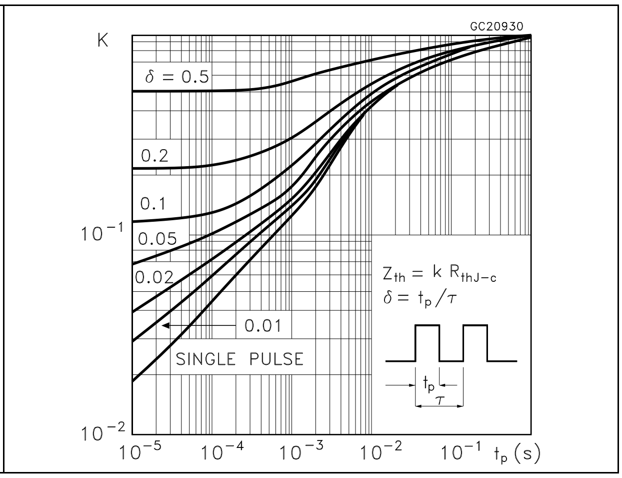


Figure 4. Safe operating area for IPAK

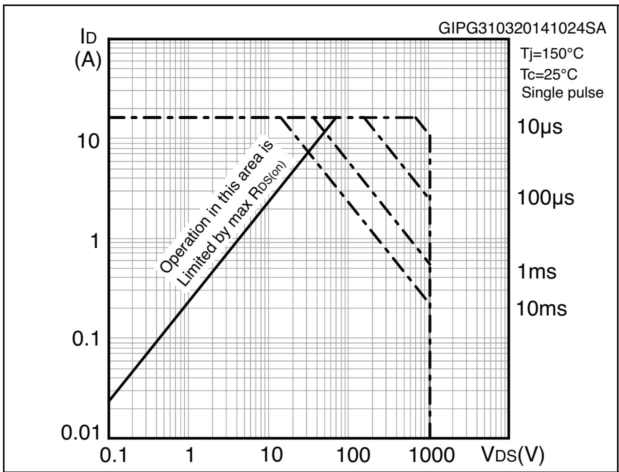


Figure 5. Thermal impedance for IPAK

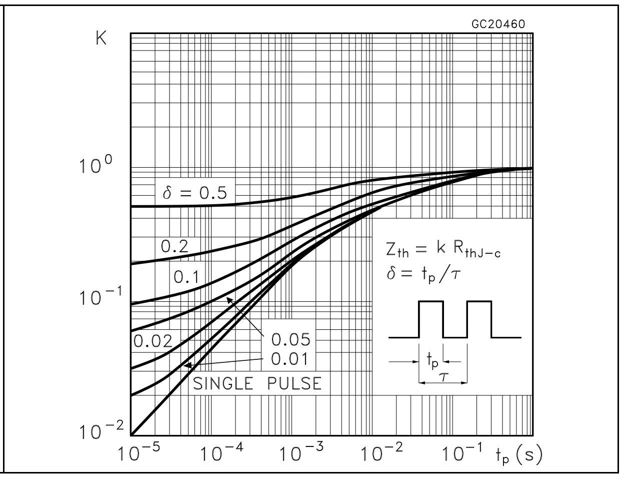


Figure 6. Output characteristics

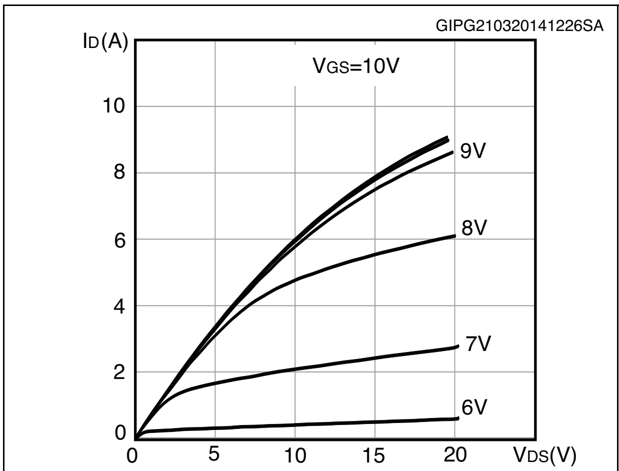


Figure 7. Transfer characteristics

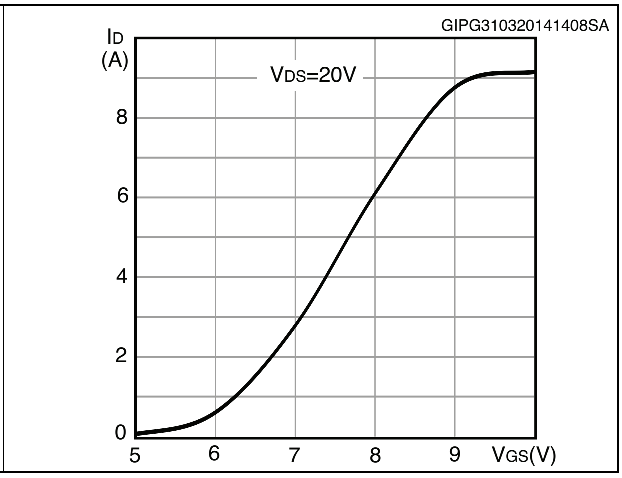


Figure 8. Gate charge vs gate-source voltage

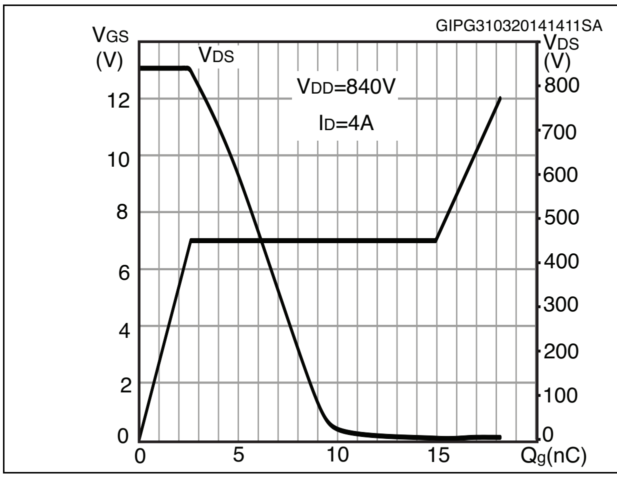


Figure 9. Static drain-source on-resistance

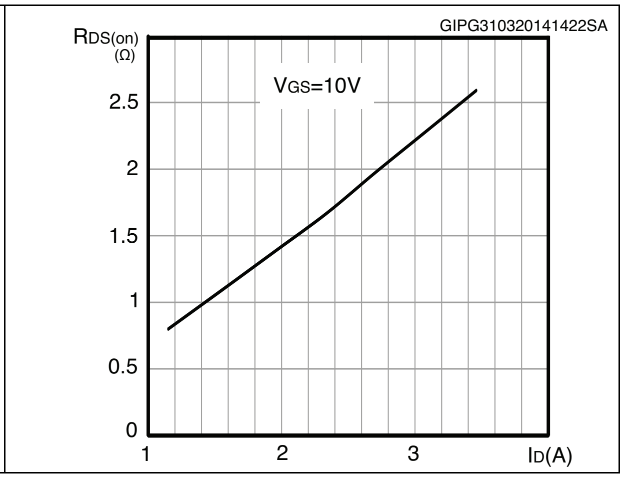


Figure 10. Capacitance variations

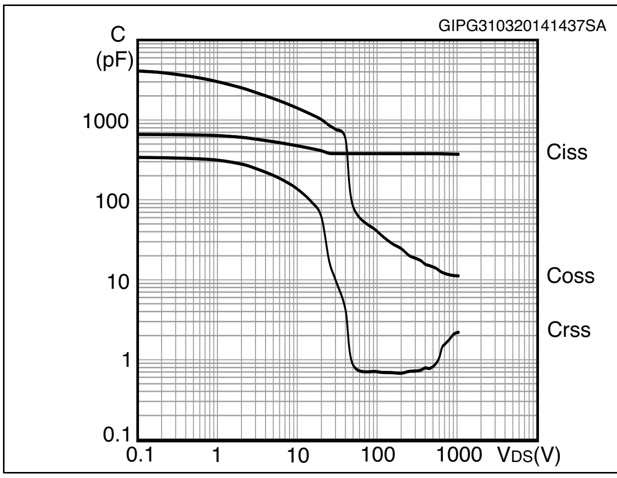


Figure 11. Output capacitance stored energy

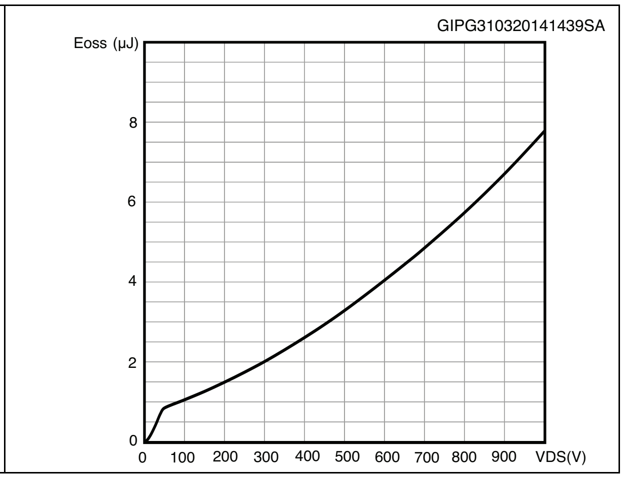


Figure 12. Normalized gate threshold voltage vs temperature

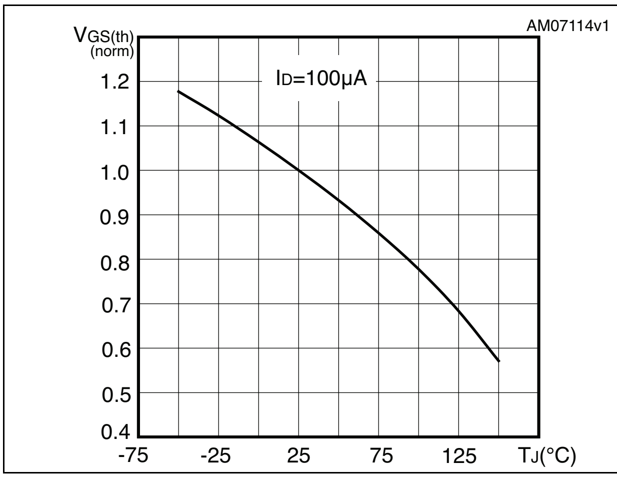


Figure 13. Normalized on-resistance vs temperature

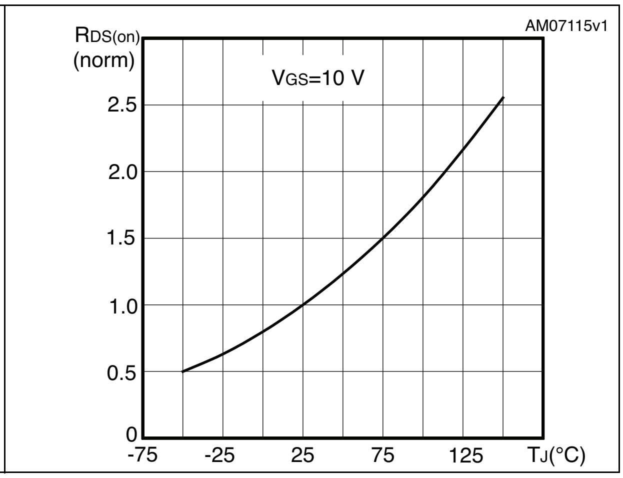


Figure 14. Source-drain diode forward characteristics

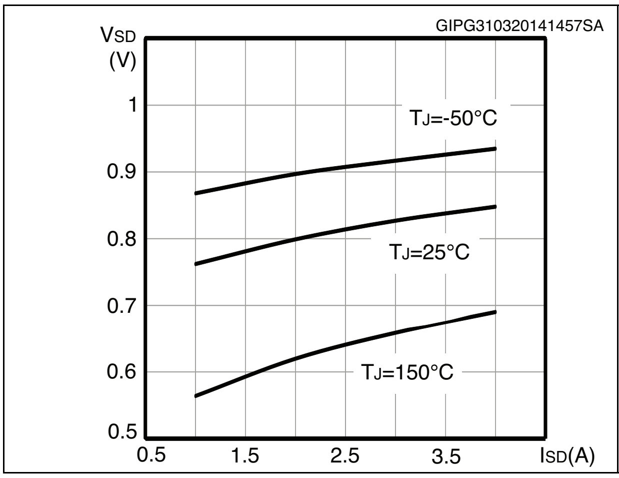


Figure 15. Normalized $V_{(BR)DSS}$ vs temperature

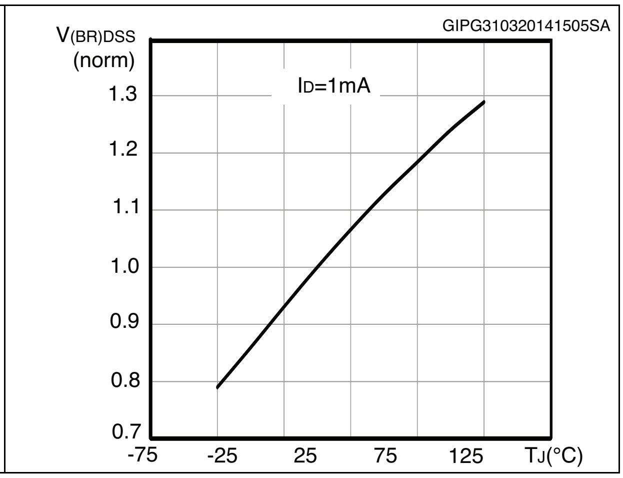
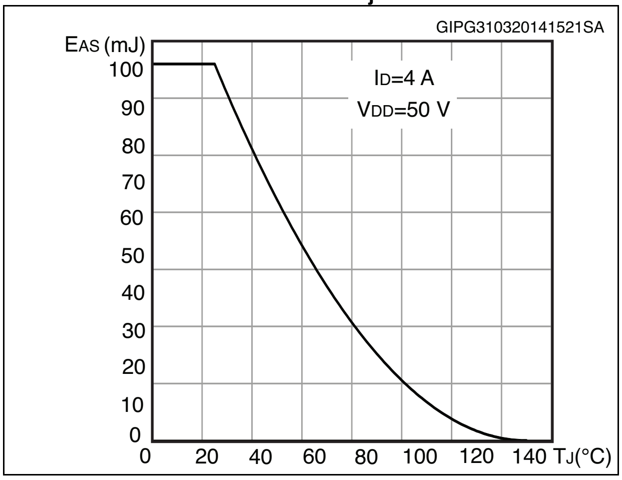


Figure 16. Maximum avalanche energy vs starting T_j



3 Test circuits

Figure 17. Switching times test circuit for resistive load

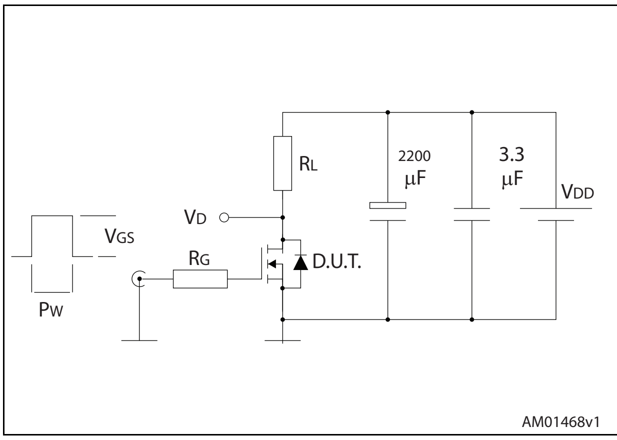


Figure 18. Gate charge test circuit

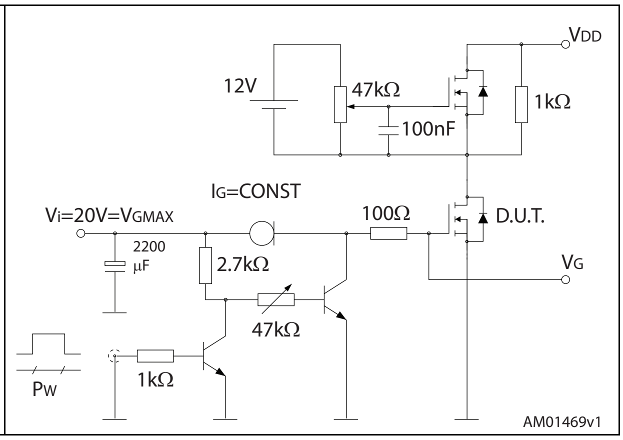


Figure 19. Test circuit for inductive load switching and diode recovery times

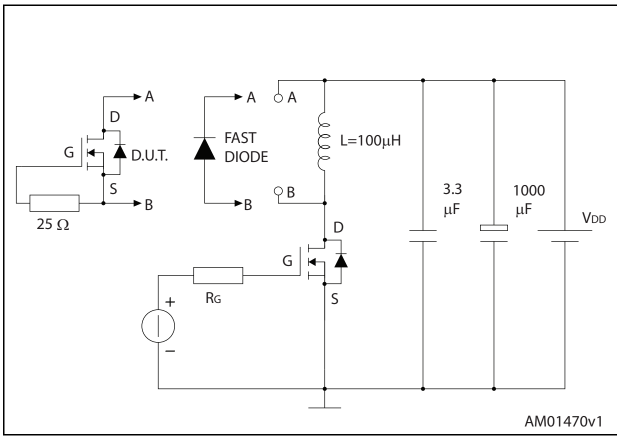


Figure 20. Unclamped inductive load test circuit

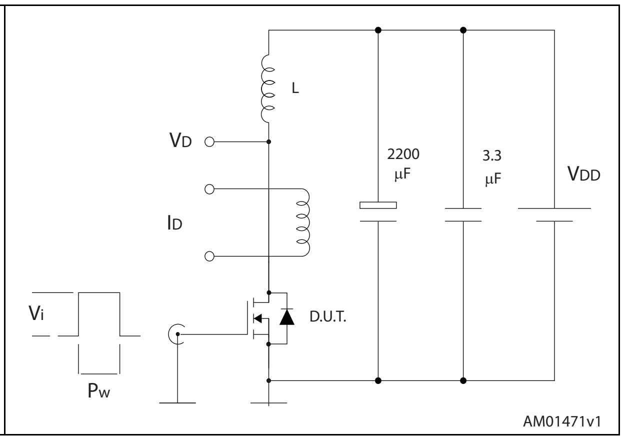


Figure 21. Unclamped inductive waveform

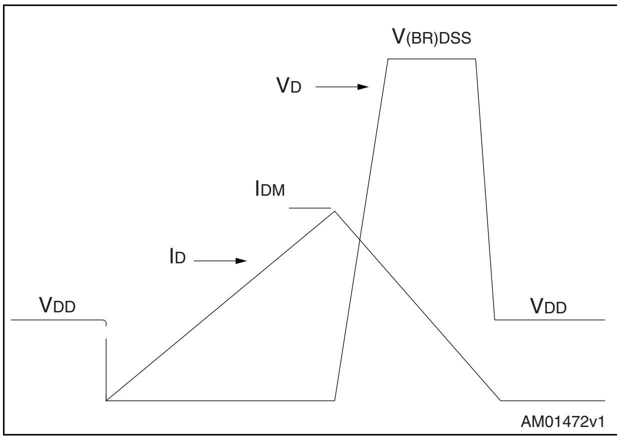
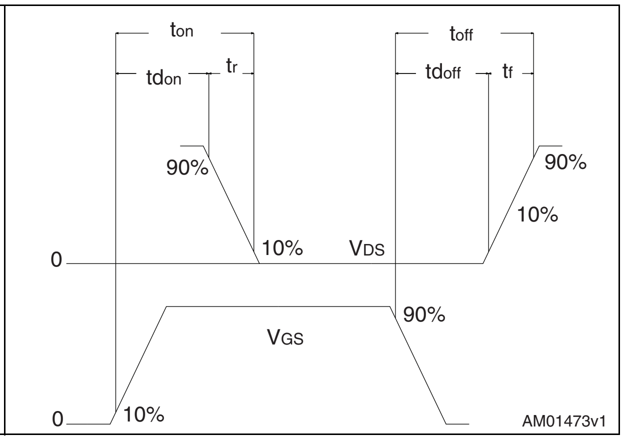


Figure 22. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 TO-220, STP7N105K5

Figure 23. TO-220 type A drawing

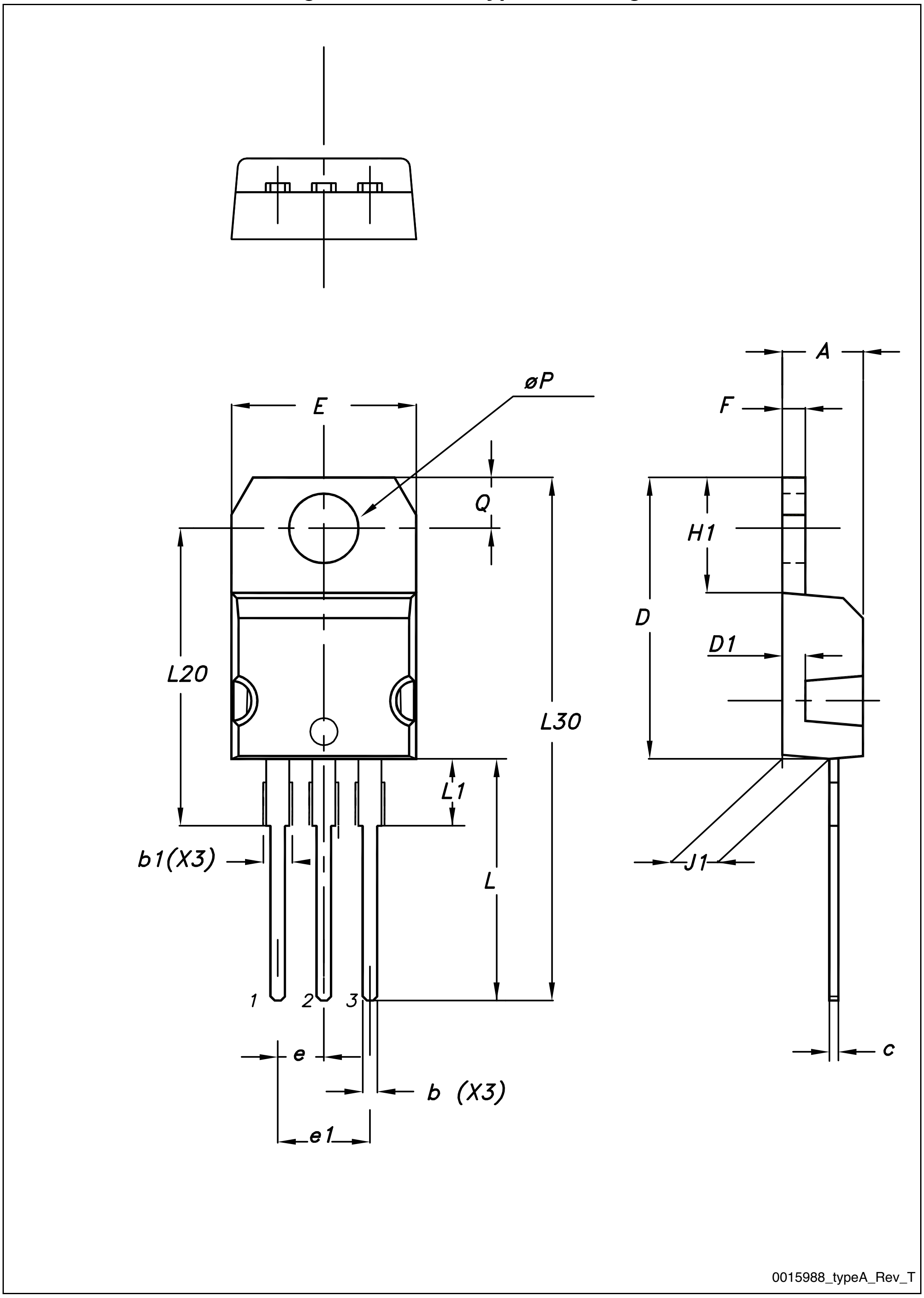


Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

4.2 IPAK, STU7N105K5

Figure 24. IPAK (TO-251) drawing

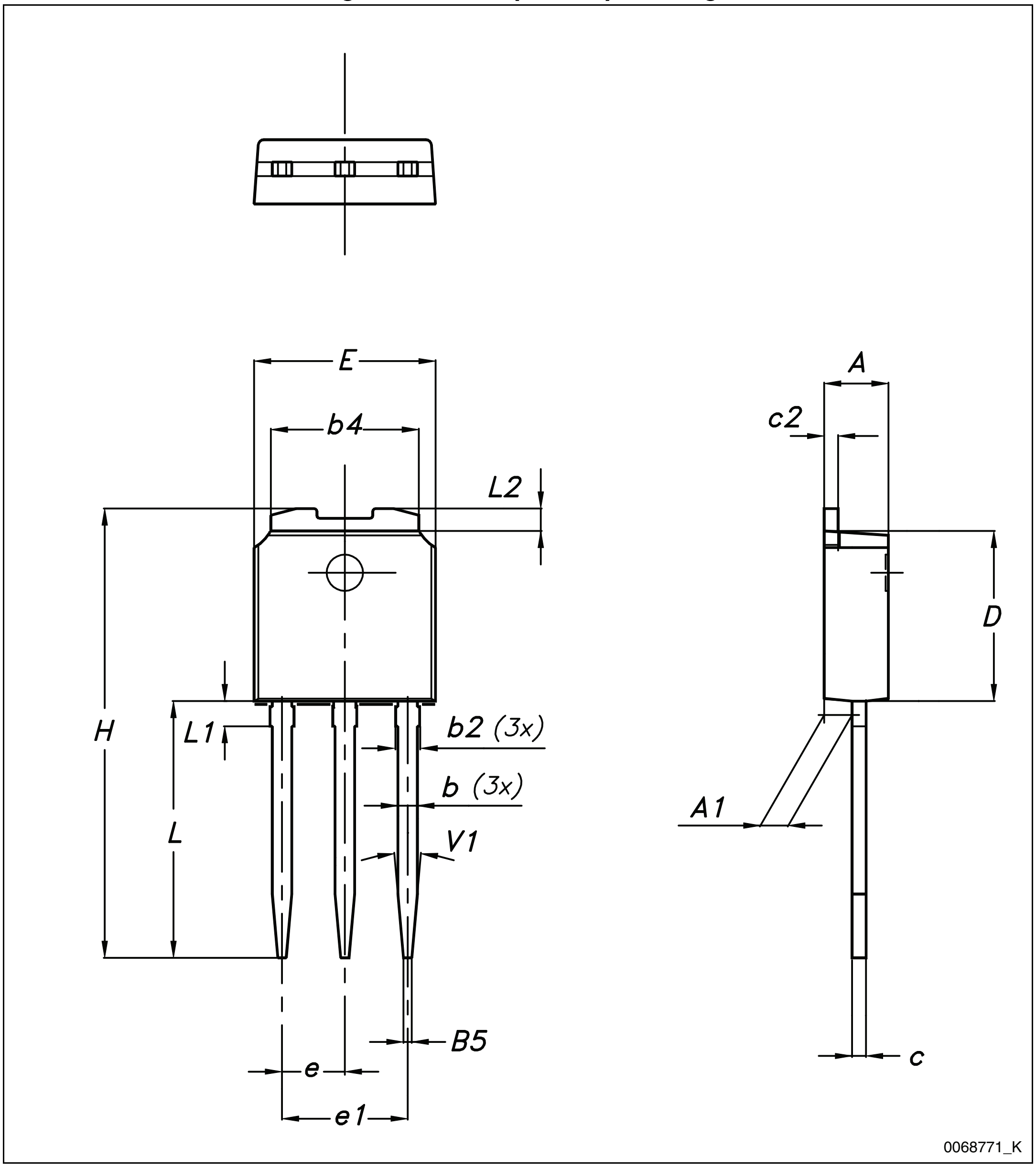


Table 10. IPAK (TO-251) mechanical data

DIM	mm.		
	min.	typ.	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

4.3 TO-247, STW7N105K5

Figure 25. TO-247 drawing

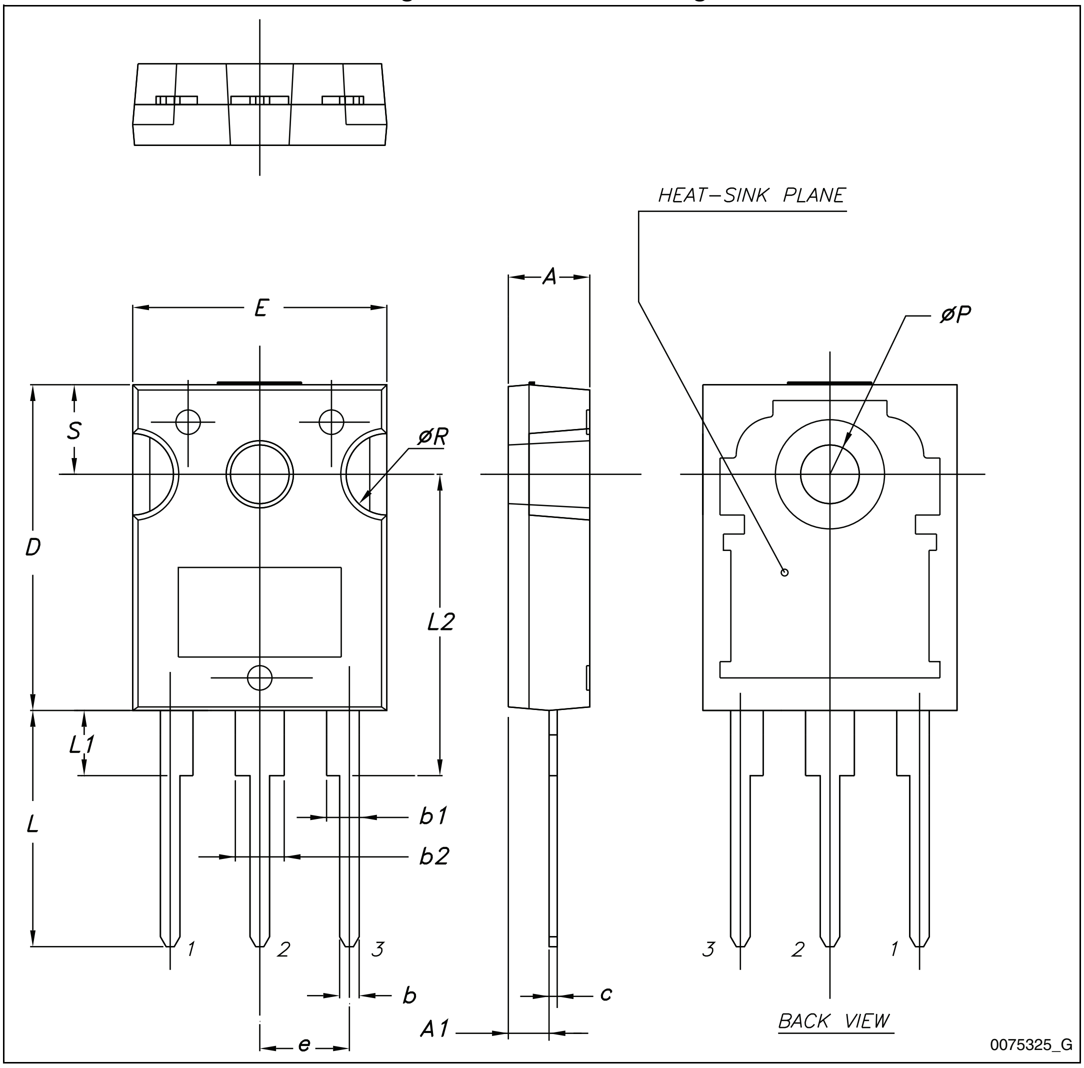


Table 11. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
07-Apr-2014	1	First release.