

N-channel 800 V, 0.470 Ω typ., 9 A MDmesh™ K5 Power MOSFET in a TO-220FP package

Datasheet - production data

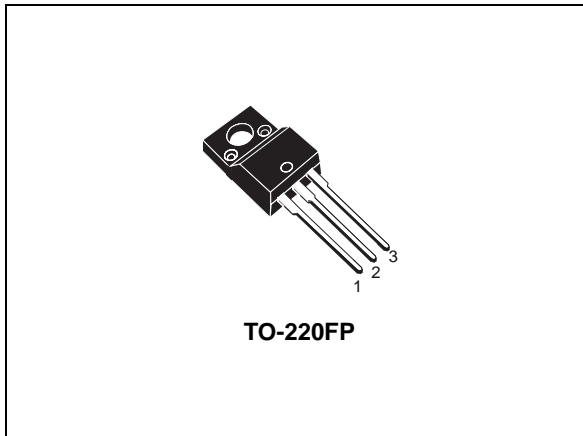
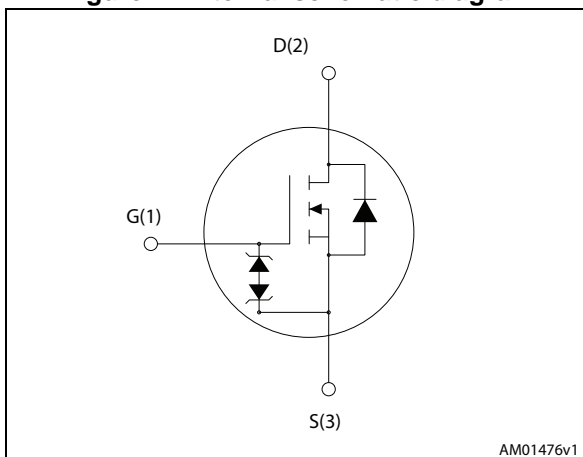


Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STF10N80K5	800 V	0.600 Ω	9 A	30 W

- Industry's best $R_{DS(on)}$
- Industry's best figure of merit (FoM)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STF10N80K5	10N80K5	TO-220FP	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Units
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	9	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6	A
$I_{DM}^{(2)}$	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	30	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	3	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	130	mJ
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2500	V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	50	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 9\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS(Peak)} \leq V_{(BR)DSS}$
- $V_{DS} \leq 640\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Units
$R_{thj-case}$	Thermal resistance junction-case max	4.2	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	800			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 800\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 800\text{ V}, T_C = 125\text{ °C}$			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$		0.470	0.600	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	635	-	pF
C_{oss}	Output capacitance		-	53	-	pF
C_{rss}	Reverse transfer capacitance		-	0.8	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0, V_{DS} = 0\text{ to }640\text{ V}$	-	85	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	34	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	6	-	Ω
Q_g	Total gate charge	$V_{DD} = 640\text{ V}, I_D = 9\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 16)	-	22	-	nC
Q_{gs}	Gate-source charge		-	5.5	-	nC
Q_{gd}	Gate-drain charge		-	13.2	-	nC

1. "Time related" is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. "Energy related" is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 4.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 18)	-	14.5	-	ns
t_r	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time		-	35	-	ns
t_f	Fall time		-	14	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
I_{SDM}	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 9\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, (see Figure 17)	-	370		ns
Q_{rr}	Reverse recovery charge		-	4.58		μC
I_{RRM}	Reverse recovery current		-	25		A
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}$, $V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	520		ns
Q_{rr}	Reverse recovery charge		-	5.88		μC
I_{RRM}	Reverse recovery current		-	22.5		A

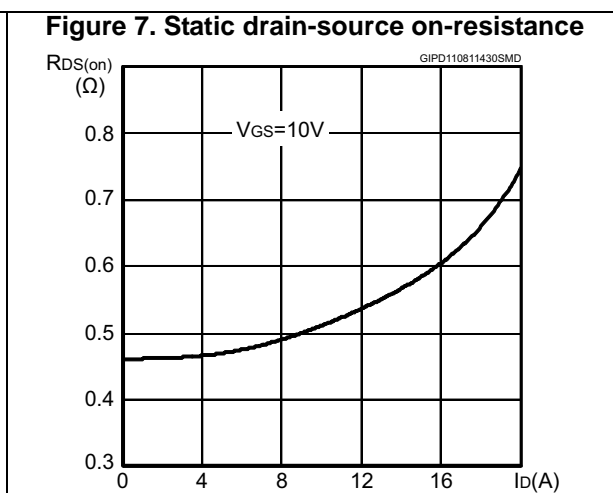
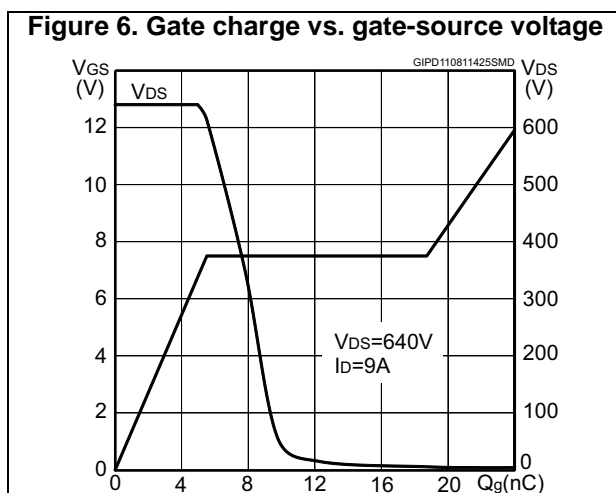
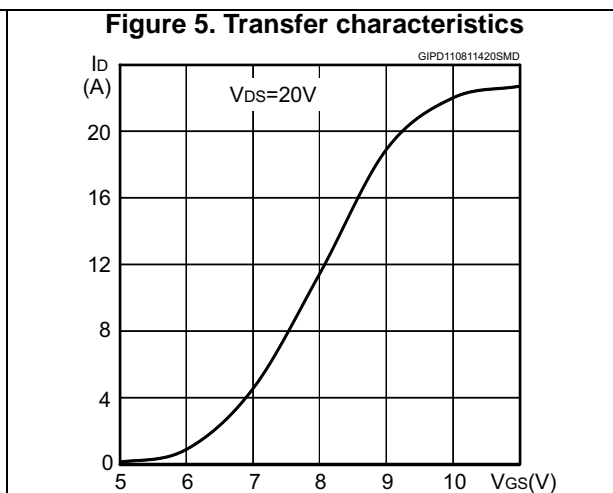
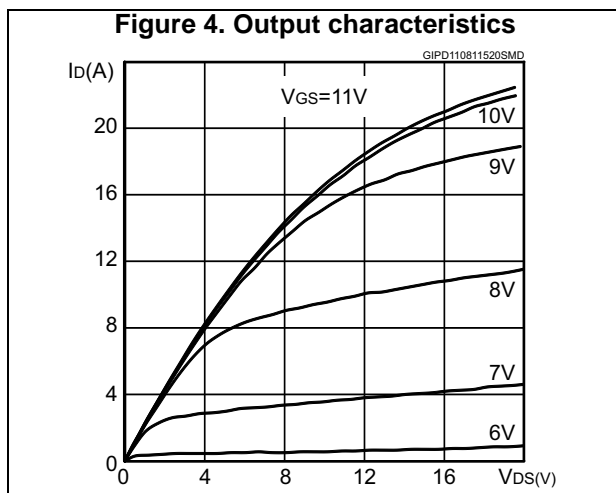
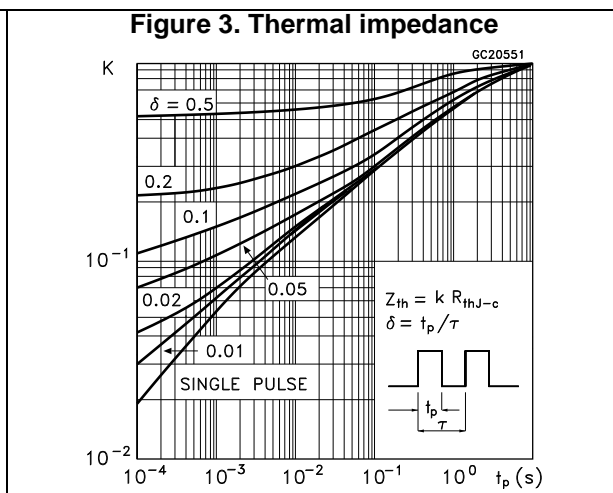
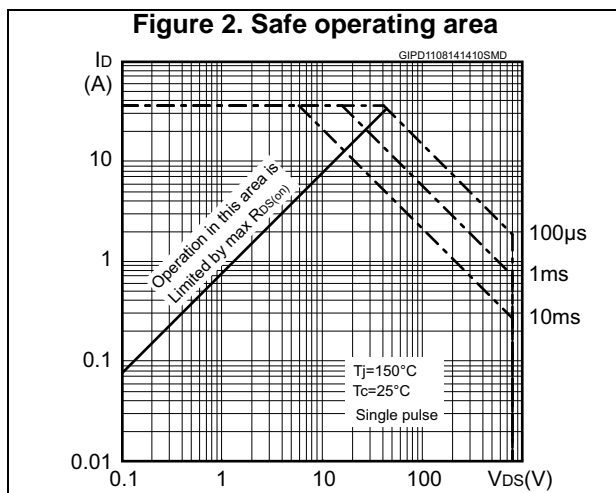
1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0$	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

3 Electrical characteristics (curves)



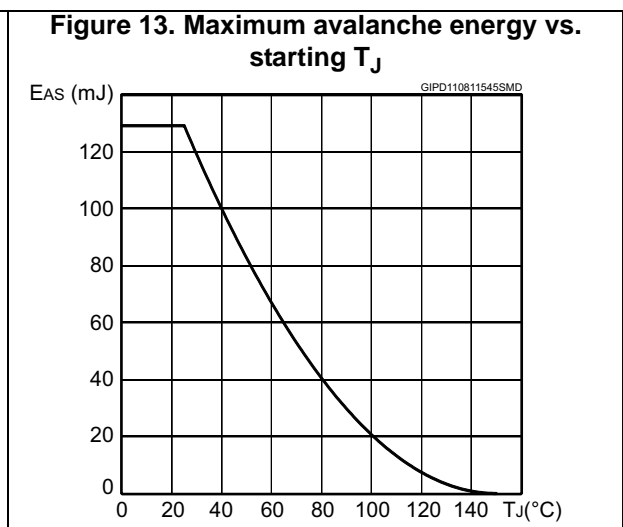
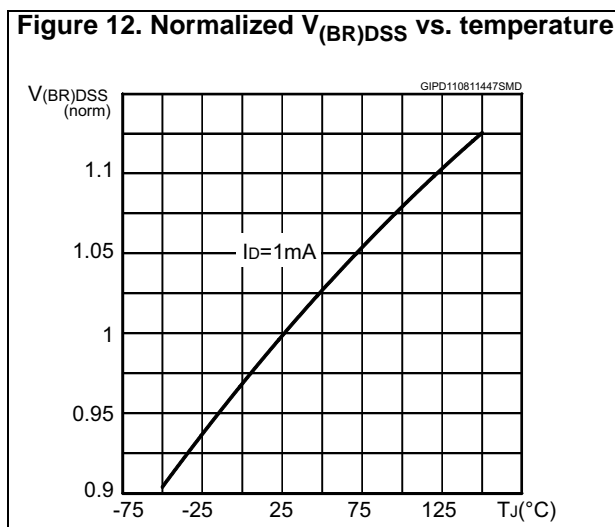
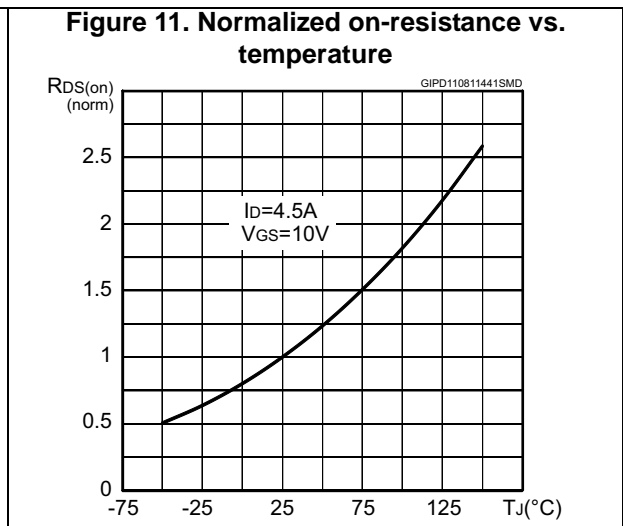
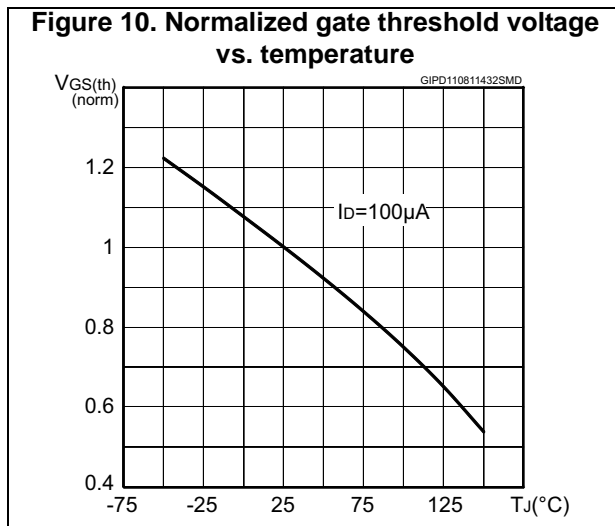
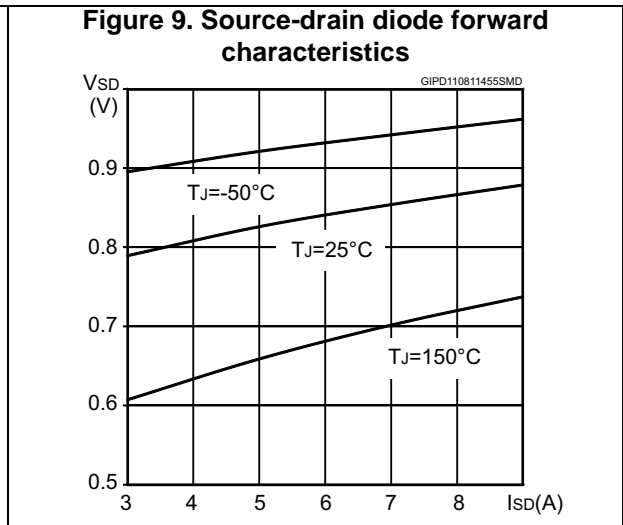
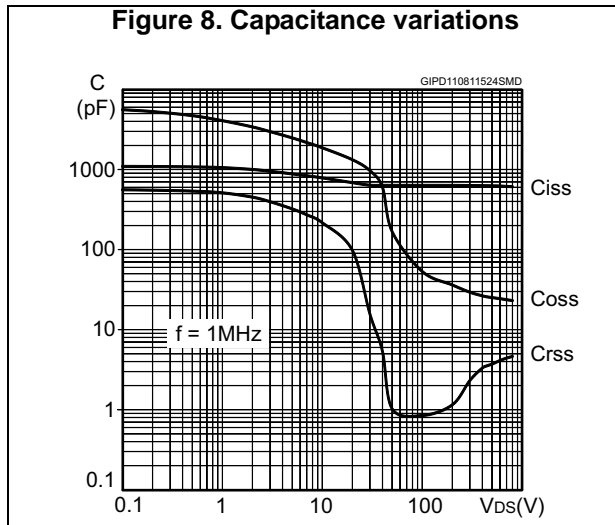
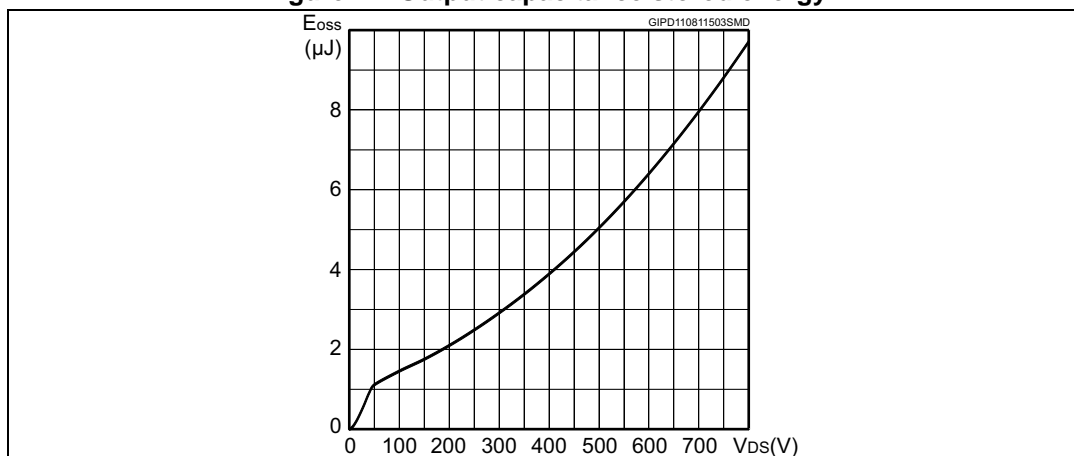


Figure 14. Output capacitance stored energy



4 Test circuits

Figure 15. Switching times test circuit for resistive load

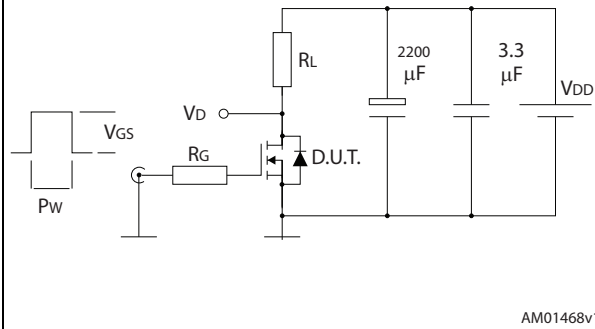


Figure 16. Gate charge test circuit

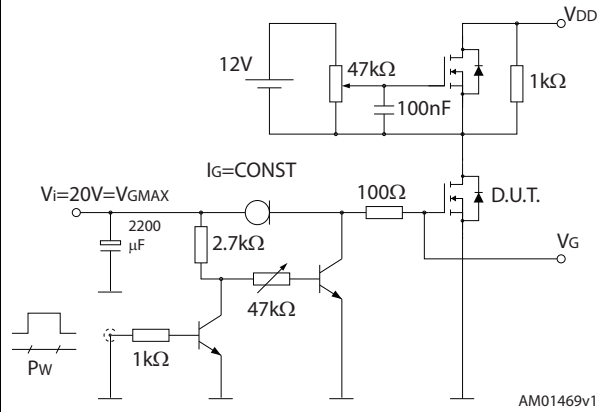


Figure 17. Test circuit for inductive load switching and diode recovery times

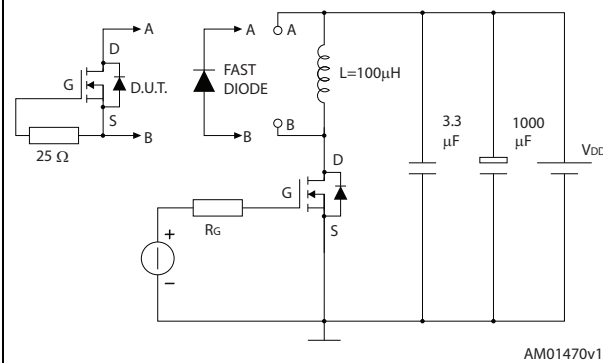
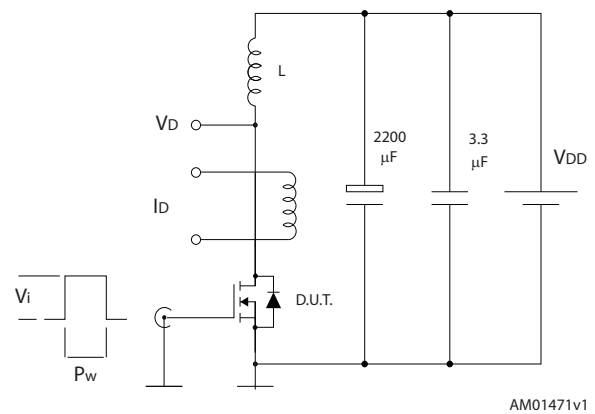


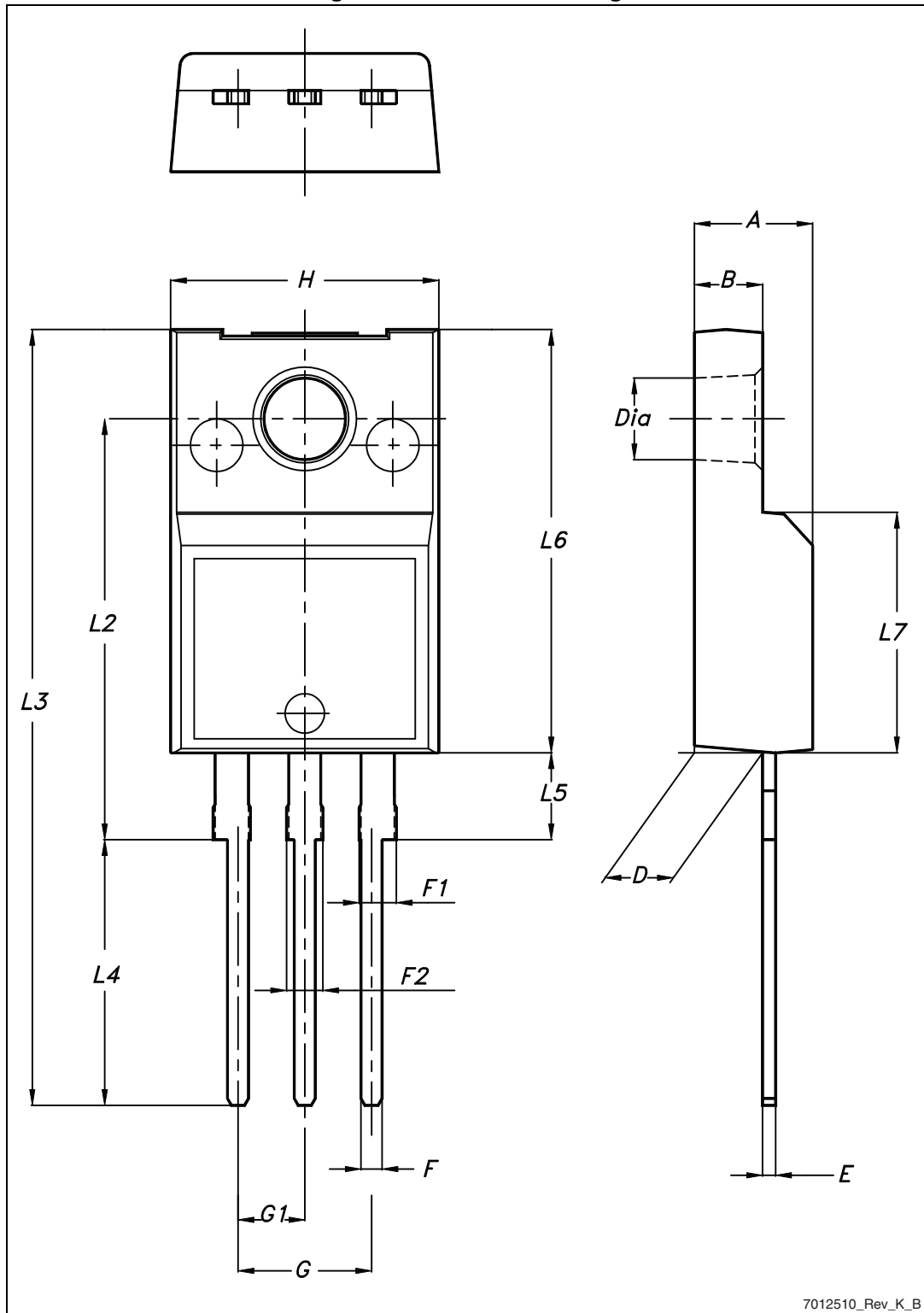
Figure 18. Unclamped inductive load test circuit



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. TO-220FP drawing



7012510_Rev_K_B

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
23-Jun-2014	1	Initial release.
13-Aug-2014	2	<ul style="list-style-type: none">– Document status promoted from preliminary data to production data.– Inserted Section 3: Electrical characteristics (curves).– Minor text changes.
17-Sep-2014	3	Updated title, features and description in cover page.
05-Nov-2014	4	Updated 3: Electrical characteristics (curves) Minor text changes

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