

## Automotive-grade N-channel 600 V, 0.085 $\Omega$ typ., 34 A MDmesh™ DM2 Power MOSFET in a D<sup>2</sup>PAK package

Datasheet - production data

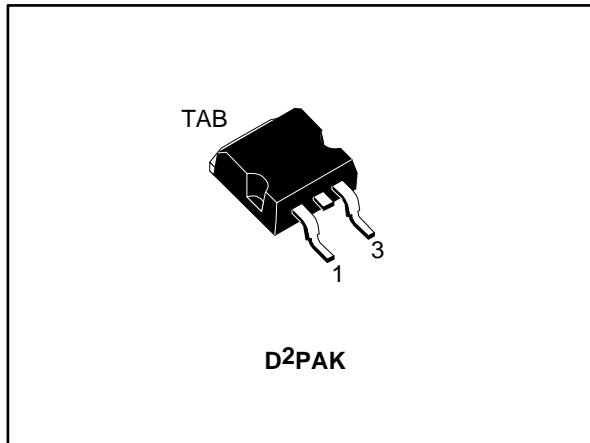
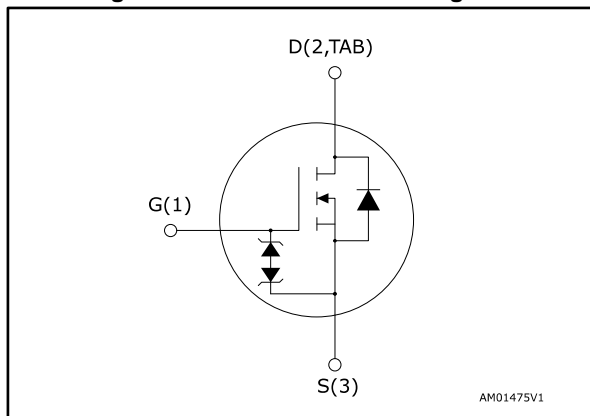


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub> @ T <sub>Jmax.</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STB45N60DM2AG	650 V	0.093 $\Omega$	34 A	250 W

- Designed for automotive applications and AEC-Q101 qualified
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge ( $Q_{rr}$ ) and time ( $t_{rr}$ ) combined with low  $R_{DS(on)}$ , rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STB45N60DM2AG	45N60DM2	D <sup>2</sup> PAK	Tape and reel

---

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
	2.1 Electrical characteristics (curves).....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information .....</b>	<b>9</b>
	4.1 D <sup>2</sup> PAK (TO-263) type A package information .....	9
	4.2 D <sup>2</sup> PAK packing information .....	12
<b>5</b>	<b>Revision history .....</b>	<b>14</b>

# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	34	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	21	
$I_{DM}^{(1)}$	Drain current (pulsed)	136	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ °C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_{stg}$	Storage temperature	-55 to 150	°C
$T_j$	Operating junction temperature		

**Notes:**

(1) Pulse width is limited by safe operating area.

(2)  $I_{SD} \leq 34\text{ A}$ ,  $di/dt=800\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

(3)  $V_{DS} \leq 480\text{ V}$ .

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.50	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	

**Notes:**

(1) When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive	6	A
$E_{AS}^{(1)}$	Single pulse avalanche energy	800	mJ

**Notes:**

(1) starting  $T_j = 25\text{ °C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$ , $T_{\text{case}} = 125\text{ °C}$			100	
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 17\text{ A}$		0.085	$0.09_3$	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	2500	-	$\mu\text{F}$
$C_{\text{oss}}$	Output capacitance		-	120	-	
$C_{\text{riss}}$	Reverse transfer capacitance		-	3	-	
$C_{\text{oss eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$	-	200	-	$\mu\text{F}$
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$	-	4	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 480\text{ V}$ , $I_{\text{D}} = 34\text{ A}$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 15: "Gate charge test circuit"</a> )	-	56	-	nC
$Q_{\text{gs}}$	Gate-source charge		-	13	-	
$Q_{\text{gd}}$	Gate-drain charge		-	30	-	

**Notes:**

<sup>(1)</sup>  $C_{\text{oss eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$ , $I_{\text{D}} = 25\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 14: "Switching times test circuit for resistive load"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	29	-	ns
$t_{\text{r}}$	Rise time		-	27	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	85	-	
$t_{\text{f}}$	Fall time		-	6	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		34	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		136	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 34\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 34\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 16</a> : "Test circuit for inductive load switching and diode recovery times")	-	120		ns
$Q_{rr}$	Reverse recovery charge		-	0.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	10.4		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 34\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> : "Test circuit for inductive load switching and diode recovery times")	-	240		ns
$Q_{rr}$	Reverse recovery charge		-	2.4		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20.5		A

**Notes:**

- <sup>(1)</sup> Pulse width is limited by safe operating area.  
<sup>(2)</sup> Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

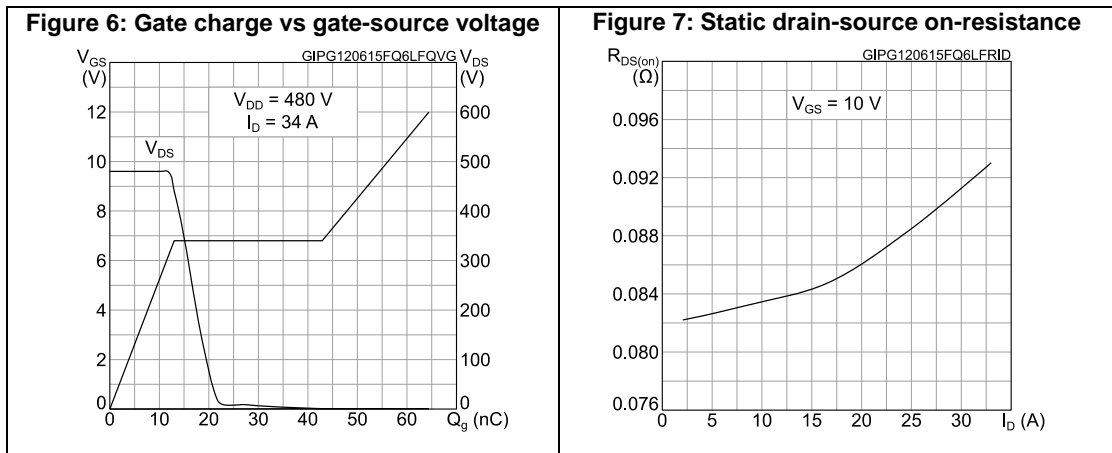
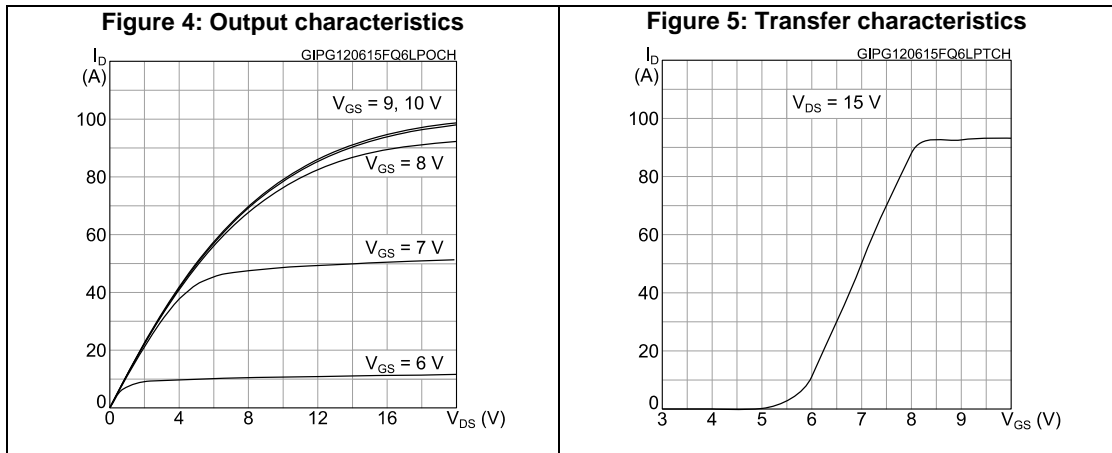
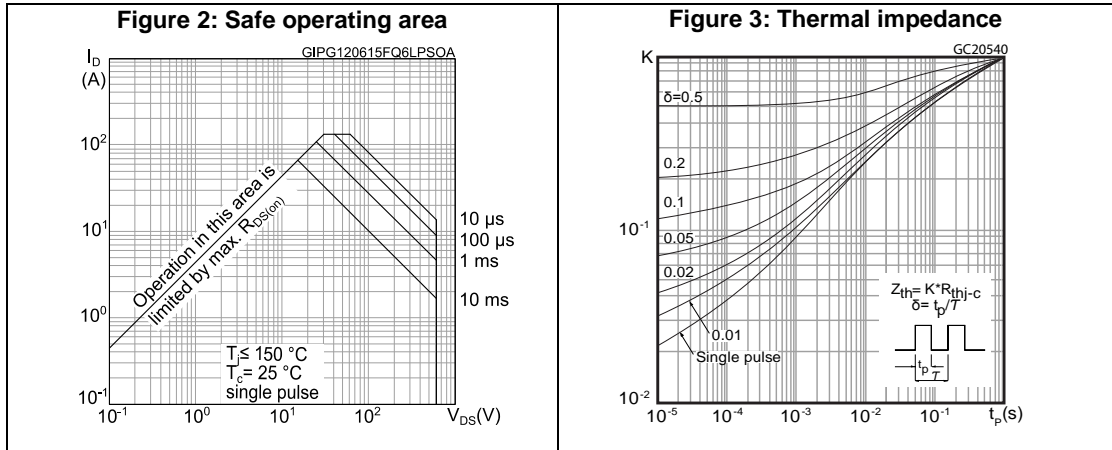


Figure 8: Capacitance variations

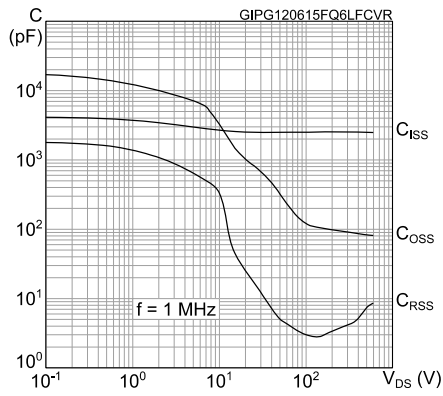


Figure 9: Normalized gate threshold voltage vs temperature

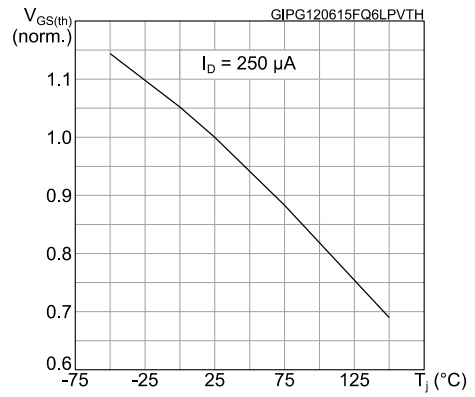


Figure 10: Normalized on-resistance vs temperature

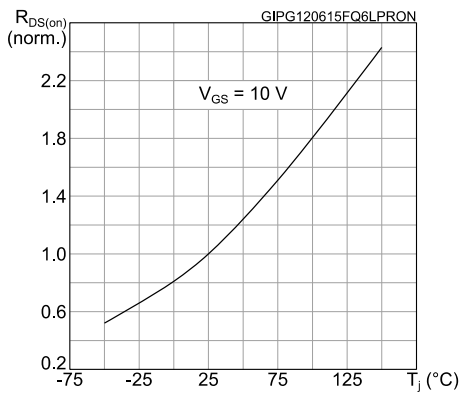


Figure 11: Normalized V(BR)DSS vs temperature

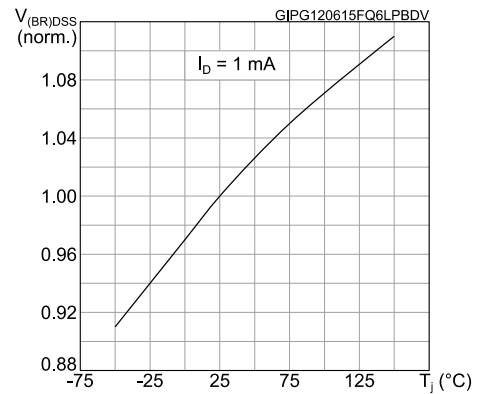


Figure 12: Output capacitance stored energy

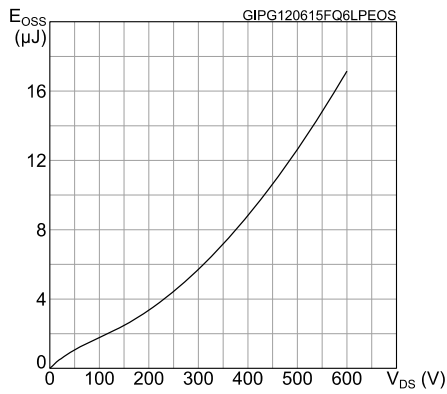
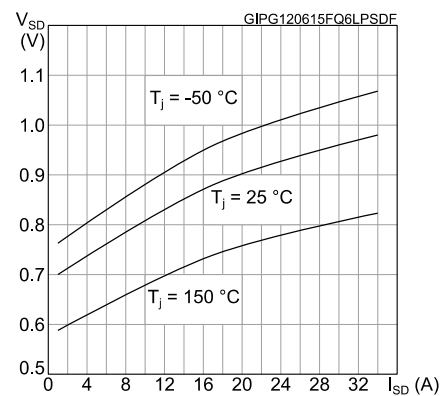
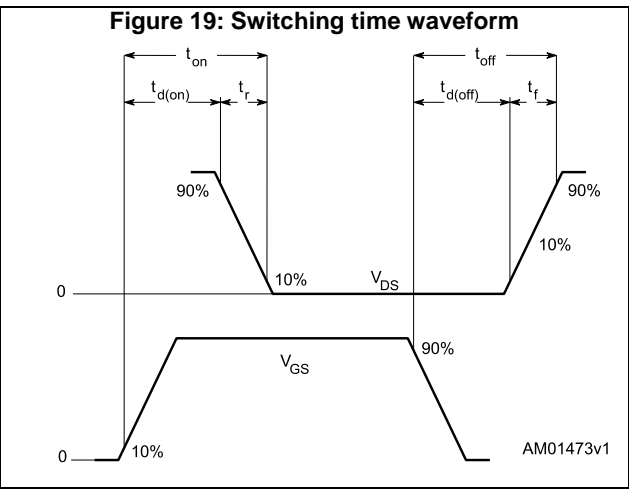
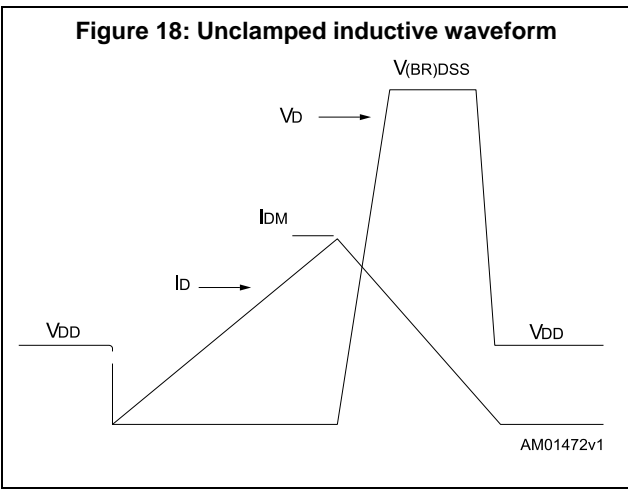
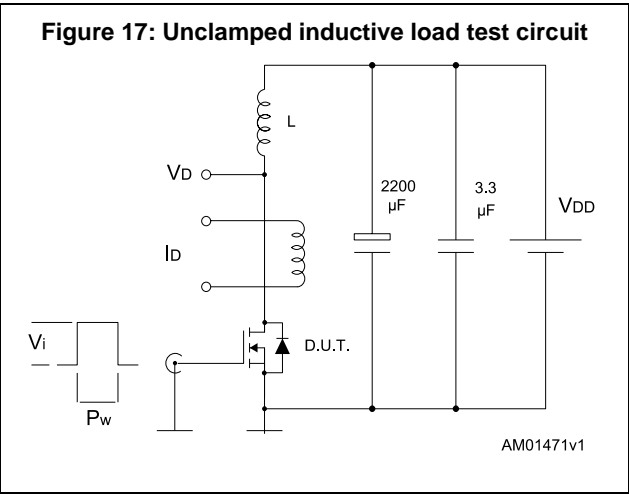
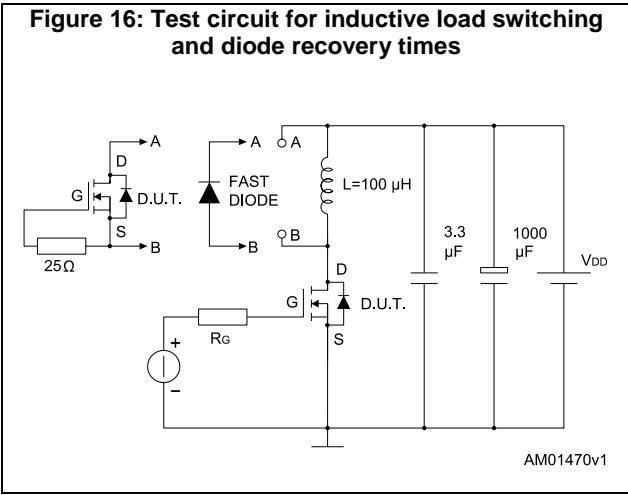
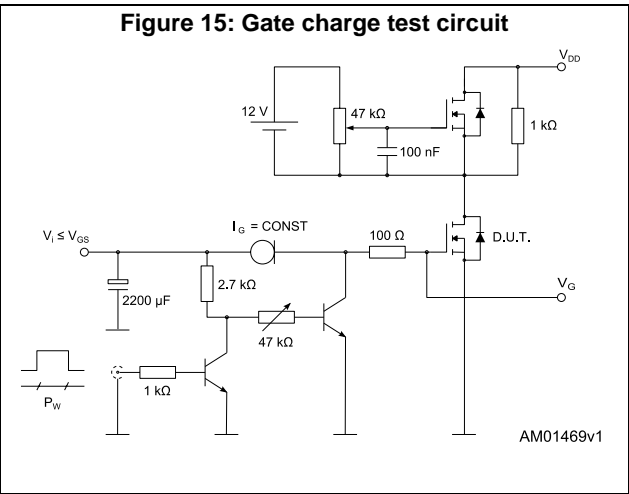
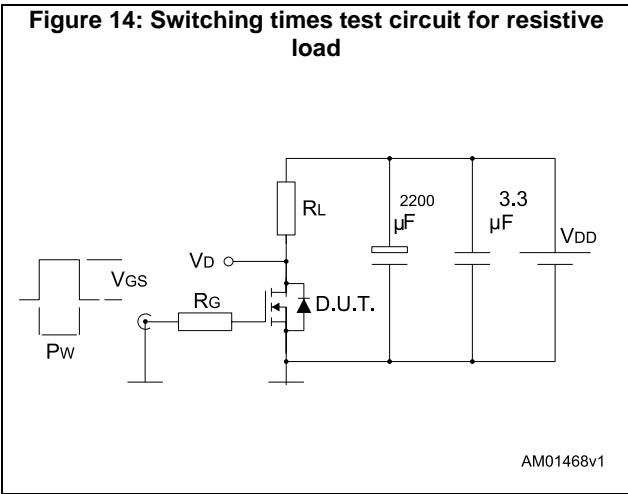


Figure 13: Source-drain diode forward characteristics



### 3 Test circuits





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 D<sup>2</sup>PAK (TO-263) type A package information

Figure 20: D<sup>2</sup>PAK (TO-263) type A package outline

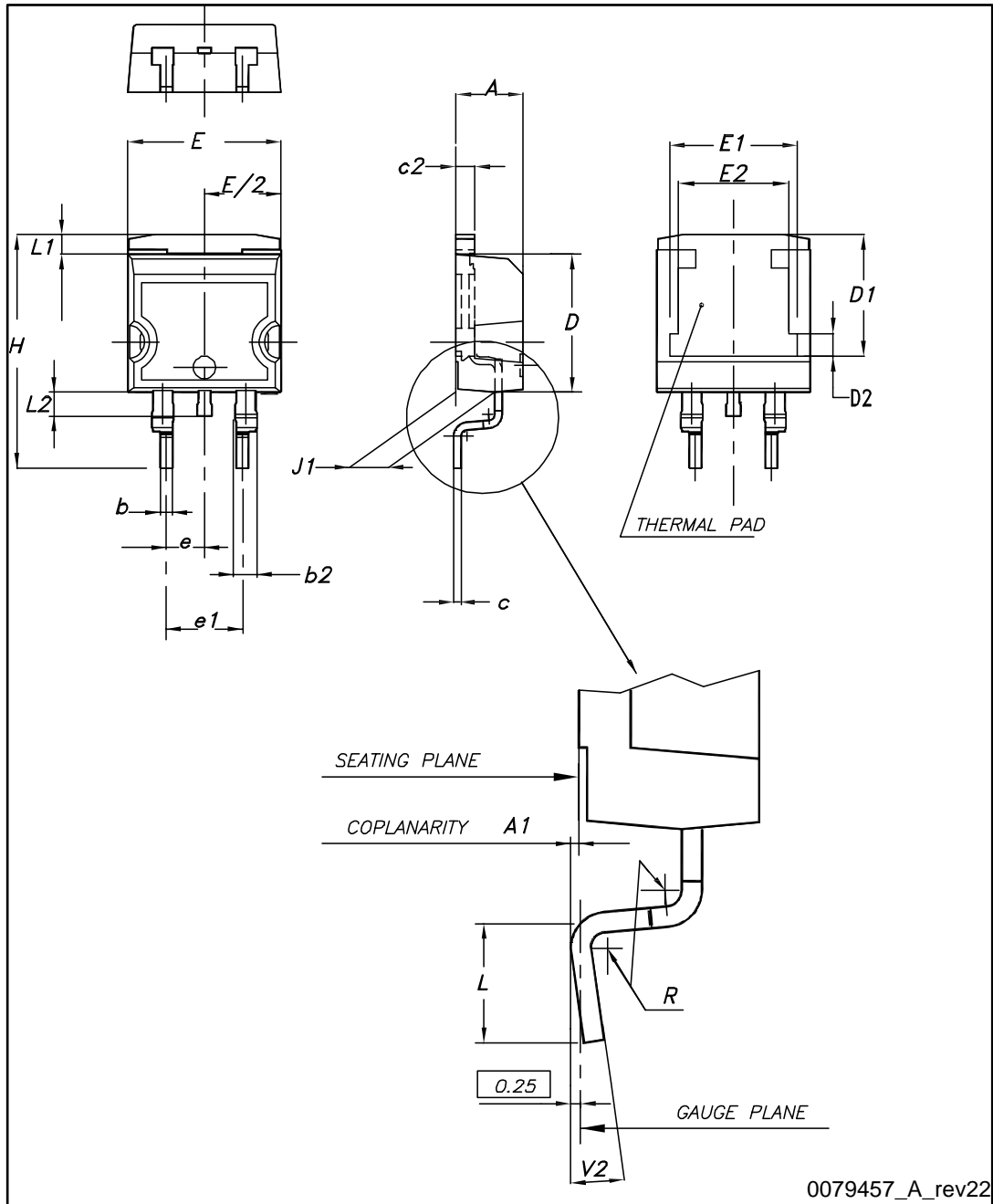
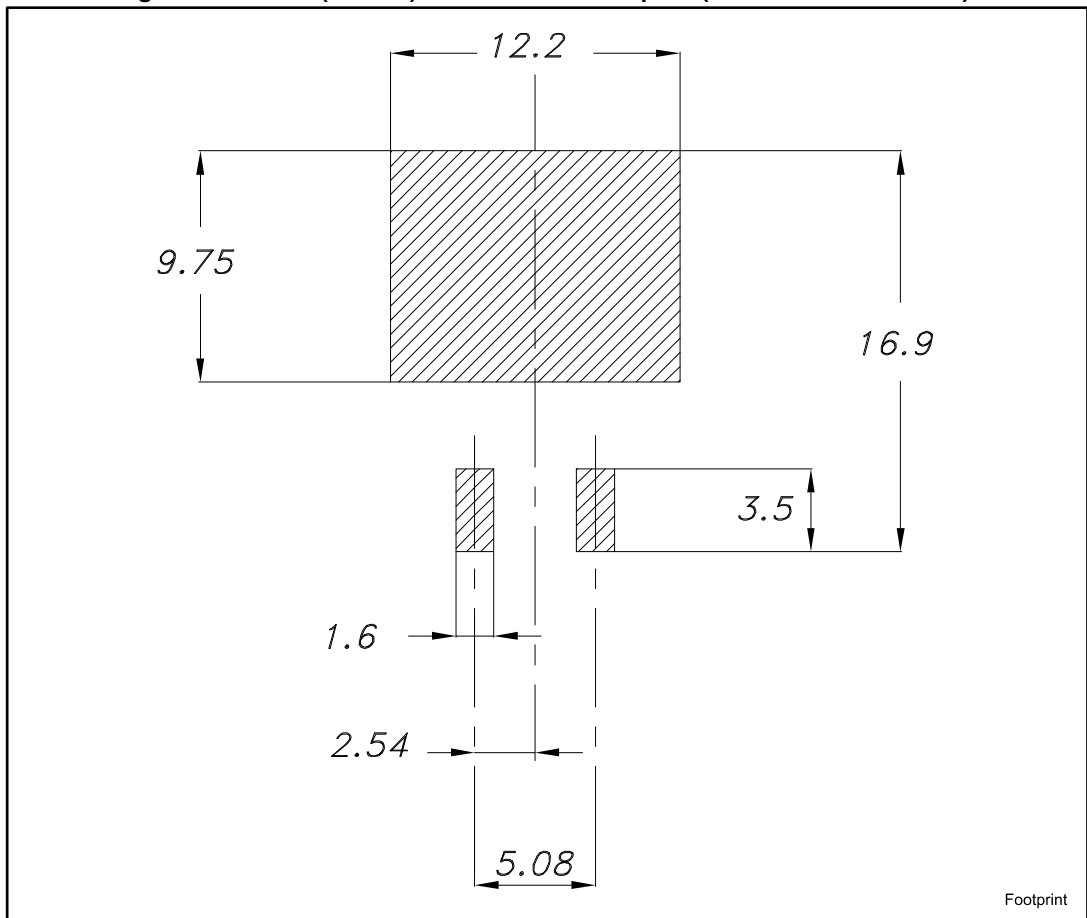


Table 9: D<sup>2</sup>PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 21: D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)



### 4.2 D<sup>2</sup>PAK packing information

Figure 22: Tape

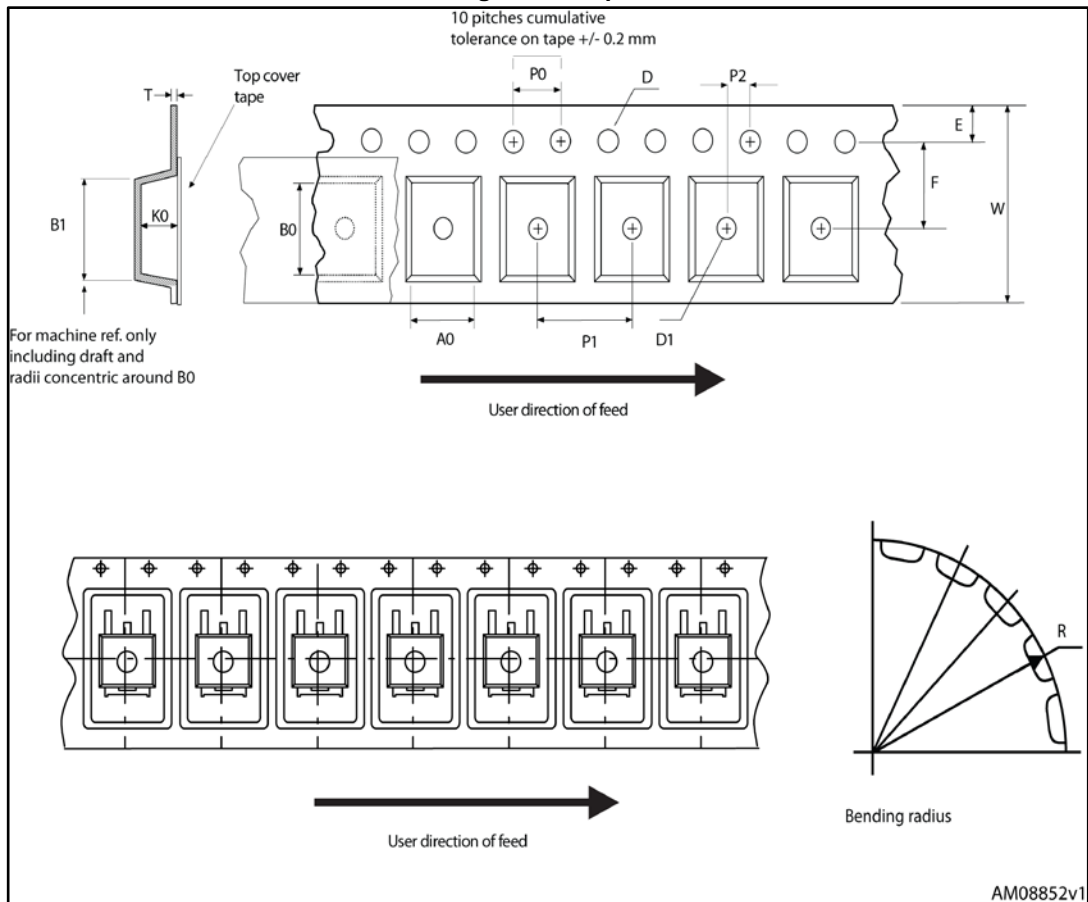


Figure 23: Reel

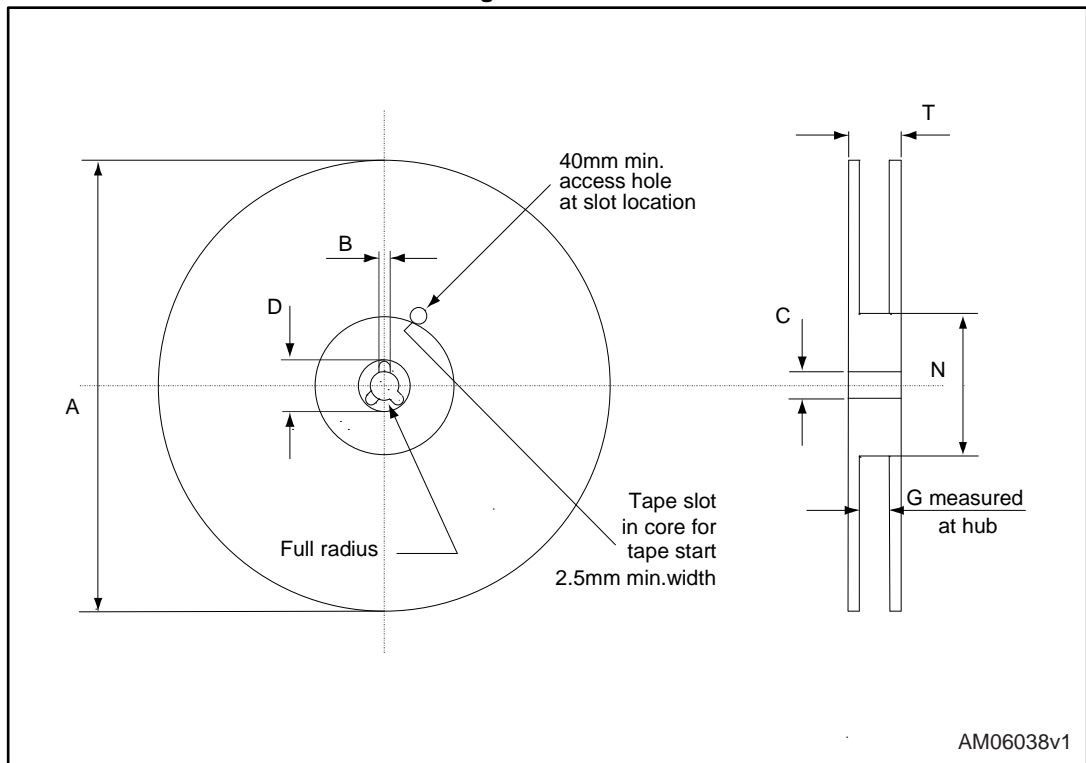


Table 10: D<sup>2</sup>PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
02-Jul-2015	1	Initial release.

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[STB45N60DM2AG](#)