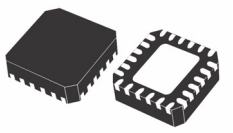
LED7706

6-rows 30 mA LEDs driver with boost regulator for LCD panels backlight

Features

- Boost section
  - 4.5 V to 36 V input voltage range
  - Internal power MOSFET
  - Internal +5 V LDO for device supply
  - Up to 36 V output voltage
  - Constant frequency peak current-mode control
  - 250 kHz to 1 MHz adjustable switching frequency
  - External synchronization for multi-device application
  - Pulse-skip power saving mode at light load
  - Programmable soft-start
  - Programmable OVP protection
  - Stable with ceramic output capacitors
  - Thermal shutdown
- Backlight driver section
  - Six rows with 30 mA maximum current capability (adjustable)
  - Rows disable option
  - Less than 500 ns minimum dimming on-time (1 % minimum dimming duty-cycle at 20 kHz)
  - ±2 % current matching between rows
  - LED failure (open and short-circuit) detection



VFQFPN-24 4x4

Description

The LED7706 consists of a high efficiency monolithic boost converter and six controlled current generators (rows) specifically designed to supply LEDs arrays used in the backlighting of LCD panels. The device can manage an output voltage up to 36 V (i.e. 10 white LEDs per row).

The generators can be externally programmed to sink up to 30 mA and can be dimmed via a PWM signal (1 % dimming duty-cycle at 20 kHz can be managed). The device allows to detect and manage the open and shorted LED faults and to let unused rows floating. Basic protections (output over-voltage, internal MOSFET over-current and thermal shutdown) are provided.

Applications

- LCD monitors and TV panels
- PDAs panel backlight
- GPS panel backlight

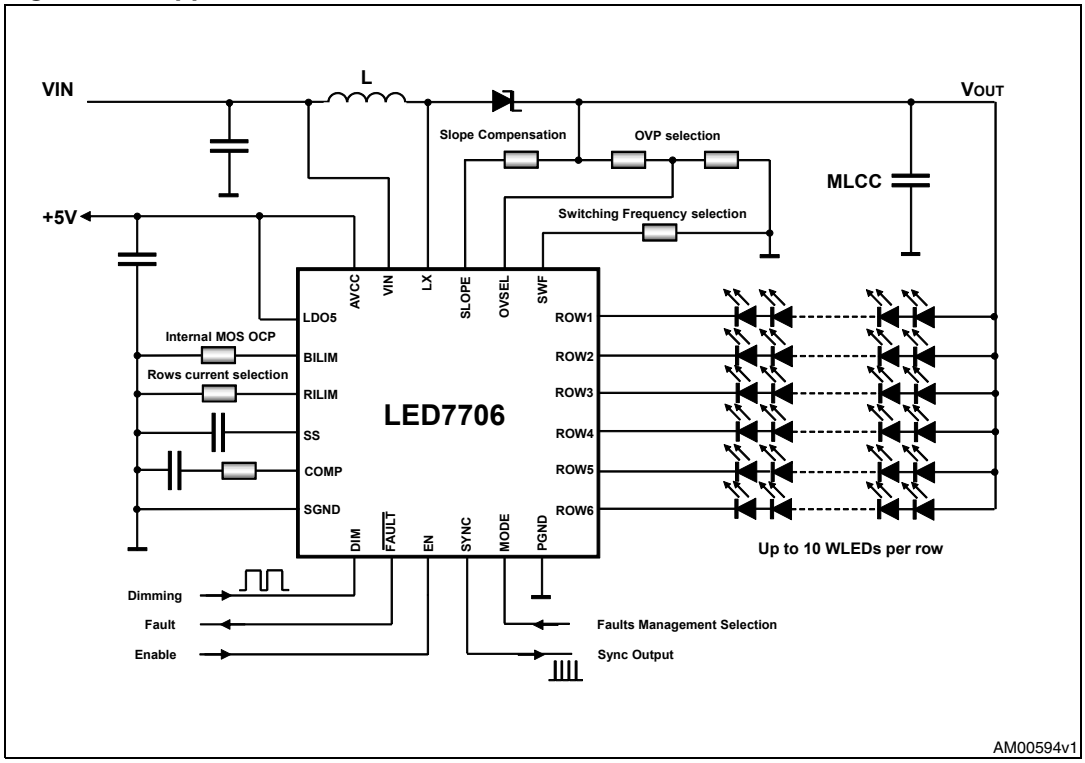
Table 1. Device summary

Order codes	Package	Packaging
LED7706	VFQFPN-24 4x4 (exposed pad)	Tube
LED7706TR		Tape and reel

Contents

1 Typical application circuit

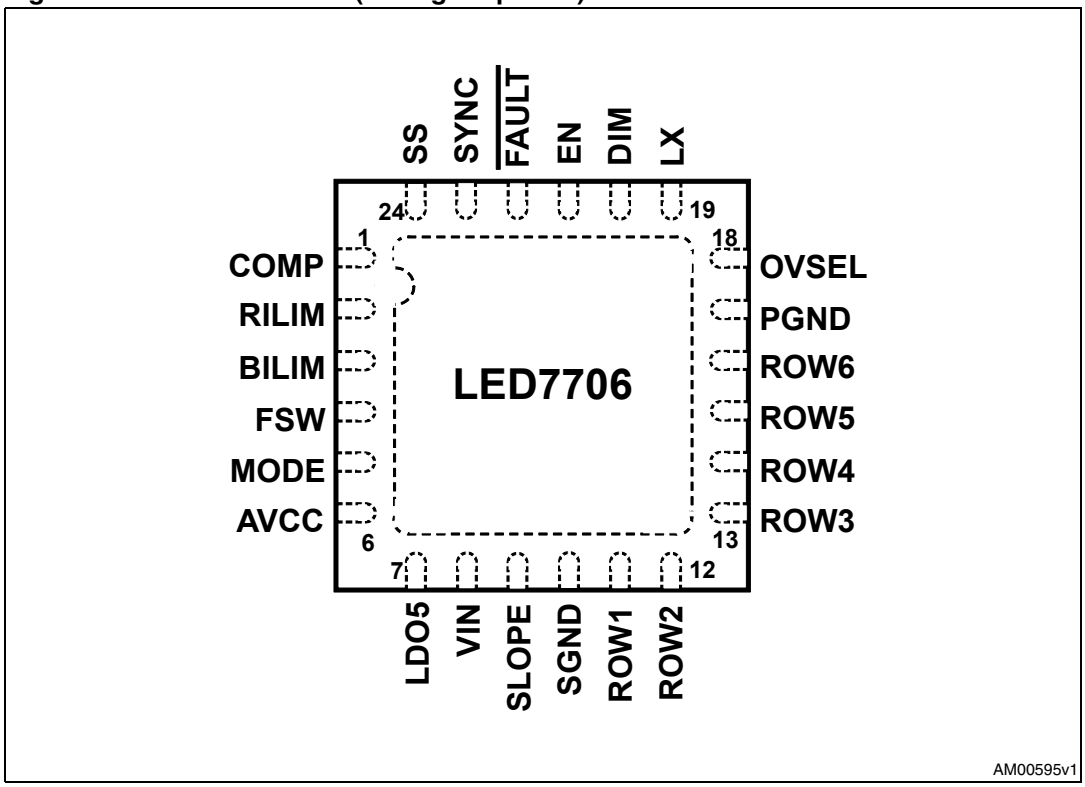
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 2. Pin functions

N°	Pin	Function
1	COMP	Error amplifier output. A simple RC series between this pin and ground is needed to compensate the loop of the boost regulator.
2	RILIM	Output generators current limit setting. The output current of the rows can be programmed connecting a resistor to SGND.
3	BILIM	Boost converter current limit setting. The internal MOSFET current limit can be programmed connecting a resistor to SGND.
4	FSW	Switching frequency selection and external sync input. A resistor to SGND is used to set the desired switching frequency. The pin can also be used as external synchronization input. See *Section 5.1.5 on page 15* for details.
5	MODE	Current generators fault management selector. It allows to detect and manage LEDs failures. See *Section 5.3.2 on page 21* for details.
6	AVCC	+ 5 V analog supply. Connect to LDO5 through a simple RC filter.
7	LDO5	+ 5 V LDO output and power section supply. Bypass to SGND with a 1 µF ceramic capacitor.
8	VIN	Input voltage. Connect to the main supply rail.
9	SLOPE	Slope compensation setting. A resistor between the output of the boost converter and this pin is needed to avoid sub-harmonic instability. Refer to *Section 6.1 on page 24* for details.
10	SGND	Signal ground. Supply return for the analog circuitry and the current generators.
11	ROW1	Row driver output #1.
12	ROW2	Row driver output #2.
13	ROW3	Row driver output #3.
14	ROW4	Row driver output #4.
15	ROW5	Row driver output #5.
16	ROW6	Row driver output #6.
17	PGND	Power ground. Source of the internal Power MOSFET.
18	OVSEL	Over-voltage selection. Used to set the desired OV threshold by an external divider. See *Section 5.1.4 on page 14* for details.
19	LX	Switching node. Drain of the internal Power MOSFET.
20	DIM	Dimming input. Used to externally set the brightness by using a PWM signal.
21	EN	Enable input. When low, the device is turned off. If tied high or left open, the device is turned on and a soft-start sequence takes place.
22	$\overline{\text{FAULT}}$	Fault signal output. Open drain output. The pin goes low when a fault condition is detected (see *Section 5.3.1 on page 21* for details).
23	SYNC	Synchronization output. Used as external synchronization output.
24	SS	Soft-start. Connect a capacitor to SGND to set the desired soft-start duration.

3 Electrical data

3.1 Maximum rating

Table 3. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{LDO5}	LDO5 to SGND	-0.3 to 6	
	PGND to SGND	-0.3 to 0.3	
V_{IN}	VIN to PGND	-0.3 to 40	
V_{LX}	LX to SGND	-0.3 to 40	
	LX to PGND	-0.3 to 40	
	RILIM, BILIM, SYNC, OVSEL, SS to SGND	-0.3 to V_{AVCC} + 0.3	
	EN, DIM, SW, MODE, FAULT to SGND	-0.3 to 6	
	ROWx to PGND/ SGND	-0.3 to 40	
	SLOPE to VIN	V_{IN} - 0.3 to V_{IN} + 6	
	SLOPE to SGND	-0.3 to 40	
	Internal switch maximum RMS current (flowing through LX node)	2.0	A
P_{TOT}	Power dissipation @ T_A = 25 °C	2.3 (2)	W
	Maximum withstanding voltage range test condition: CDF-AEC-Q100-002- “human body model” acceptance criteria: “normal performance”	±1000	V

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. Power dissipation referred to the device mounted on the demonstration board described in section 5.5

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	-50 to 150	°C
T_J	Junction operating temperature range	-40 to 150	°C

4 Electrical characteristics

V_{IN} = 12 V; T_J = 25 °C and LDO5 connected to AVCC if not otherwise specified [a]

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply section						
V_{IN}	Input voltage range		4.5		36	V
V_{BST}	Boost section output voltage				36	
V_{LDO5} / V_{AVCC}	LDO output and IC supply voltage	EN High I_{LDO5} = 0 mA	4.4	5	5.5	V
$I_{IN,Q}$	Operating quiescent current	R_{RILIM} = 51 kΩ, R_{BILIM} = 220 kΩ, R_{SLOPE} = 680 kΩ DIM tied to SGND.		1		mA
$I_{IN,SHDN}$	Operating current in shutdown	EN low		20	30	µA
$V_{UVLO,ON}$	LDO5 under voltage lock out upper threshold			3.8	4.0	V
$V_{UVLO,OFF}$	LDO5 under voltage lock out lower threshold		3.3	3.6		
LDO linear regulator						
	Line regulation	6 V ≤ V_{IN} ≤ 36 V, I_{LDO5} = 30 mA			30	mV
	LDO dropout voltage	V_{IN} = 4.3 V, I_{LDO5} = 10 mA		80	120	
	LDO maximum output current	V_{LDO5} > $V_{UVLO,ON}$	25	40	60	mA
		V_{LDO5} < $V_{UVLO,OFF}$		20	30	
Boost section						
$t_{ON,min}$	Minimum switching on-time				200	ns
f_{SW}	Default switching frequency	FSW connected to AVCC	570	660	750	kHz
	Minimum FSW sync frequency			210		
	FSW sync input threshold		240			mV
	FSW sync low level				350	
	FSW sync input hysteresis			20		
	FSW sync min. ON time				270	ns
	SYNC output Duty-Cycle	FSW connected to AVCC (Internal oscillator selected)		34	40	%
	SYNC output high level	I_{SYNC} = 10 µA	V_{AVCC} -20V			mV
	SYNC output low level	I_{SYNC} = -10 µA			20	

a. Specification referred to T_J from 0 °C to +85 °C. Specification over the 0 to +85 °C T_J range are assured by design, characterization and statistical correlation.

Table 5. Electrical characteristics (continued)

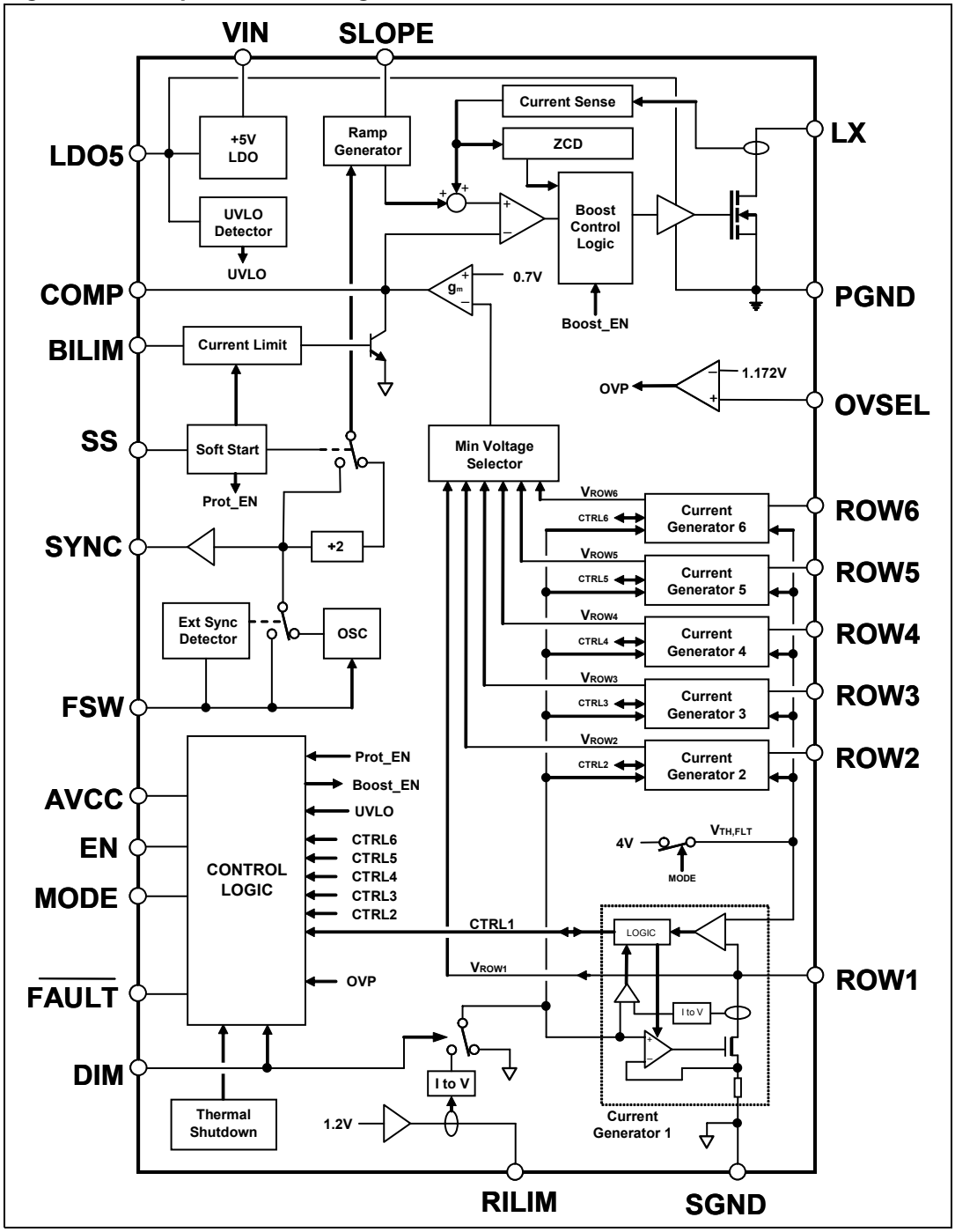
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Power switch						
K_B	LX current coefficient	R_{BILIM} = 600 kΩ	$5 \cdot 10^5$	$6 \cdot 10^5$	$7 \cdot 10^5$	V
R_{DSon}	Internal MOSFET on-resistance			280	500	mΩ
OC and OV protections						
$V_{TH,OVP}$	Over voltage protection reference threshold (OVSEL)		1.190	1.234	1.280	V
$V_{TH,FRD}$	Floating channel detection threshold		1.100	1.145	1.190	
$\Delta V_{OVP,FRD}$	Voltage gap between OVP and FRD thresholds			90		mV
Soft-start and power management						
	EN, Turn-on threshold				1.6	V
	EN, Turn-off threshold		0.8			
	DIM, high level threshold		1.3			
	DIM, low level threshold				0.8	
	EN, pull-up current			2.5		µA
	SS, charge current		4	5	6	
	SS, end-of-startup threshold		2.0	2.4	2.8	V
	SS, reduced switching frequency release threshold			0.8		
Current generators section						
$T_{DIM-ON,min}$	Minimum dimming on-time			500		ns
K_R	Current generators gain			987		V
ΔK_R(1)	Current generators gain accuracy				±2.0	%
V_{IFB}	Feedback regulation voltage			400		mV
$V_{rowx,FAULT}$	Shorted LED fault detection threshold	MODE tied to SGND		3.4		V
		MODE connected to AVCC		6.0		
$V_{FAULT,LOW}$	FAULT pin low-level voltage	$I_{FAULT,SINK}$ = 4 mA		200	350	mV
Thermal shutdown						
T_{SHDN}	Thermal shutdown turn-off temperature			150		°C
	Thermal shutdown hysteresis			30		

1. $I_{ROW} = K_R / R_{RILIM}$, $\Delta I_{ROW}/I_{ROW} \approx \Delta K_R/K_R + \Delta R_{RILIM}/R_{RILIM}$

5 Operation description

The device can be divided into two sections: the boost section and the backlight driver section. These sections are described in the next paragraphs. *Figure 3* provides an overview of the internal blocks of the device.

Figure 3. Simplified block diagram



5.1 Boost section

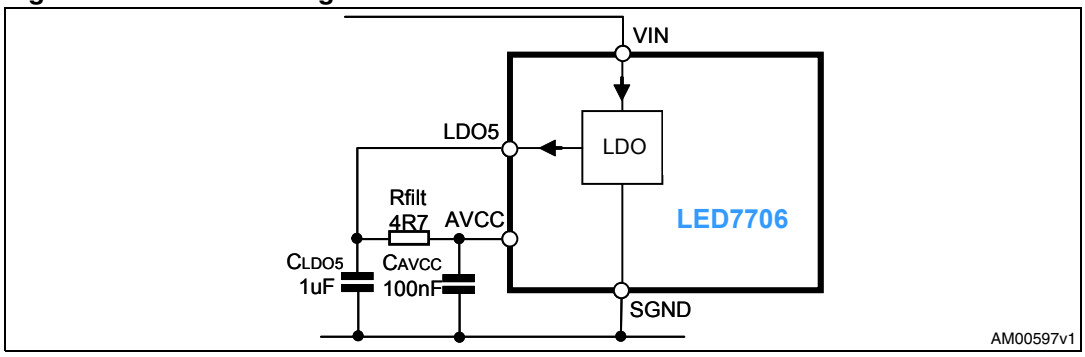
5.1.1 Functional description

The LED7706 is a monolithic LEDs driver for the backlight of LCD panels and it consists of a boost converter and six PWM-dimmable current generators.

The boost section is based on a constant switching frequency, peak current-mode architecture. The boost output voltage is controlled such that the lowest row's voltage, referred to SGND, is equal to an internal reference voltage (400 mV typ. see *Figure 5*). The input voltage range is from 4.5 V up to 36 V. In addition, the LED7706 has an internal LDO that supplies the internal circuitry of the device and is capable to deliver up to 40 mA. The input of the LDO is the VIN pin.

The LDO5 pin is the LDO output and the supply for the power MOSFET driver at the same time. The AVCC pin is the supply for the analog circuitry and should be connected to the LDO output through a simple RC filter in order to improve the noise rejection.

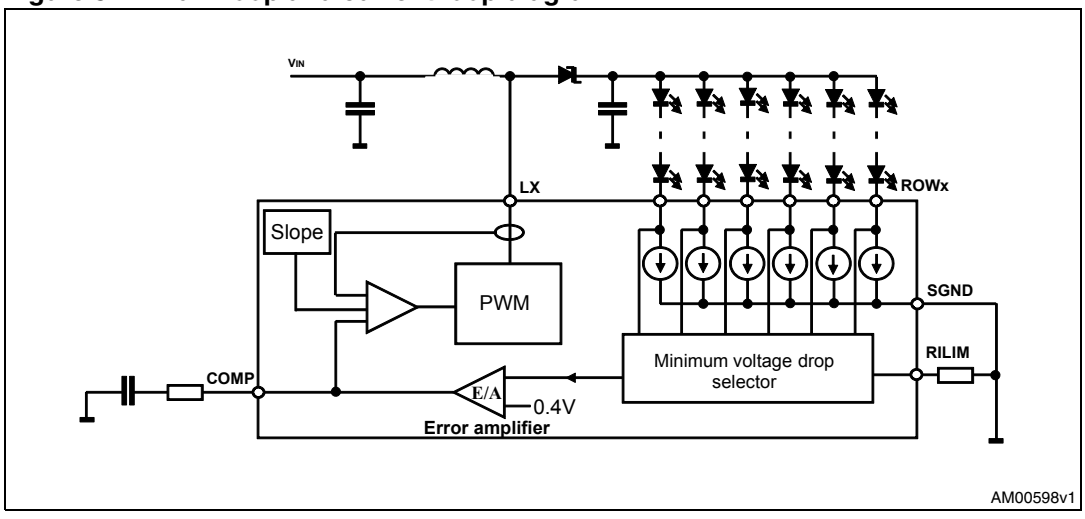
Figure 4. AVCC filtering



Two loops are involved in regulating the current sunk by the generators.

The main loop is related to the boost regulator and uses a constant frequency peak current-mode architecture to regulate the power rail that supplies the LEDs (*Figure 5*), while an internal current loop regulates the same current (flowing through the LEDs) at each row according to the set value (RILIM pin).

Figure 5. Main loop and current loop diagram



A dedicated circuit automatically selects the lowest voltage drop among all the rows and provides this voltage to the main loop that, in turn, regulates the output voltage. In fact, once the reference generator has been detected, the error amplifier compares its voltage drop to the internal reference voltage and varies the COMP output. The voltage at the COMP pin determines the inductor peak current at each switching cycle. The output voltage of the boost regulator is thus determined by the total forward voltage of the LEDs strings (see *Figure 6*):

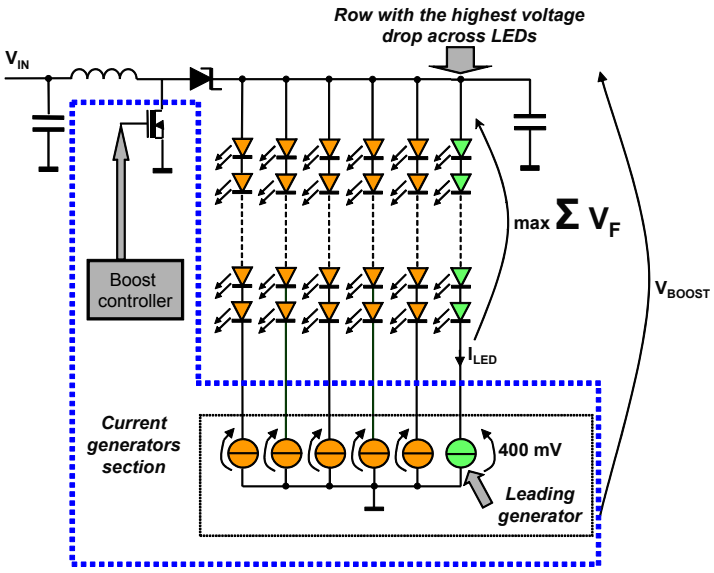
Equation 1

$$V_{OUT} = \max_{i=1}^{N_{ROWS}} \left(\sum_{j=1}^{m_{LEDS}} V_{F,j} \right) + 400mV$$

where the first term represents the highest total forward voltage drop over N active rows and the second is the voltage drop across the leading generator (400 mV typ.).

The device continues to monitor the voltage drop across all the rows and automatically switches to the current generator having the lowest voltage drop.

Figure 6. Calculation of the output voltage of the boost regulator

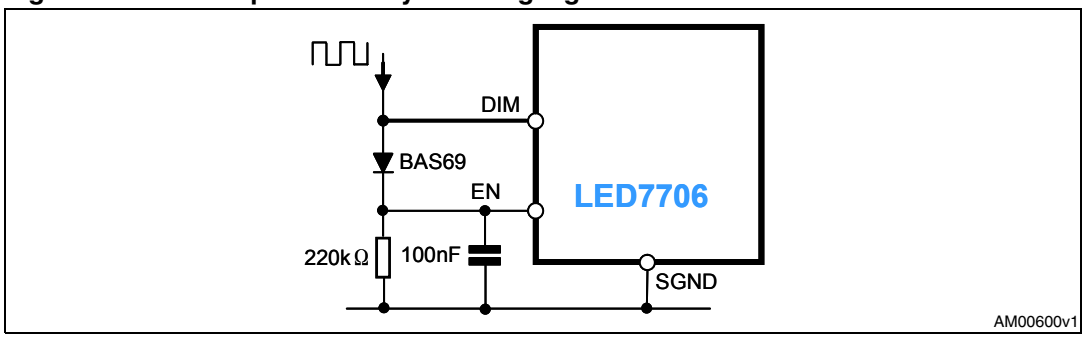


5.1.2 Enable function

The LED7706 is enabled by the EN pin. This pin is active high and, when forced to SGND, the device is turned off. This pin is connected to a permanently active 2.5 µA current source; when sudden device turn-on at power-up is required, this pin must be left floating or connected to a delay capacitor. When turned off, the LED7706 quickly discharges the soft-start capacitor and turns off the power MOSFET, the current generators and the LDO. The power consumption is thus reduced to 20 µA only.

In applications where the dimming signal is used to turn on and off the device, the EN pin can be connected to the DIM pin as shown in *Figure 7*.

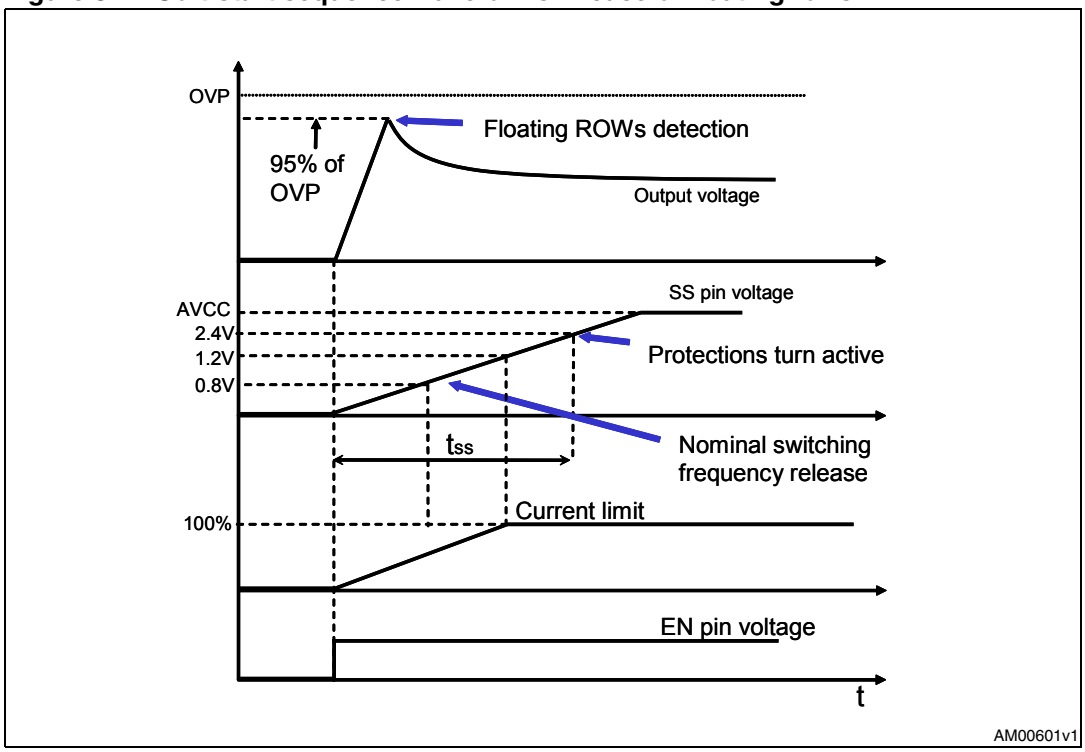
Figure 7. Enable pin driven by dimming signal



5.1.3 Soft-start

The soft-start function is required to perform a correct start-up of the system, controlling the inrush current required to charge the output capacitor and to avoid output voltage overshoot. The soft-start duration is set connecting an external capacitor between the SS pin and ground. This capacitor is charged with a 5 µA (typ.) constant current, forcing the voltage on the SS pin to ramp up. When this voltage increases from zero to nearly 1.2 V, the current limit of the power MOSFET is proportionally released from zero to its final value. However, because of the limited minimum on-time of the switching section, the inductor might saturate due to current runaway. To solve this problem the switching frequency is reduced to one half of the nominal value at the beginning of the soft-start phase. The nominal switching frequency is restored after the SS pin voltage has crossed 0.8 V.

Figure 8. Soft-start sequence waveforms in case of floating rows



During the soft-start phase the floating rows detection is also performed. In presence of one or more floating rows, the voltage across the involved current generator drops to zero. This voltage becomes the inverting input of the error amplifier through the minimum voltage drop

selector (see *Figure 5*). As a consequence the error amplifier is unbalanced and the loop reacts by increasing the output voltage. When it reaches the floating row detection (FRD) threshold (95% of the OVP threshold), the floating rows are managed according to *Table 6* (see *Section 5.3 on page 21*). After the SS voltage reaches a 2.4 V threshold, the start-up finishes and all the protections turn active. The soft-start capacitor C_{SS} can be calculated according to equation 2.

Equation 2

$$C_{SS} \cong \frac{I_{SS} \cdot t_{SS}}{2.4}$$

Where I_{SS} = 5 µA and t_{SS} is the desired soft-start duration.

5.1.4 Overvoltage protection

An adjustable over-voltage protection is available. It can be set feeding the OVSEL pin with a partition of the output voltage. The voltage of the central tap of the divider is thus compared to a fixed 1.234 V threshold. When the voltage on the OVSEL pin exceeds the OV threshold, the FAULT pin is tied low and the device is turned off; this condition is latched and the LED7706 is restarted by toggling the EN pin or by performing a Power-On Reset (the POR occurs when the LDO output falls below the lower UVLO threshold and subsequently crosses the upper UVLO threshold during the rising phase of the input voltage). Normally, the value of the high-side resistors of the divider must be chosen as high as possible (but lower than 1 MΩ) to reduce the output capacitor discharge when the boost converter is off (during the off phase of the dimming cycle). The R2/R1 ratio is calculated to trigger the OVP circuitry as soon as the output voltage is 2 V higher than the maximum value for a given LED string (see equation 3). Two additional filtering capacitors, C_{10} and C_{13}, may be required to improve noise rejection at the OVSEL pin, as shown in *Figure 9*. The typical value for C_{10} is in the 100 pF-330 pF range, while the C_{13} value is given by equation 4.

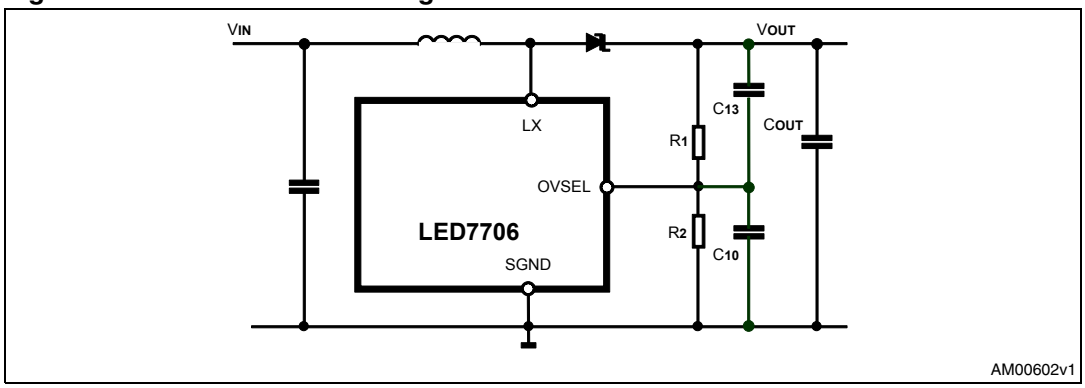
Equation 3

$$R_2 = R_1 \cdot \frac{1.234V}{(V_{OUT,OVP} + 2V - 1.234V)}$$

Equation 4

$$C_{13} = 2 \cdot C_{10} \frac{R_2}{R_1}$$

Figure 9. OVP threshold setting



5.1.5 Switching frequency selection and synchronization

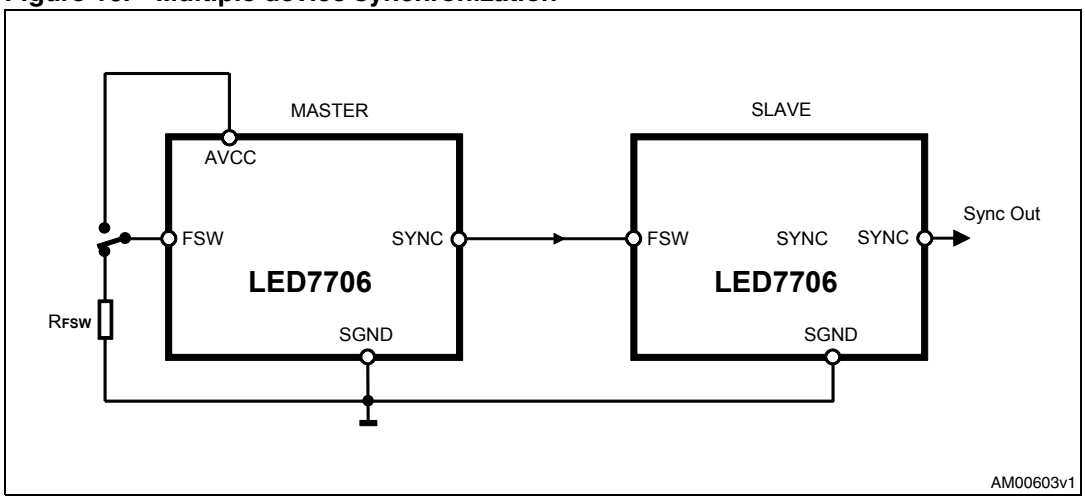
The switching frequency of the boost converter can be set in the 250 kHz-1 MHz range by connecting the FSW pin to ground through a resistor. Calculation of the setting resistor is made using equation 5 and should not exceed the 100 kΩ-400 kΩ range.

Equation 5

$$R_{FSW} = \frac{F_{SW}}{2.5}$$

In addition, when the FSW pin is tied to AVCC, the LED7706 uses a default 660 kHz fixed switching frequency, allowing to save a resistor in minimum component-count applications.

Figure 10. Multiple device synchronization

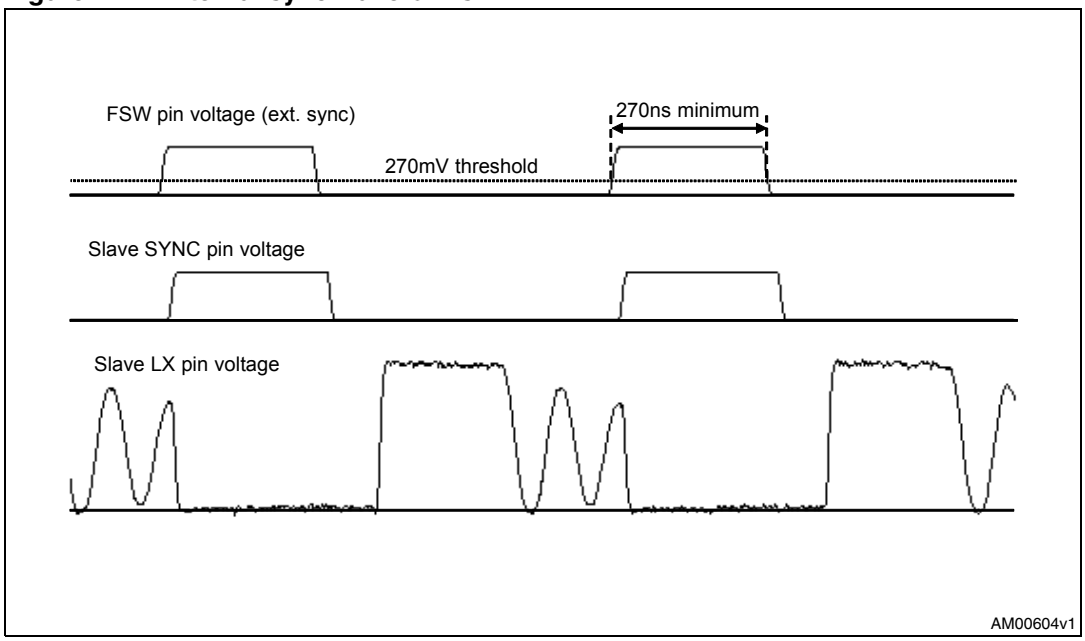


The FSW pin can also be used as synchronization input, allowing the LED7706 to operate both as master or slave device. If a clock signal with a 210 kHz minimum frequency is applied to this pin, the device locks synchronized. The signal provided to the FSW pin must cross the 270 mV threshold in order to be recognized. The minimum pulse width which allows the synchronizing pulses to be detected is 270 ns. An Internal time-out allows synchronization as long as the external clock frequency is greater than 210 kHz.

Keeping the FSW pin voltage lower than 270 mV for more than 4.8 µs results in a stop of the device switching activity. Normal operation is resumed as soon as FSW rises above the mentioned threshold and the soft-start sequence is repeated.

The SYNC pin is a synchronization output and provides a 35 % (typ.) duty-cycle clock when the LED7706 is used as master or a replica of the FSW pin when used as slave. It is used to connect multiple devices in a daisy-chain configuration or to synchronize other switching converters running in the system with the LED7706 (master operation). When an external synchronization clock is applied to the FSW pin, the internal oscillator is over-driven: each switching cycle begins at the rising edge of the clock, while the slope compensation (*Figure 11*) ramp starts at the falling edge of the same signal. Thus, to prevent sub-harmonic instability (see *Section 5.1.6*), the external synchronization clock is required to have a 40 % maximum duty-cycle when the boost converter is working in continuous-conduction mode (CCM) in order to assure that the slope compensation is effective (starts with duty-cycle lower than 40%)

Figure 11. External sync waveforms



5.1.6 Slope compensation

The constant frequency, peak current-mode topology has the advantage of very easy loop compensation with output ceramic caps (reduced cost and size of the application) and fast transient response. In addition, the intrinsic peak-current measurement simplifies the current limit protection, avoiding undesired saturation of the inductor.

On the other side, this topology has a drawback: there is an inherent open loop instability when operating with a duty-ratio greater than 0.5. This phenomenon is known as “Sub-Harmonic Instability” and can be avoided by adding an external ramp to the one coming from the sensed current. This compensating technique, based on the additional ramp, is called “slope compensation”. In *Figure 12*, where the switching duty-cycle is higher than 0.5, the small perturbation ΔI_L dies away in subsequent cycles thanks to the slope compensation and the system reverts to a stable situation.

The SLOPE pin allows to properly set the amount of slope compensation connecting a simple resistor R_{SLOPE} between the SLOPE pin and the output. The compensation ramp starts at 35% (typ.) of each switching period and its slope is given by the following equation:

Equation 6

$$S_E = K_S\left(\frac{V_{OUT} - V_{IN} - V_{BE}}{R_{SLOPE}}\right)$$

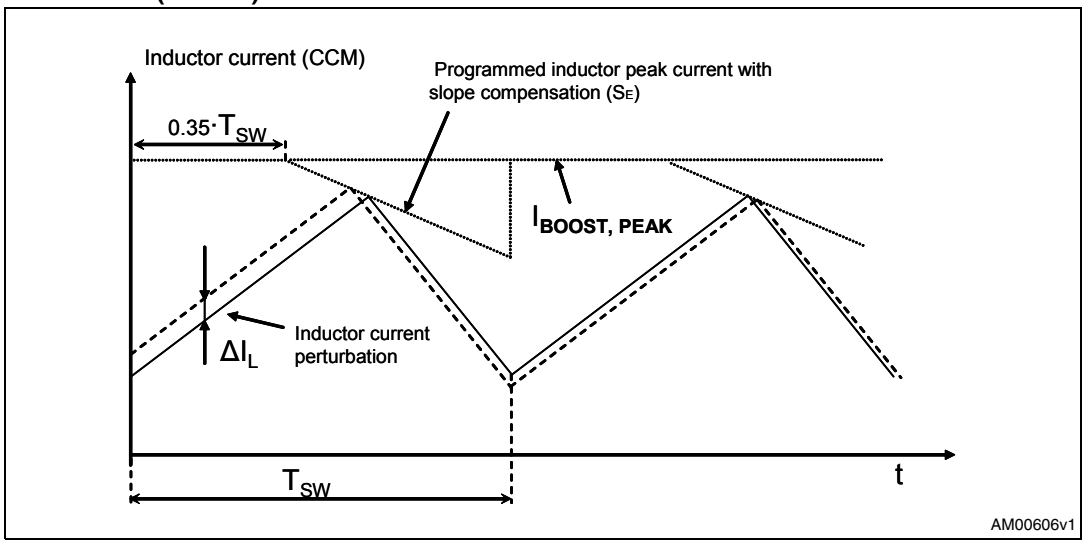
Where KS = 5.8 ·10^{10} s^{-1}, V_{BE} = 2 V (typ.) and S_E is the slope ramp in [A/s].

To avoid sub-harmonic instability, the compensating slope should be at least half the slope of the inductor current during the off-phase when the duty-cycle is greater than 50%. The value of R_{SLOPE} can be calculated according to equation 7.

Equation 7

$$R_{SLOPE} \leq \frac{2 \cdot K_S \cdot L \cdot (V_{OUT} - V_{IN} - V_{BE})}{(V_{OUT} - V_{IN})}$$

Figure 12. Effect of slope compensation on small inductor current perturbation (D > 0.5)



5.1.7 Boost current limit

The design of the external components, especially the inductor and the flywheel diode, must be optimized in terms of size relying on the programmable peak current limit. The LED7706 improves the reliability of the final application giving the way to limit the maximum current flowing into the critical components. A simple resistor connected between the BILIM pin and ground sets the desired value. The voltage at the BILIM pin is internally fixed to 1.23 V and the current limit is proportional to the current flowing through the setting resistor, according to the following equation:

Equation 8

$$I_{BOOST,PEAK} = \frac{K_B}{R_{BILIM}}$$

where

$$K_B = 6 \cdot 10^5 V$$

The maximum allowed current limit is 5 A, resulting in a minimum setting resistor $R_{BILIM} > 120\ k\Omega$. The maximum guaranteed RMS current in the power switch is 2 A.

In a boost converter the RMS current through the internal MOSFET depends on both the input and output voltages, according to equations 9a (DCM) and 9b (CCM).

The current limitation works by clamping the COMP pin voltage proportionally to R_{BILIM}. Peak inductor current is limited to the above threshold decreased by the slope compensation contribution.

Equation 9 a

$$I_{MOS,rms} = \frac{V_{IN} \cdot D}{F_{SW} \cdot L}\sqrt{\frac{D}{3}}$$

Equation 9 b

$$I_{MOS,rms} = I_{OUT}\sqrt{\left(\frac{D}{(1-D)^2} + \frac{1}{12}\left(\frac{V_{OUT}}{I_{OUT} \cdot f_{SW} \cdot L}\right)^2 (D(1-D))^3\right)}$$

5.1.8 Thermal protection

In order to avoid damage due to high junction temperature, a thermal shutdown protection is implemented. When the junction temperature rises above 150 °C (typ.), the device turns off both the control logic and the boost converter and holds the FAULT pin low. The LDO is kept alive and normal operation is automatically resumed after the junction temperature has been reduced by 30 °C.

5.2 Backlight driver section

5.2.1 Current generators

The LED7706 is a LEDs driver with six channels (rows); each row is able to drive multiple LEDs in series (max. 36 V) and to sink up to 30 mA maximum current, allowing to manage different kinds of LEDs.

The LEDs current can be set by connecting an external resistor (R_{RILIM}) between the RILIM pin and ground. The voltage across the RILIM pin is internally set to 1.23 V and the rows current is proportional to the RILIM current according to the following equation:

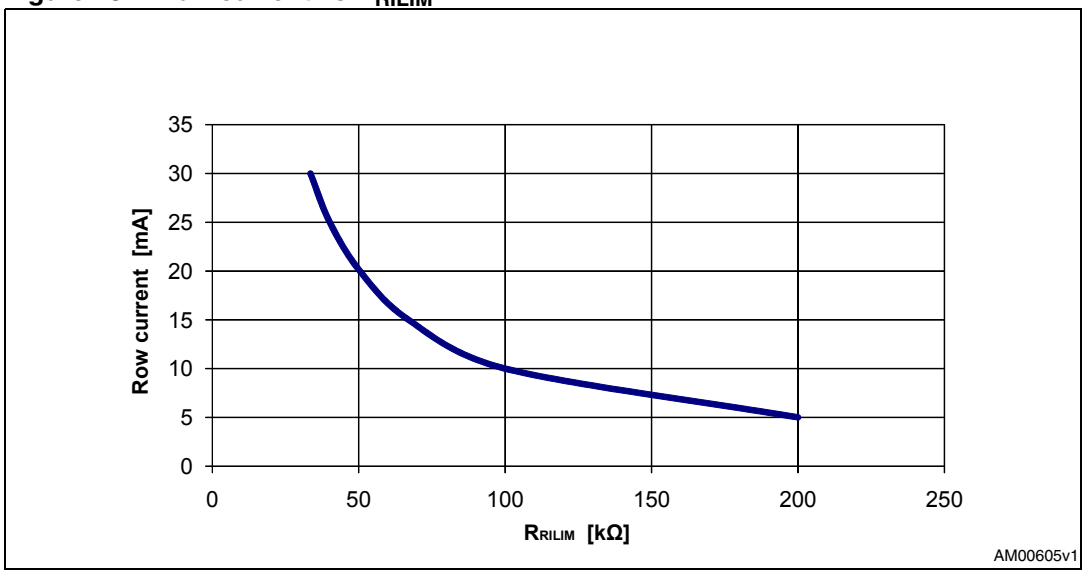
Equation 10

$$I_{ROWx} = \frac{K_R}{R_{RILIM}}$$

Where K_R = 987 V.

The graph in *Figure 13* better shows the relationship between I_{ROW} and R_{RILIM} and helps to choose the correct value of the resistor to set the desired row current.

Figure 13. Row current vs R_{RILIM}



The maximum current mismatch between the rows is ± 2 % @ I_{rowx} = 20 mA.

5.2.2 PWM dimming

The brightness control of the LEDs is performed by a pulse-width modulation of the rows current. When a PWM signal is applied to the DIM pin, the current generators are turned on and off mirroring the DIM pin behavior. Actually, the minimum dimming duty-cycle depends on the dimming frequency.

The real limit to the PWM dimming is the minimum on-time that can be managed for the current generators; this minimum on-time is approximately 500 ns.

Thus, the minimum dimming duty-cycle depends on the dimming frequency according to the following formula:

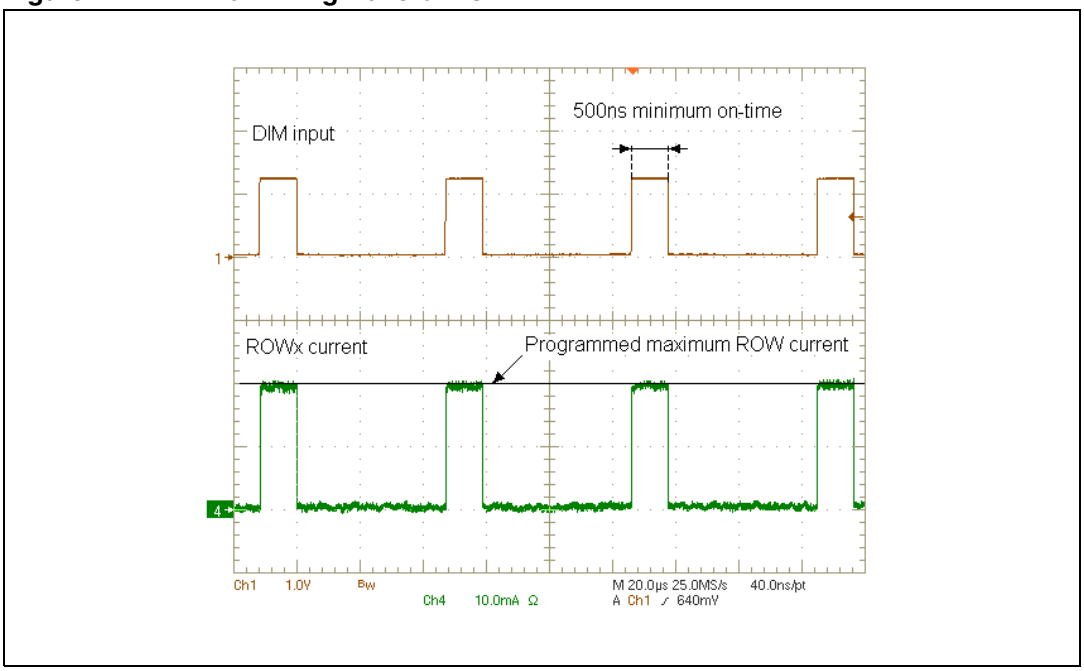
Equation 11

$$D_{DIM,min} = 500ns \cdot f_{DIM}$$

For example, at a dimming frequency of 20 kHz, 1% of dimming duty-cycle can be managed.

During the off-phase of the PWM signal the boost converter is paused and the current generators are turned off. The output voltage can be considered almost constant because of the relatively slow discharge of the output capacitor. During the start-up sequence (see *Section 5.1.3 on page 13*) the dimming duty-cycle is forced to 100% to detect floating rows regardless of the applied dimming signal.

Figure 14. PWM dimming waveforms



5.3 Fault management

The main loop keeps the row having the lowest voltage drop regulated to about 400 mV. This value slightly depends on the voltage across the remaining active rows. After the soft-start sequence, all protections turn active and the voltage across the active current generators is monitored to detect shorted LEDs.

5.3.1 FAULT pin

The FAULT pin is an open-collector output, (with 4 mA current capability) active low, which gives information regarding faulty conditions eventually detected. This pin can be used either to drive a status LED or to warn the host system.

The FAULT pin status is strictly related to the MODE pin setting (see *Table 6* for details).

5.3.2 MODE pin

The MODE pin is a digital input and can be connected to AVCC or SGND in order to choose the desired fault detection and management. The LED7706 can manage a faulty condition in two different ways, according to the application needs. *Table 6* summarizes how the device detects and handles the internal protections related to the boost section (over-current, over-temperature and over-voltage) and to the current generators section (open and shorted LEDs).

Table 6. Faults management summary

FAULT	MODE to GND	MODE to VCC
Internal MOSFET over current	FAULT pin HIGH Power MOS turned OFF	
Output over voltage	FAULT pin LOW Device turned OFF, latched condition	
Thermal shutdown	FAULT pin LOW. Device turned OFF. Automatic restart after 30 C temperature drop.	
LED short shorted led	FAULT pin LOW Device turned OFF, latched condition (Vth = 3.4 V)	FAULT pin LOW Faulty row(s) disconnected Device keeps on working with the remaining row(s) (Vth = 6 V)
Open row(s)	FAULT pin LOW Device turned OFF at first occurrence, latched condition	FAULT pin HIGH Faulty row(s) disconnected. Device keeps on working with the remaining row(s)

5.3.3 Open LED fault

In case a row is not connected or a LED fails open, the device has two different behaviors according to the MODE pin status.

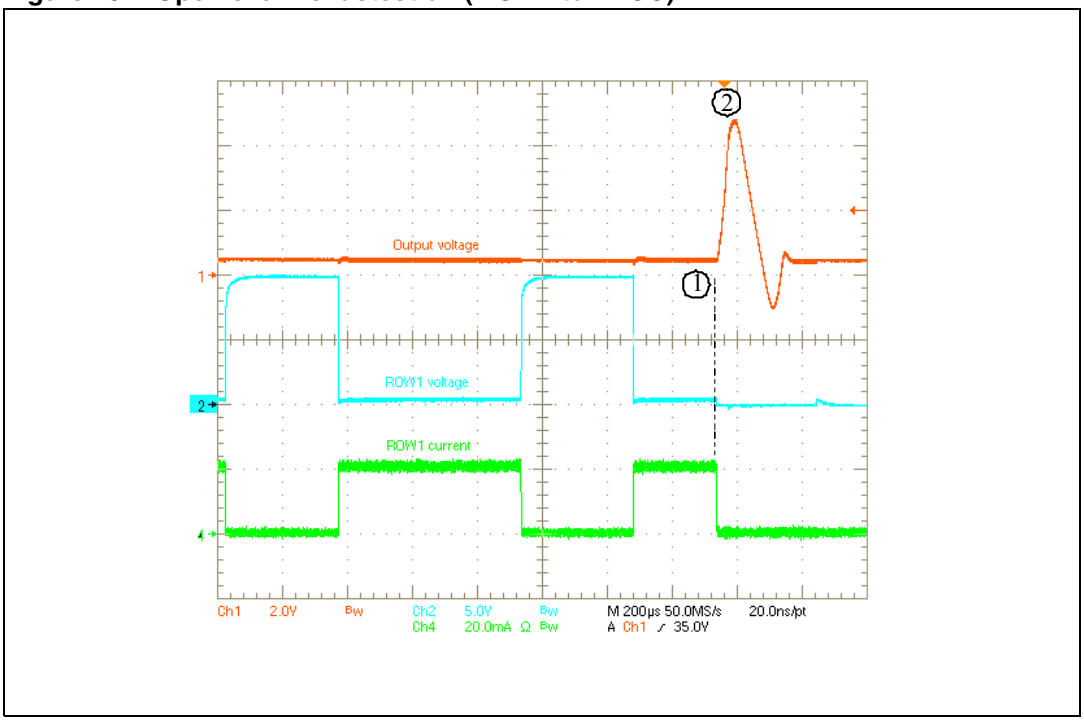
Connecting the MODE pin to SGND, as soon as an open row is detected the FAULT pin is tied low and the device is turned off. The internal logic latches this status: to restore the normal operation, the device must be restarted by toggling the EN pin or performing a Power-On Reset (POR occurs when the voltage at the LDO5 pin falls below the lower UVLO threshold and subsequently rises above the upper one).

If the MODE pin is high (i.e. connected to AVCC), the LED7706 behaves in a different manner: the open row is excluded from the control loop and the device continues to work properly with the remaining rows. The FAULT pin is not affected. Thus, if less than six rows are used in the application, the MODE pin must be set high.

Figure 15 shows an example of open channel detection in case of MODE connected to AVCC.

At the point marked as “1” in *Figure 15*, the row opens (row current drops to zero). From this point on the output voltage is increased as long as the output voltage reaches the floating row detection threshold (see *Section 5.1.3 on page 13*). Then (point marked as “2”) the faulty row is disconnected and the device keeps on working only with the remaining rows.

Figure 15. Open channel detection (MODE to AVCC)



5.3.4 Shorted LED fault

When a LED is shorted, the voltage across the related current generator increases of an amount equal to the missing voltage drop of the faulty LED. Since the feedback voltage on each active generator is constantly compared with a fault threshold $V_{TH,FAULT}$, the device detects the faulty condition and acts according to the MODE pin status.

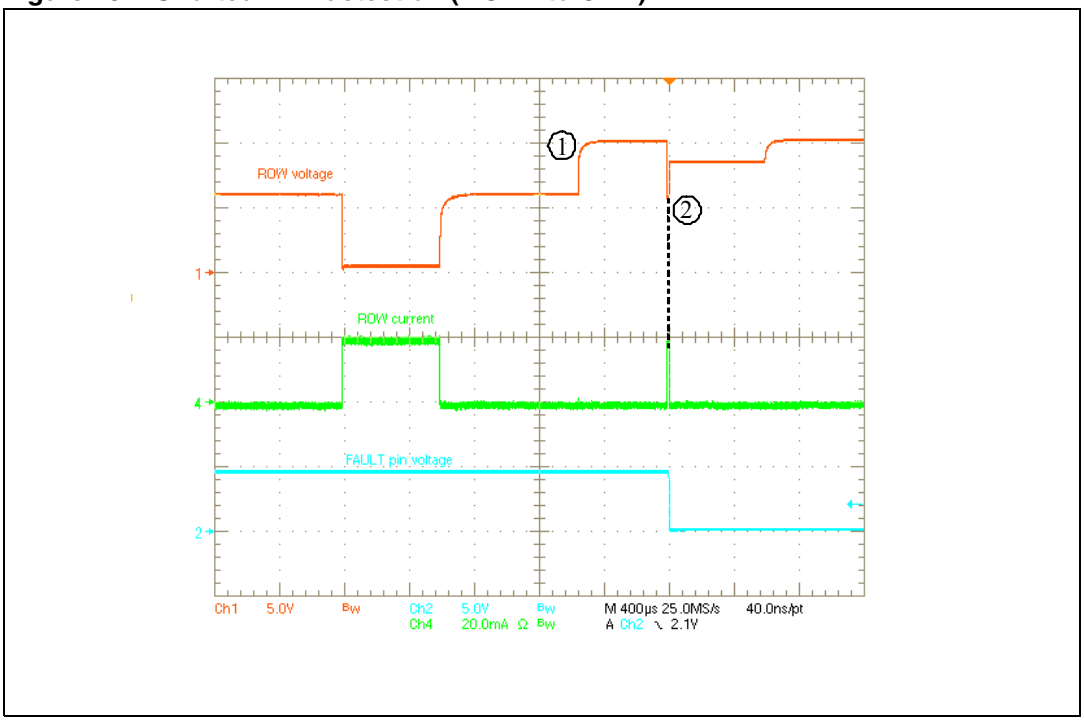
If the MODE pin is low, the fault threshold is $V_{TH,FAULT}$ = 3.4 V. When the voltage across a row is higher than this threshold, the FAULT pin is set low and the device is turned off. The internal logic latches this status until the EN pin is toggled or a POR is performed.

In case the MODE pin is connected to AVCC, the fault threshold is set to 6 V. The LED7706 simply disconnects the rows whose voltage is higher than the threshold and the FAULT pin is forced low. This option is also useful to avoid undesired triggering of the shorted-LED protection simply due to the high voltage drop spread across the LEDs.

Figure 16 shows an example of shorted LED detection in case MODE is connected to GND.

At the point marked as “1” in *Figure 16* one LED fails becoming a short-circuit. The voltage across the current generator of the channel where the failed LED is connected increases by an amount equal to the forward voltage of the faulty LED. Since the voltage across the current generator is above the threshold (3.4 V in this case), the device is turned off and the fault pin is set low (point “2”).

Figure 16. Shorted LED detection (MODE to GND)



6 Application information

6.1 System stability

The boost section of the LED7706 is a fixed frequency, current-mode converter. During normal operation, a minimum voltage selection circuit compares all the voltage drops across the active current generators and provides the minimum one to the error amplifier. The output voltage of the error amplifier determines the inductor peak current in order to keep its inverting input equal to the reference voltage (400 mV typ). The compensation network consists of a simple RC series (R_{COMP} - C_{COMP}) between the COMP pin and ground.

The calculation of R_{COMP} and C_{COMP} is fundamental to achieve optimal loop stability and dynamic performance of the boost converter and is strictly related to the operating conditions.

6.1.1 Loop compensation

The compensation network can be quickly calculated using equations 12 to 16. Once both R_{COMP} and C_{COMP} have been determined, a fine-tuning phase may be required in order to get the optimal dynamic performance from the application.

The first parameter to be fixed is the switching frequency. Normally, a high switching frequency allows reducing the size of the inductor and positively affects the dynamic response of the converter (wider bandwidth) but increases the switching losses. For most of applications, the fixed value (660 kHz) represents a good trade-off between power dissipation and dynamic response, allowing to save an external resistor at the same time. In low-profile applications, the inductor value is often kept low to reduce the number of turns; an inductor value in the 4.7 µH-15 µH range is a good starting choice.

In order to avoid instability due to interaction between the DC-DC converter's loop and the current generators' loop, the bandwidth of the boost should not exceed the bandwidth of the current generators. A unity-gain frequency (f_U) in the order of 30-40 kHz is acceptable. Also, take care not to exceed the CCM-mode right half-plane zero (RHPZ).

Equation 12

$$f_U \leq 0.2 \cdot F_{SW}$$

Equation 13

$$f_U \leq 0.2 \cdot \frac{M^2 R}{2\pi \cdot L} = 0.2 \cdot \frac{\left(\frac{V_{IN,min}}{V_{OUT}}\right)^2 \left(\frac{V_{OUT}}{I_{OUT}}\right)}{2\pi \cdot L}$$

Equation 14 a

$$M = \frac{V_{IN,min}}{V_{OUT}}$$

Equation 14b

$$R = \frac{V_{OUT}}{I_{OUT}}$$

Where $V_{IN,min}$ is the minimum input voltage and I_{OUT} is the overall output current.

Note that, the lower the inductor value (and the higher the switching frequency), the higher the bandwidth can be achieved. The output capacitor is directly involved in the loop of the boost converter and must be large enough to avoid excessive output voltage drop in case of a sudden line transition from the maximum to the minimum input voltages.

However a more significant requirement concerns the output voltage ripple.

The output capacitor should be chosen in accordance with the following expression:

Equation 15

$$C_{OUT} > \frac{\left(I_{L,peak} - I_{OUT}\right) \cdot T_{OFF}}{2 \cdot \Delta V_{OUT,max}}$$

where $\Delta V_{OUT,\,max}$ is the maximum acceptable output voltage ripple, $I_{L,\,peak}$ is the peak inductor current, T_{OFF} is the off-time of the switching cycle (for an extensive explanation see *Section 6.4.4 on page 31*).

Once the output capacitor has been chosen, the R_{COMP} can be calculated as:

Equation 16

$$R_{COMP} = \frac{2\pi \cdot f_U \cdot C}{G_M \cdot g_{EA} \cdot M}$$

Where G_M = 2.7 S and g_{EA} = 375 µS

Equation 16 places the loop bandwidth at f_U. Then, the C_{COMP} capacitor is determined to place the frequency of the compensation zero 5 times lower than the loop bandwidth:

Equation 17

$$C_{COMP} = \frac{1}{2\pi \cdot f_Z \cdot R_{COMP}}$$

Where f_Z=f_U/5.

In most of the applications an experimental approach is also very valid to compensate the circuit. A simple technique to optimize different applications is to choose C_{COMP} = 4.7 nF and to replace R_{COMP} with a 10 kΩ trimmer adjusting its value to properly damp the output transient response. Insufficient damping will result in excessive ringing at the output and poor phase margin.

Figure 17 (a and b) give an example of compensation adjustment for a typical application.

Figure 17. Poor phase margin (a) and properly damped (b) load transient responses

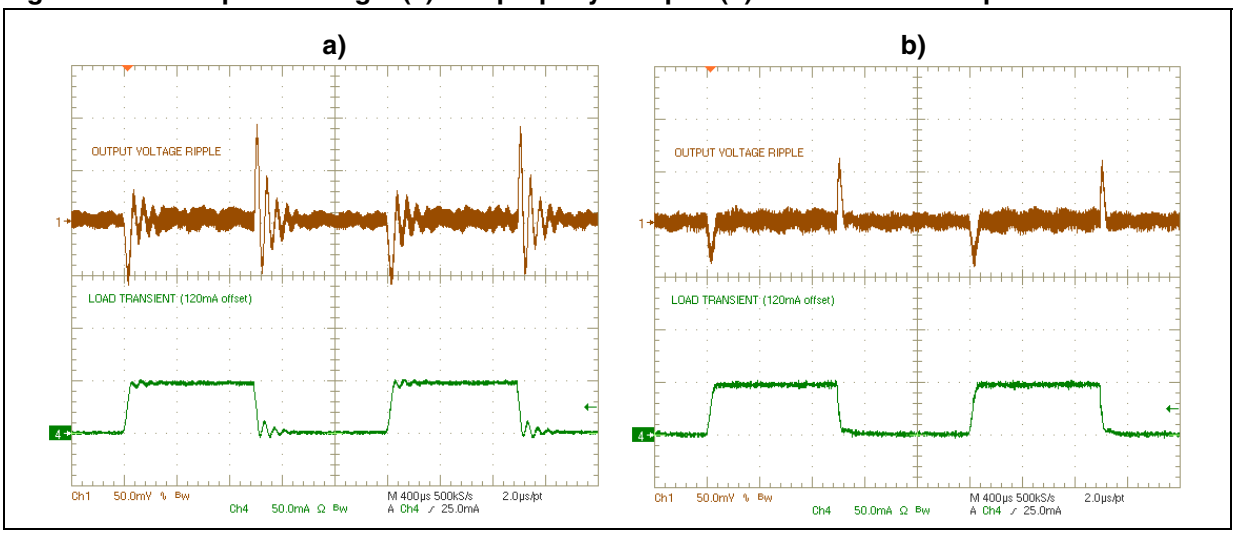
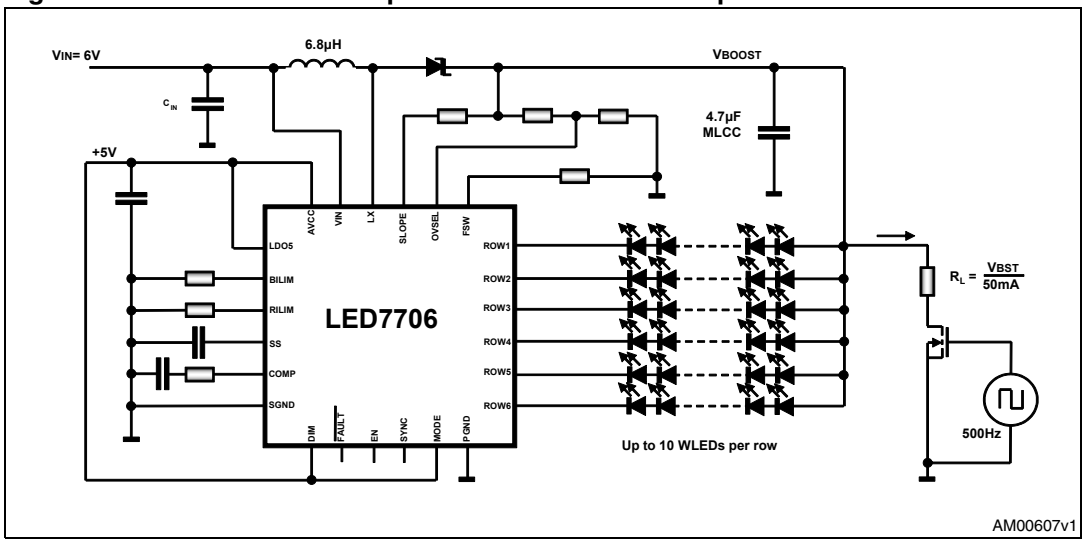


Figure 18. Load transient response measurement set-up



6.2 Thermal considerations

In order to prevent the device from exceeding the thermal shutdown threshold (150 °C), it is important to estimate the junction temperature through the following equation:

Equation 18

$$T_J = T_{Amb} + R_{th,JA} \cdot P_{D,tot}$$

where T_A is the ambient temperature, $R_{th,JA}$ is the equivalent thermal resistance junction to ambient and $P_{D,tot}$ is the power dissipated by the device.

The $R_{th,JA}$ measured on the application demonstration board (described in *Section 6.5*) is 42 °C/W.

The $P_{D,tot}$ has several contributions, listed below.

a) Conduction losses due to the $R_{DS(on)}$ of the internal power switch, equal to:\

Equation 19

$$P_{D,cond} = R_{DSon} \cdot I_{IN}^2 \cdot D \cdot D_{DIM}$$

where D is defined as:

Equation 20

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

and D_{DIM} is the duty cycle of the PWM dimming signal.

b) Switching losses due to the power MOSFET turn on and off, calculated as:

Equation 21

$$P_{D,sw} = V_{OUT} \cdot I_{IN} \cdot f_{sw} \cdot \frac{(t_r + t_f)}{2} \cdot D_{DIM}$$

where t_r and t_f are the power MOSFET rise time and fall time respectively.

c) Current generators losses. This contribution is strictly related to the LEDs used in the application. Only the contribution of the leading current generator (“master” current generator) can be predicted, regardless of the LEDs forward voltage:

Equation 22

$$P_{GEN,Master} = I_{ROW} \cdot V_{IFB} \cdot D_{DIM}$$

where I_{ROW} is the current flowing through the row, whereas V_{IFB} is the voltage across the master current generator (typically 400 mV).

The voltages across the other current generators depend on the spread of the LEDs forward voltage. The worst case for power dissipation (maximum forward voltage LEDs in the master row, minimum forward voltage LEDs in all other rows) can be estimated as:

Equation 23

$$P_{GEN} = I_{ROW} \cdot (n_{ROWs} - 1) \cdot (V_{IFB} + \Delta V_{f,LEDs} \cdot n_{LEDs}) \cdot D_{DIM}$$

where n_{ROWs} is the number of active rows, $\Delta V_{f,LEDs}$ is the spread of the LEDs forward voltage and n_{LEDs} is the number of LEDs per row.

d) LDO losses, due to the dissipation of the 5 V linear regulator:

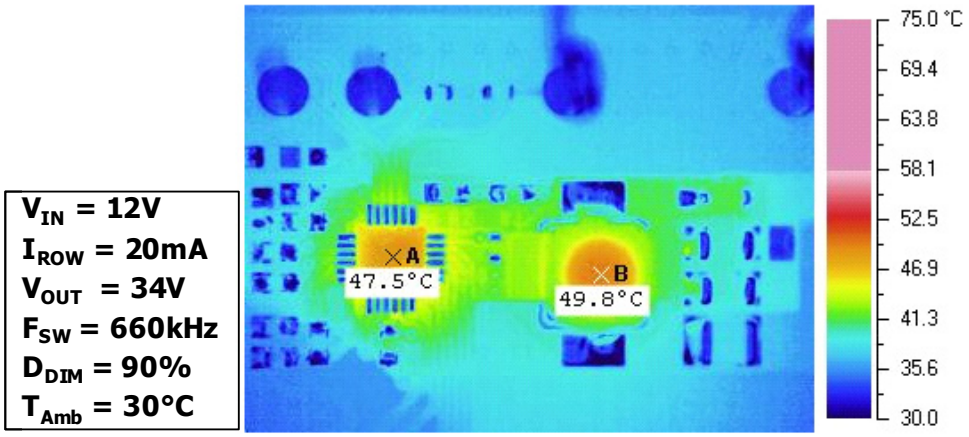
Equation 24

$$P_{D,LDO} = (V_{IN} - V_{LDO}) \cdot I_{LDO}$$

The LED7706 is housed in a 24 leads 4x4-VFQFPN package with exposed pad that allows good thermal performance. However it is also important to design properly the demonstration board layout in order to assure correct heat dissipation.

Figure 19 shows a picture of the LED7706 application demonstration board taken using an infrared camera. The chip temperature, in those application conditions, is kept below 50 °C.

Figure 19. Demonstration board thermographic analysis



6.3 Component selection

6.3.1 Inductor selection

Being the LED7706 mostly dedicated to backlighting, real-estate applications dictate severe constrain in selecting the optimal inductor. The inductor choice must take into account different parameters like conduction losses (DCR), core losses (ferrite or iron-powder), saturation current and magnetic-flux shielding (core shape and technology).

The switching frequency of the LED7706 can be set in the 200 kHz-1 MHz range, allowing a wide selecting room for the inductance value. Low switching frequencies takes to high inductance value, resulting in significant DCR and size. On the other hand, high switching frequencies result in significant core losses. The suggested range is 4.7-22 µH, even if the

best trade off between the different loss contributions varies from manufacturer to manufacturer.

A 6.8 µH inductor has been experimentally found as the most suitable for applications running at a 660 kHz switching frequency.

Table 7. Recommended inductors

Manufacturer	Part number	Description	Size
Coilcraft	LPS6235-682MLC	6.8 µH, 75 mΩ, 2.7 A	6x6 mm
Wurth	7440650068	6.8 µH, 33 mΩ, 3.6 A	10x10 mm

6.3.2 Capacitors selection

The input and output capacitors should have very low ESR (ceramic capacitors) in order to minimize the ripple voltage. The boost converter of the LED7706 has been designed to support ceramic capacitors. The required capacitance depends on the programmed LED current and the minimum dimming frequency (the boost converter is off when the DIM pin is low and the output capacitor is slowly discharged). Considering the worst case (i.e. 200 Hz dimming frequency and 30 mA/channel), two 2.2 µF MLCCs are suitable for almost all applications. Particular care must be taken when selecting the rated voltage and the dielectric type of the output capacitors: 50 V rated MLCC may show a significant capacitance drop when biased, especially in case of Y5V dielectric.

As in most of boost converters, the input capacitor is less critical, although it is necessary to reduce the switching noise on the supply rail. The input capacitor is also important for the internal LDO of the LED7706 and must be kept as close as possible to the chip. The rated voltage of the input capacitor can be chosen according to the supply voltage range; a 10 µF X5R MLCC is recommended.

Table 8. Recommended capacitors

Manufacturer	Part number	Description	Package	Notes
Taiyo Yuden	UMK325BJ106KM-T	Ceramic, 35V, X5R, 20 %	SMD 1210	C_{IN}
Murata	GRM31CR71H225KA88B	Ceramic, 50V, X7R, 20 %	SMD 1206	C_{OUT}
Murata	GRM31CR71H475KA88B	Ceramic, 50V, X7R, 20 %	SMD 1206	C_{OUT}

6.3.3 Flywheel diode selection

The flywheel diode must be a Schottky type to minimize the losses. This component is subject to an average current equal to the output one and must sustain a reverse voltage equal to the maximum output rail voltage. Considering all the channels sinking 30mA each (i.e. 180 mA output current) and the maximum output voltage (36 V), the STP1L40M ($I_{f,ave}$ = 1 A, V_r = 40 V) diode is a good choice. Smaller diodes can be used in applications involving lower output voltage and/or lower output current.

6.4 Design example

In order to help the design of an application using the LED7706, in this section a simple step-by-step design example is provided.

A possible application could be the LED backlight in a 15” LCD panel using the LED7706.

Here below the possible application conditions are listed:

- V_{IN} = 12 ± 20 %
- 2 strings of 48 white LEDs (20 mA) each (arranged in 6 rows, 8 LEDs per row)
- $V_{F, LEDs}$ = 3.5 V ± 200 mV

6.4.1 Switching frequency setting

To reduce the number of the external components, the default switching frequency is selected (660 kHz typ.) by connecting the FSW pin to AVCC pin.

However, in case a different switching frequency is required, a resistor from FSW pin and ground can be connected, according to the equation (5) in *Section 5.1.5*.

6.4.2 Row current setting

Considering the equation 10 in *Section 5.2.1*, the R_{RILIM} resistor can be calculated as:

Equation 25

$$R_{RILIM} = \frac{K_R}{I_{ROW}} = \frac{987 \quad V}{20 \quad mA} = 49.35k\Omega$$

The closest standard commercial value is 51 kΩ. The actual value of the row current will be a little lower (19.3 mA).

6.4.3 Inductor choice

The boost section, as all DC-DC converters, can work in CCM (continuous conduction mode) or in DCM (discontinuous conduction mode) depending on load current, input and output voltage and other parameters, among which the inductor value.

In a boost converter it is usually preferable to work in DCM.

Once the load, the input and output voltage, and the switching frequency are fixed, the inductor value defining the boundary between DCM and CCM operation can be calculated as:

Equation 26

$$L_B = \frac{R_0 \cdot D \cdot (1-D)^2}{2 \cdot F_{SW}}$$

where D is the duty-cycle defined as:

Equation 27

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = \begin{cases} 0.68 & @ \quad V_{IN,min} = 9.6V \\ 0.52 & @ \quad V_{IN,max} = 14.4V \end{cases}$$

whereas R_0 is:

Equation 28

$$R_0 = \frac{V_{OUT}}{I_{OUT}} = 250\Omega$$

and

Equation 29

$$I_{OUT} = 6 \cdot I_{ROW} = 120mA$$

The output voltage in the above calculations is considered as the maximum value (LED with the maximum forward voltage connected to the leading generator):

Equation 30

$$V_{OUT,max} = 8 \cdot V_{F,LEDs,max} + 400mV = 30V$$

Considering the input voltage range, the lower L_B will be at the lower input voltage. Hence the condition to assure the DCM operation becomes:

Equation 31

$$L < L_B(V_{IN,min}) = 13.2\mu H$$

An inductor value of 6.8 µH could be a suitable value, considering also a margin from the boundary condition.

It is important to highlight that the inductor choice involves not only the value itself but the saturation current (higher than the current limit, see *Section 6.4.4*), the rated RMS current (the compliance with the saturation current might be not enough; also the thermal performances must be taken into account), the DCR (which affects the efficiency) and the size (in some application might be a strict requirement).

However the DCR can't be reduced keeping the size small. Hence a trade off between these two requirements must be achieved according to the application.

6.4.4 Output capacitor choice

The choice of the output capacitor is mainly affected by the desired output voltage ripple.

Since the voltage across the LEDs can be considered almost constant, this ripple is transferred across the current generators, affecting their dynamic response.

The output ripple can be estimated as (neglecting the contribution of ESR of C_{OUT}, very low in case of MLCC):

Equation 32

$$\Delta V_{OUT} = \frac{(I_{L,peak} - I_{OUT}) \cdot T_{OFF}}{2 \cdot C_{OUT}}$$

where $I_{L,\,peak}$ is the inductor peak current (see *Figure 20*) calculated as:

Equation 33

$$I_{L,peak} = \frac{V_{IN} \cdot D}{F_{sw} \cdot L} = \begin{cases} 1.044A & @ \quad V_{IN,min} = 9.6V \\ 0.914A & @ \quad V_{IN,max} = 14.4V \end{cases}$$

whereas D, working in DCM, is:

Equation 34

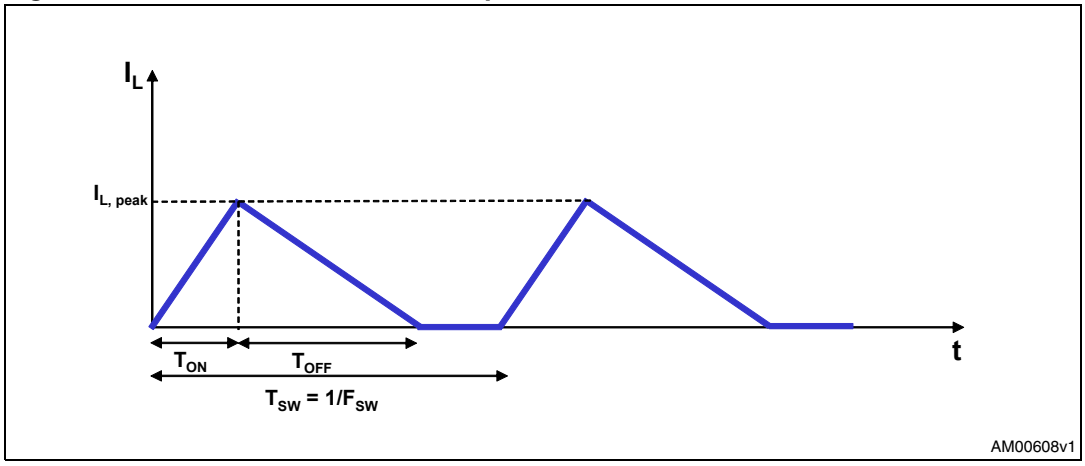
$$D = \sqrt{\frac{2 \cdot F_{sw} \cdot L \cdot M(M-1)}{R_0}} = \begin{cases} 0.488 & @ \quad V_{IN,min} = 9.6V \\ 0.285 & @ \quad V_{IN,max} = 14.4V \end{cases}$$

defining M as:

Equation 35

$$M = \frac{V_{OUT}}{V_{IN}} \begin{cases} 3.125 & @ \quad V_{IN,min} = 9.6V \\ 2.083 & @ \quad V_{IN,max} = 14.4V \end{cases}$$

Figure 20. Inductor current in DCM operation



T_{OFF} can be calculated as:

Equation 36

$$T_{OFF} = T_{SW} \cdot D_2 = \begin{cases} 348.5ns & @ \quad V_{IN,min} = 9.6V \\ 398.5ns & @ \quad V_{IN,max} = 14.4V \end{cases}$$

defining D_2 as:

Equation 37

$$D_2 = \sqrt{\frac{2 \cdot F_{SW} \cdot L \cdot M}{R_0 \cdot (M-1)}} = \begin{cases} 0.23 & @ \quad V_{IN,min} = 9.6V \\ 0.263 & @ \quad V_{IN,max} = 14.4V \end{cases}$$

The worst case for the output voltage ripple is when input voltage is lower ($V_{IN,min}$ = 9.6 V).

A simple way to select the C_{OUT} value is fixing a maximum voltage ripple.

In order to affect as less as possible the current generators, it would be better to fix the maximum ripple lower than the typical voltage across the generators.

For example considering ΔV_{OUT} lower than 80 mV (i.e. the 20 % of the voltage across the leading generator), the required capacitance is:

Equation 38

$$C_{OUT} > \frac{(I_{L,peak} - I_{OUT}) \cdot T_{OFF}}{2 \cdot \Delta V_{OUT,max}} = 2.02\mu F$$

A margin from the calculated value should be taken into account because of the capacitance drop due to the applied voltage when MLCCs are used.

A 4.7 µF MLCC can be a good choice for this application (two 2.2 µF MLCC in parallel can be also a good solution).

In case a dimming duty cycle different from 100 % is used, a further contribution to the capacitor discharge (during the off time of the dimming cycle) should be considered.

6.4.5 Input capacitor choice

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input, and hence, the input current waveform is continuous.

A low ESR capacitor is always recommended.

A capacitor of 10 µF is tentatively a good choice for most of the applications.

6.4.6 Over-voltage protection divider setting

The over-voltage protection (OVP) divider provides a partition of the output voltage to the OVSEL pin. The OVP divider setting not only fixes the OVP threshold, but also the open-channel detection threshold (95 % of the OVP threshold).

The proper OVP divider setting can be calculated by the equation (3):

Equation 39

$$R_2 = R_1 \cdot \frac{1.234V}{(V_{OUT,MAX} + 2V - 1.234V)}$$

where $V_{OUT, MAX}$ is the maximum output voltage considering the worst case (all LEDs with the maximum $V_F = V_{F,max}$ = 3.7 V on the same row):

Equation 40

$$V_{OUT,OVP} = nLED \cdot V_{F,max} + 400mV = 30V$$

R_1 can be chosen is in the order of hundreds of kilo-ohms to reduce the leakage current in the resistor divider. For example, setting R_1 = 510 kΩ leads to R_2 = 21.89 kΩ. The closest standard commercial value is R_2 = 22 kΩ.

The correct selection of the OVP divider (and, as consequence, the open channel detection threshold) must take into account the shorted LED fault threshold (see *Section 5.3.4*).

When the selected OVP threshold is too high, an undesired triggering of the shorted LED detection circuitry may occur when a channel opens.

In fact, as explained in section 4.3.3, once a channel opens, the device reacts increasing the output voltage and the voltage across the working current generators may reach the shorted LED detection threshold before the open channel detection threshold.

6.4.7 Compensation network

For the compensation network, the suggestions provided in *Section 6.1* are always valid.

In this condition, tentatively the following value of R3 and C8 (see *Figure 23*) are usually a good choice for the loop stability:

R_3 = 2.4 kΩ

C_8 = 4.7 nF

6.4.8 Boost current limit

The boost current limit is set to protect the internal power switch against excessive current. The slope compensation may reduce the programmed current limit. Hence, to take into account this effect, as a rule of thumb, the current limit can be set as twice as much the maximum inductor peak current (see *Section 6.4.4*):

$I_{BOOST, PEAK}$ > 2.09 A

Therefore, using equation (8) and choosing $I_{BOOST, PEAK}$ = 2.5 A, R_{BILIM} will be:

Equation 41

$$R_{BILIM} = \frac{K_B}{I_{BOOST,PEAK}} = 240k\Omega$$

6.4.9 Power dissipation estimate

As explained in *Section 6.2*, there are several contributions to the total power dissipation.

Neglecting the power dissipated by the LDO (surely less significant compared with the other contributions), equation (19), (21), (22) and (23) help to estimate the overall power dissipation.

Before starting the power dissipation estimate it is important to highlight that the following calculations are considering the worst case (the actual value of the dissipated power would require measurements). Therefore the power dissipation is estimated according to the following assumptions:

1. Minimum input voltage (9.6 V), which leads to maximum input current (and also D will have the higher value, see *Section 6.4.4*);
2. Maximum $R_{DS(on)}$ of the internal power MOSFET;
3. LEDs in the row of the leading generator will have the maximum forward voltage, whereas all other LEDs in the other rows will have the minimum forward voltage.
4. 100 % dimming signal duty cycle is considered.

The conduction and switching losses on the internal power switch can be calculated as:

Equation 42

$$P_{D,cond} = R_{DSon} \cdot I_{IN}^2 \cdot D \cdot D_{DIM} = 34mW$$

Equation 43

$$P_{D,sw} = V_{OUT} \cdot I_{IN} \cdot f_{sw} \cdot \frac{(t_r + t_f)}{2} \cdot D_{DIM} = 111mW$$

where $t_r = t_f = 15$ ns

The power dissipation related to the current generators is given by:

Equation 44

$$P_{GEN,Master} = I_{ROW} \cdot V_{IFB} \cdot D_{DIM} = 8mW$$

Equation 45

$$P_{GEN} = I_{ROW} \cdot (n_{ROWs} - 1) \cdot (V_{IFB} + \Delta V_{f,LEDs} \cdot n_{LEDs}) \cdot D_{DIM} = 360mW$$

Equation 46

$$P_{D,tot} \cong P_{D,cond} + P_{D,sw} + P_{GEN,Master} + P_{GEN} = 513mW$$

The junction temperature can be estimated by equation (18) considering $T_A = 25$ °C:

Equation 47

$$T_J = T_{Amb} + R_{th,JA} \cdot P_{D,tot} = 46.5°C$$

In order to estimate also the efficiency, other contributions to the power dissipation must be added to $P_{D, tot}$ (which represents only the power dissipated by the device), that is:

Equation 48

$$P_{DISS,Diode} = V_{F,Diode} \cdot I_{IN} \cdot D_2 = 34.5mW$$

where $V_{F, Diode} = 0.4$ V

Equation 49

$$P_{DISS,Ind} = DCR \cdot I^2_{Ind,RMS} \cong DCR \cdot I^2_{IN} = 11.2mW$$

where DCR = 80 mΩ (typical DCR of the recommended inductors).

Therefore the total dissipated power is:

Equation 50

$$P_{DISS,TOTAL} = P_{D,tot} + P_{DISS,Diode} + P_{DISS,Ind} = 559.1mW$$

Considering the input power as the result of input voltage multiplied by the input current, the estimated efficiency is:

Equation 51

$$\eta = \frac{P_{IN} - P_{DISS,TOT}}{P_{IN}} = 0.845$$

Note: It is important to remind that the previous calculations consider the worst case, especially for the power dissipated on the current generators.
Statistical analysis (confirmed by bench measurements) shows that the series connection of more LEDs on each channel leads to compensation effects.
The hypothesis 3 above mentioned is thus rather unlikely.
Therefore P_{GEN} is significantly lower and the overall efficiency is typically around 90 %.

6.5 Layout consideration

1. A careful PCB layout is important for proper operation. In this section some guidelines are provided in order to achieve a good layout.
2. The device has two different ground pins: signal ground (SGND) and power ground (PGND). The PGND pin handles the switching current related to the boost section; for this reason the PCB traces should be kept as short as possible and with adequate width.
3. The signal ground is the return for the device supply and the current generators and can be connected to the thermal pad.
4. The heat dissipation area (adequate to the application conditions) should be placed backside respect to the device and with the lowest thermal impedance possible (i.e. PCB traces in the backside should be avoided). The dissipation area is thermally and electrically connected to the thermal pad by several vias (nine vias are recommended).
5. The signal and power grounds must be connected together in a single point as close as possible to the PGND pin to reduce ground loops.
6. The R-C components of the compensation network should be placed as close as possible to the COMP pin in order to avoid noise issue and instability of the compensation.
7. Noise sensitive signals (i.e. feedbacks and compensation) should be routed as short as possible to minimize noise collection. The LED7706 pinout makes it easy to separate power components (e.g. inductor, diode) from signal ones.
8. The LX switching node should have and adequate width for high efficiency.
9. The critical power path inductor-LX-PGND must be as short as possible by mounting the inductor, the diode and COUT as close as possible each other.
10. The capacitors of the compensated divider connected to the OVSEL pin should be placed as close as possible to the OVSEL pin.
11. In order to assure good performance in terms of row current accuracy/mismatch, the PCB traces from the rows pins to the LEDs should have similar length and width.
12. The capacitors of the filter connected to LDO5 and VIN pins should be mounted as close as possible to the mentioned pins

Figure 21 and *Figure 22* shows the demonstration board layout (top view and bottom view respectively).

Figure 21. Demonstration board layout (top view)

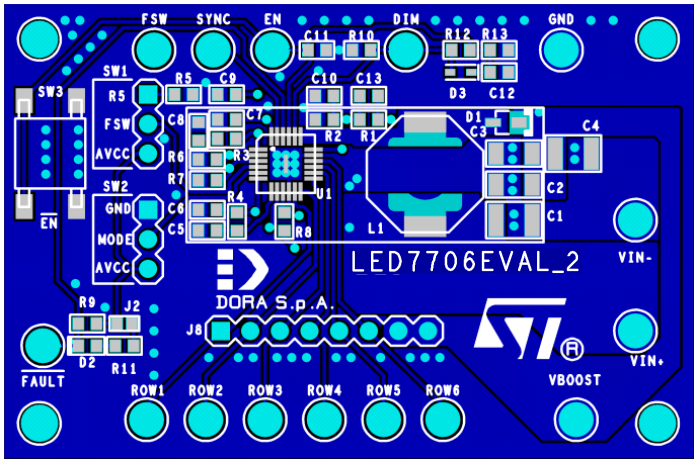


Figure 22. Demonstration board layout (bottom view)

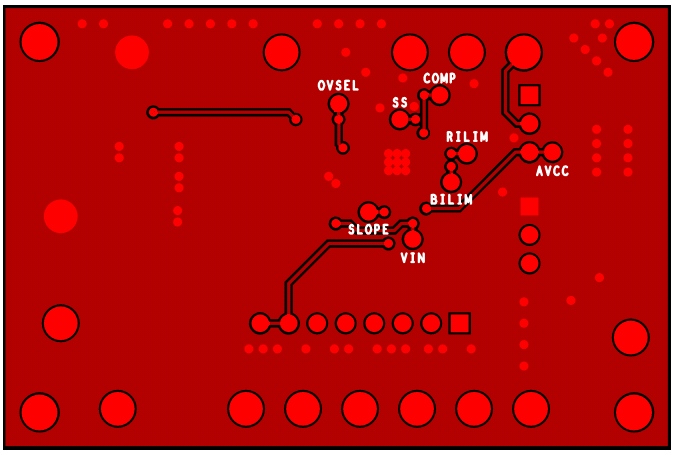


Figure 23 shows the LED7706 demonstration board application circuit, whereas *Table 9* lists the used components and their value.

Figure 23. LED7706 demonstration board schematic

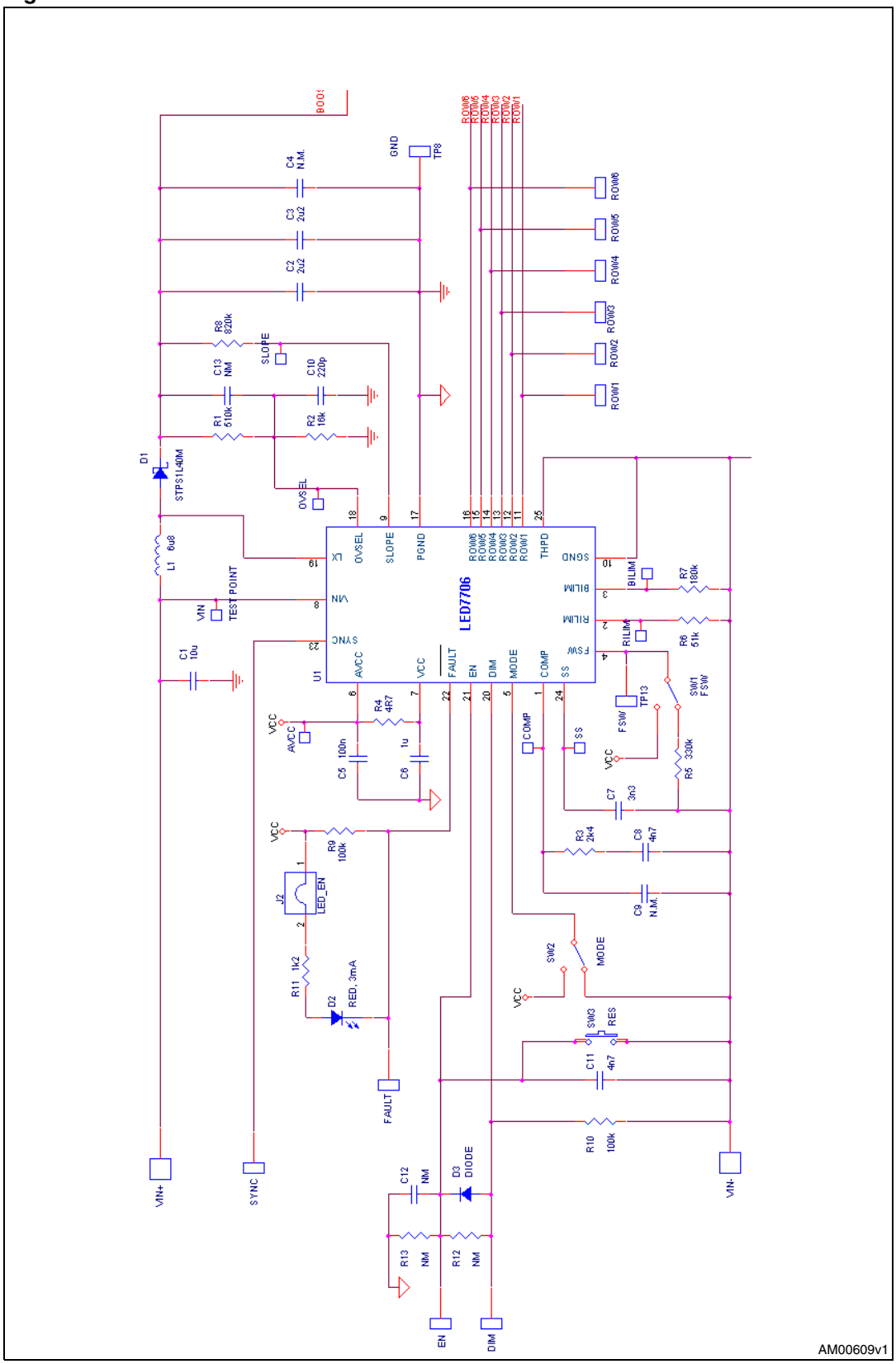


Table 9. LED7706 demonstration board component list

Component	Description	Package	Part number	MFR	Value
C1	Ceramic, 35V X5R, 20%	SMD 1210	UMK325BJ106KM-T	Taiyo Yuden	10 µF
C2,C3	Ceramic, 50V X7R, 20%	SMD 1206	GRM31CR71H225KA88B	Murata	2.2 µF
C4		SMD 1206	GRM31CR71H225KA88B		N.M.
C5	Ceramic, 25V X5R, 20%	SMD 0603		Standard	1 µF
C6					100 nF
C7					3.3 nF
C8					4.7 nF
C9					N.M.
C10					220 pF
C11					4.7 nF
C12					N.M.
C13					15 pF
R1	Chip resistor 0.1 W, 1%	SMD 0603		Standard	510 kΩ
R2					16 kΩ
R3					2.4 kΩ
R4					4.7 Ω
R5					330 kΩ
R6					51 kΩ
R7	Chip resistor 0.1 W, 1%	SMD 0603		Standard	180 kΩ
R8					680 kΩ
R9, R10					100 kΩ
R11					1.2 kΩ
R12					N.M.
R13					N.M.
L1	6u8, 75 mΩ, 2.7 A	6x6 mm	LPS6235-682MLC	Coilcraft	6.8 µF
D1	Schottky, 40 V, 1 A	DO216-AA	STPS1L40M	ST	STPS1L40M
D2	Red LED, 3 mA	SMD 0603		Standard	
D3	Signal Schottky	SOD-523		BAS69	N.M.
U1	Integrated circuit	QFN4x4	LED7706	ST	LED7706
J2	PCB pad jumper				
J8	Header 8	SIL 8		Standard	
SW1, SW2	Jumper 3	SIL 3		Standard	
SW3	Push button	6x6 mm	FSM4JSMAT	TYCO	

7 Electrical characteristics

Figure 24. Efficiency versus DIM duty cycle, V_{IN} = 6 V, 6 rows, 10 white LEDs (20 mA) in series

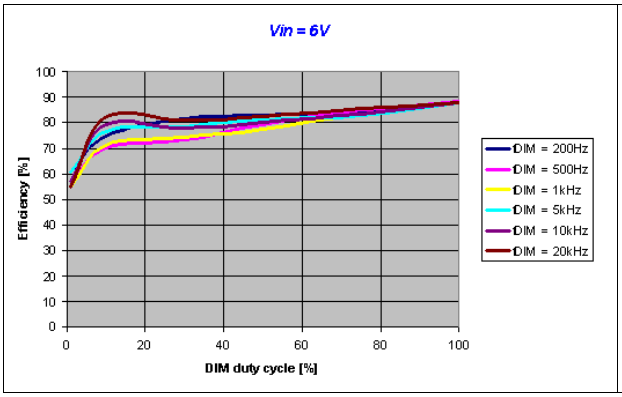


Figure 25. Efficiency versus DIM duty cycle, V_{IN} = 12 V, 6 rows, 10 white LEDs (20 mA) in series

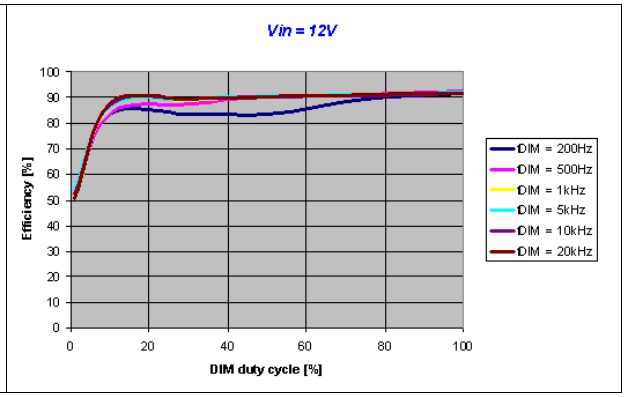


Figure 26. Efficiency versus DIM duty cycle, V_{IN} = 18 V, 6 rows, 10 white LEDs (20 mA) in series

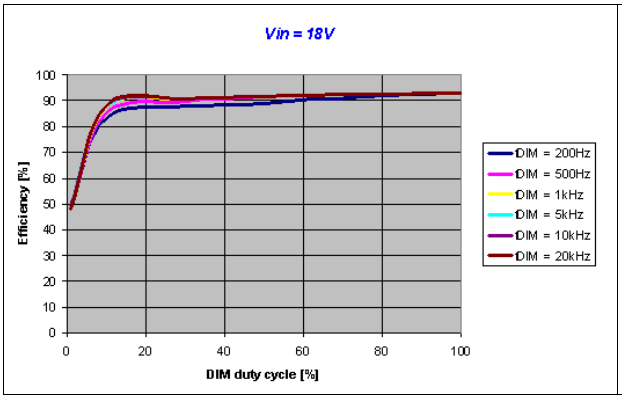


Figure 27. Efficiency versus DIM duty cycle, V_{IN} = 24 V, 6 rows, 10 white LEDs (20 mA) in series

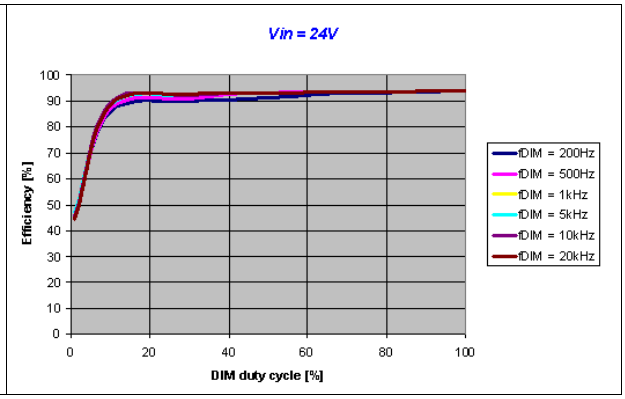


Figure 28. Soft-start waveforms (EN, SS, and V_{OUT} monitored)

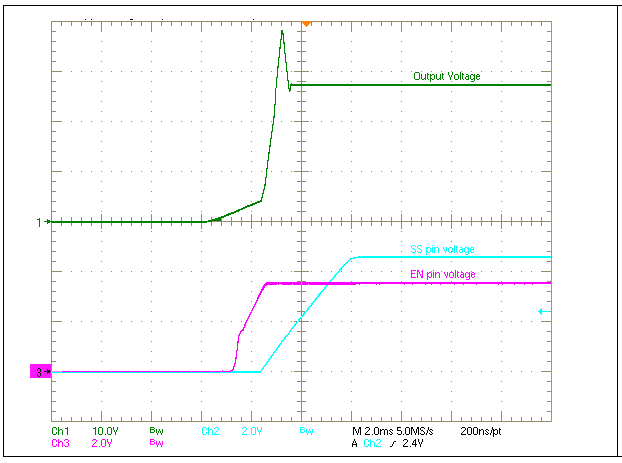


Figure 29. Boost section switching signals (LX, SYNC and inductor current monitored), V_{IN} = 12 V, 10 LEDs

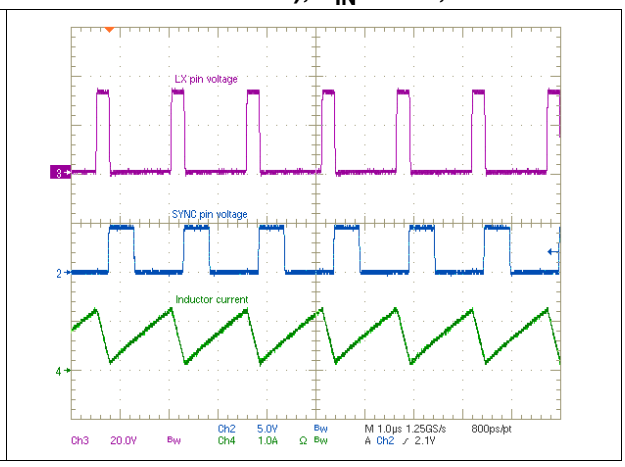


Figure 30. Dimming waveforms (F_{DIM} = 200 Hz)

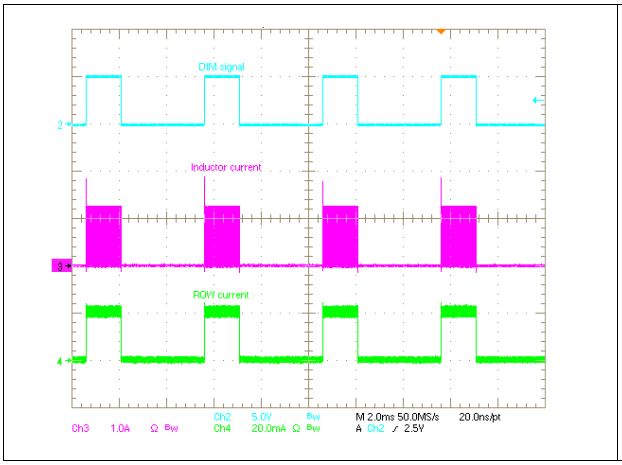


Figure 31. Dimming waveforms (F_{DIM} = 1 kHz)

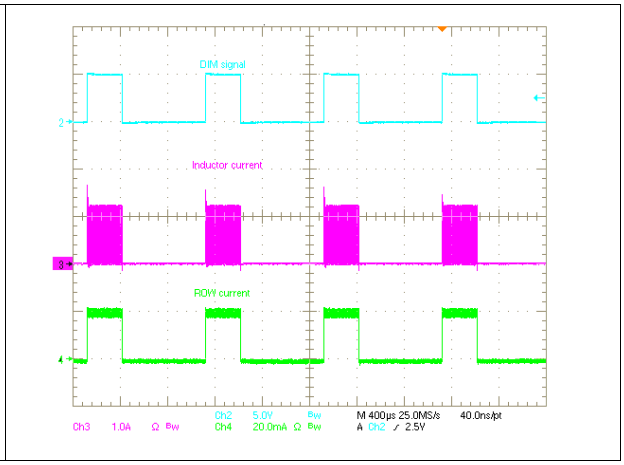


Figure 32. Dimming waveforms (F_{DIM} = 5 kHz)

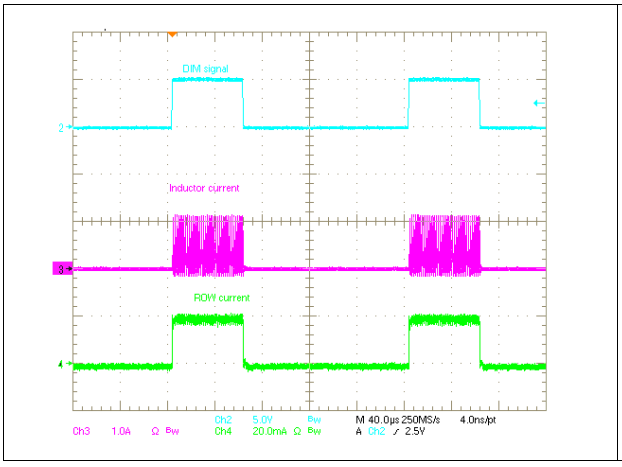


Figure 33. Dimming waveforms (F_{DIM} = 20 kHz)

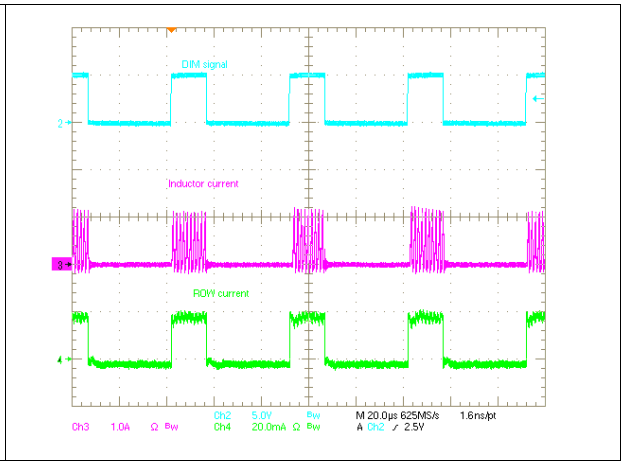


Figure 34. Dimming waveforms ($T_{DIM,ON}$ = 10 µs)

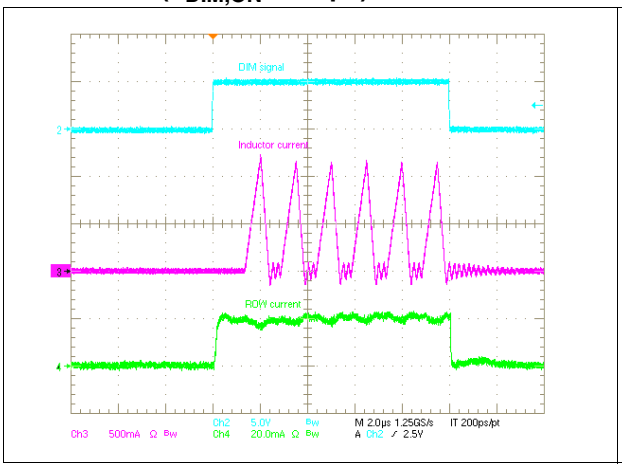
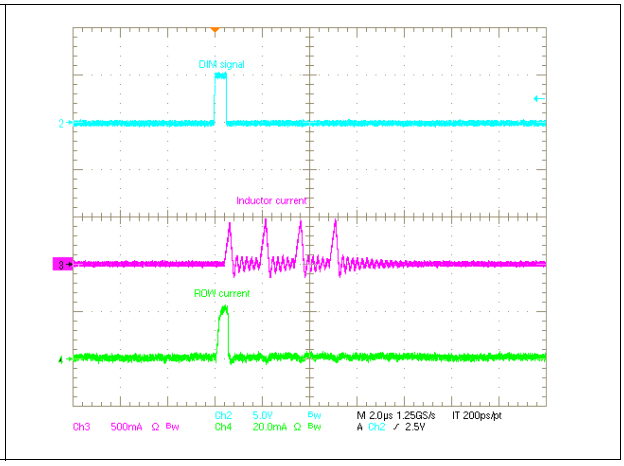


Figure 35. Dimming waveforms with the minimum dimming on time (500 ns)



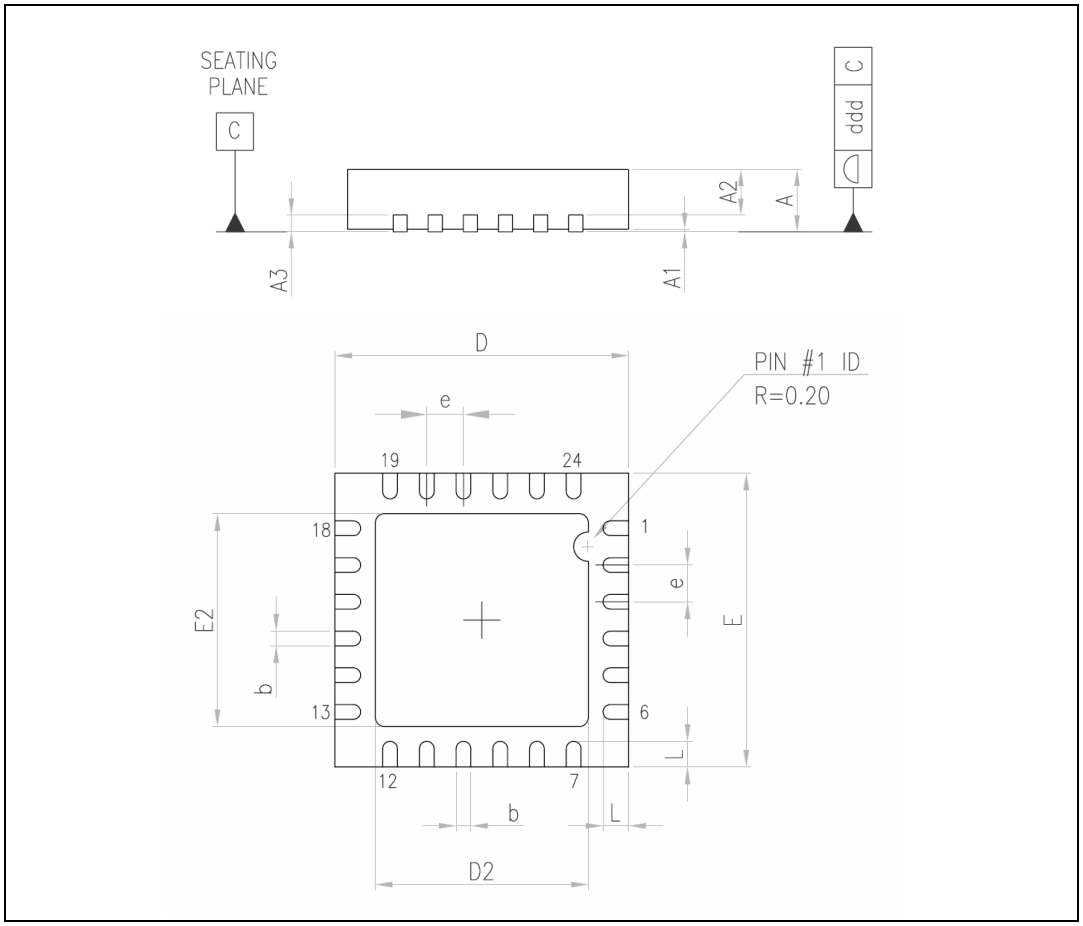
8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 10. VFQFPN-24 4 mm x 4 mm mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20	
b	0.18	0.25	0.30
D	3.85	4.00	4.15
D2	2.40	2.50	2.60
E	3.85	4.00	4.15
E2	2.40	2.50	2.60
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

Figure 36. Package dimensions



9 Revision history

Table 11. Document revision history

Date	Revision	Changes
08-Feb-2008	1	Initial release
09-Apr-2009	2	Added: *Chapter 3 on page 7*, *Chapter 3 on page 7* and *Chapter 3 on page 7* Updated: *Chapter 3 on page 7*, *Chapter 3 on page 7*, *Chapter 3 on page 7*, *Table 4*, *Table 5*, *Figure 3*, *Figure 4*, *Figure 7*, *Figure 23* and *Table 9*

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