



# STH250N55F3-6

N-channel 55 V, 2.2 mΩ, 180 A, H<sup>2</sup>PAK  
STripFET™ III Power MOSFET

## Features

| Order code    | V <sub>DSS</sub> | R <sub>DS(on) max.</sub> | I <sub>D</sub>       | P <sub>w</sub> |
|---------------|------------------|--------------------------|----------------------|----------------|
| STH250N55F3-6 | 55 V             | 2.6 mΩ                   | 180 A <sup>(1)</sup> | 300 W          |

1. Value limited by package

- Ultra low on-resistance
- 100% avalanche tested

## Application

Switching applications

## Description

This N-channel STripFET™ III Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performance.

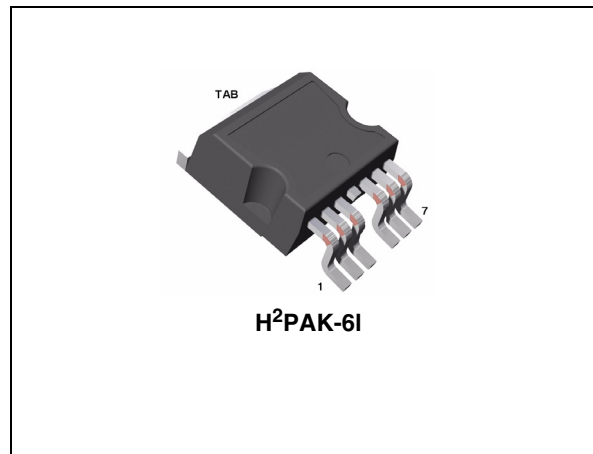


Figure 1. Internal schematic diagram

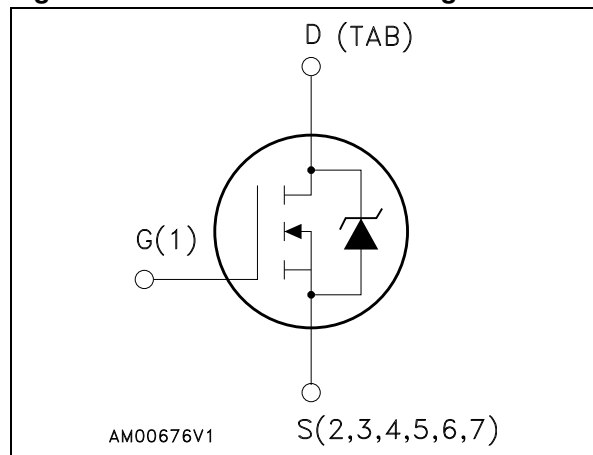


Table 1. Device summary

| Order code    | Marking  | Package            | Packaging     |
|---------------|----------|--------------------|---------------|
| STH250N55F3-6 | 250N55F3 | H <sup>2</sup> PAK | Tape and reel |

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol             | Parameter  | Value       | Unit                |
|--------------------|--|-------------|---------------------|
| $V_{DS}$           | Drain-source voltage ( $V_{GS}=0$ )                            | 55          | V                   |
| $V_{GS}$           | Gate-source voltage  | $\pm 20$    | V                   |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 180         | A                   |
| $I_D^{(1)}$        | Drain current (continuous) at $T_C=100\text{ }^\circ\text{C}$  | 160         | A                   |
| $I_{DM}^{(2)}$     | Drain current (pulsed)   | 720         | A                   |
| $P_{TOT}$          | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$          | 300         | W                   |
|                    | Derating factor  | 2.0         | W/ $^\circ\text{C}$ |
| $dv/dt^{(3)}$      | Peak diode recovery voltage slope                              | 11          | V/ns                |
| $E_{AS}^{(4)}$     | Single pulse avalanche energy                                  | 1000        | mJ                  |
| $T_j$<br>$T_{stg}$ | Operating junction temperature<br>storage temperature          | - 55 to 175 | $^\circ\text{C}$    |

1. Current limited by package.
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 120\text{ A}$ ,  $di/dt \leq 900\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$
4. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 60\text{ A}$ ,  $V_{DD} = 40\text{ V}$  (see Figure 16 and Figure 17)

**Table 3. Thermal data**

| Symbol              | Parameter                               | Value | Unit                      |
|---------------------|---|-------|---------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case        | 0.5   | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-ambient max | 35    | $^\circ\text{C}/\text{W}$ |

1. When mounted on FR-4 board, on 1inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

| Symbol        | Parameter  | Test conditions  | Min. | Typ. | Max.      | Unit                           |
|---------------|--|--|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage                   | $I_D = 1\text{ mA}$ , $V_{GS} = 0$   | 55   |      |           | V                              |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = \text{max rating}$ ,<br>$V_{DS} = \text{max rating}$ , @ $125\text{ °C}$ |      |      | 10<br>100 | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 20\text{ V}$   |      |      | $\pm 200$ | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                 | 2    |      | 4         | V                              |
| $R_{DS(on)}$  | Static drain-source on resistance                | $V_{GS} = 10$ , $I_D = 60\text{ A}$  |      | 2.2  | 2.6       | $\text{m}\Omega$               |

**Table 5. Dynamic**

| Symbol       | Parameter                    | Test conditions   | Min. | Typ. | Max. | Unit          |
|--------------|------------------------------|---|------|------|------|---------------|
| $C_{iss}$    | Input capacitance            | $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$   | -    | 6800 | -    | $\mu\text{F}$ |
| $C_{oss}$    | Output capacitance           |   |      | 1450 |      |               |
| $C_{rss}$    | Reverse transfer capacitance |   |      | 15   |      |               |
| $t_{d(on)}$  | Turn-on delay time           | $V_{DD} = 27.5\text{ V}$ , $I_D = 60\text{ A}$<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 13</a> ,<br><a href="#">Figure 18</a> ) | -    | 25   | -    | ns            |
| $t_r$        | Rise time                    |   |      | 150  |      |               |
| $t_{d(off)}$ | Turn-off delay time          |   |      | 110  |      |               |
| $t_f$        | Fall time                    |   |      | 50   |      |               |
| $Q_g$        | Total gate charge            | $V_{DD} = 44\text{ V}$ , $I_D = 120\text{ A}$ ,<br>$V_{GS} = 10\text{ V}$ ,<br>(see <a href="#">Figure 14</a> )   | -    | 100  | -    | nC            |
| $Q_{gs}$     | Gate-source charge           |   |      | 30   |      |               |
| $Q_{gd}$     | Gate-drain charge            |   |      | 26   |      |               |

**Table 6. Source drain diode**

| Symbol                            | Parameter  | Test conditions   | Min. | Typ.              | Max.       | Unit                     |
|-----------------------------------|--|---|------|-------------------|------------|--------------------------|
| $I_{SD}$<br>$I_{SDM}^{(1)}$       | Source-drain current<br>Source-drain current (pulsed)                        |   | -    |                   | 180<br>720 | A<br>A                   |
| $V_{SD}^{(2)}$                    | Forward on voltage   | $I_{SD}=120\text{ A}$ , $V_{GS}=0$  | -    |                   | 1.5        | V                        |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}=120\text{ A}$ ,<br>$di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 35\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$<br>(see <a href="#">Figure 15</a> ) | -    | 60<br>0.11<br>3.5 |            | ns<br>$\mu\text{C}$<br>A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

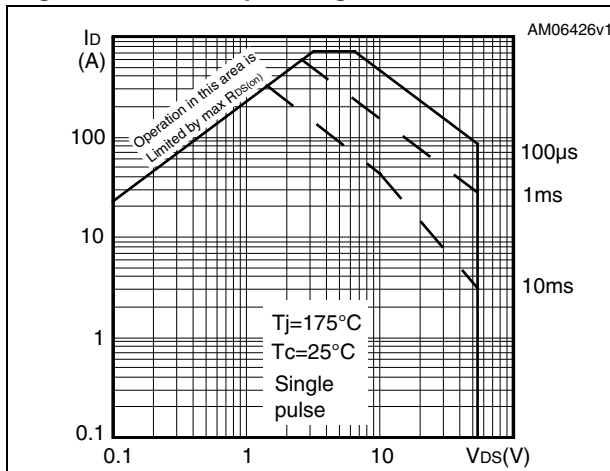


Figure 3. Thermal impedance

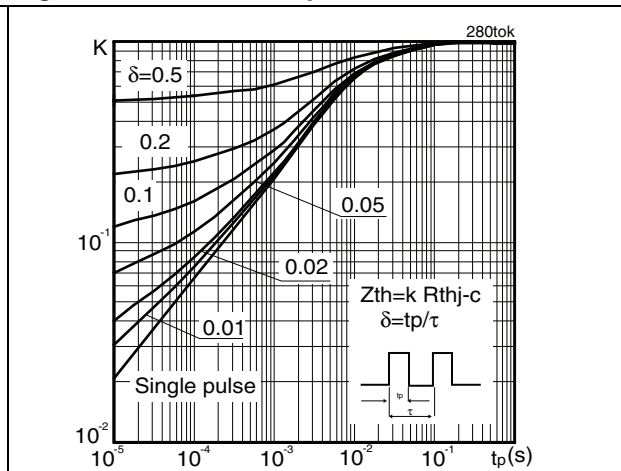


Figure 4. Output characteristics

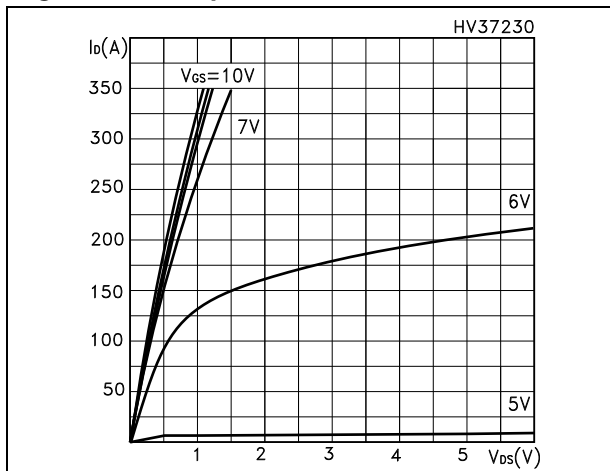


Figure 5. Transfer characteristics

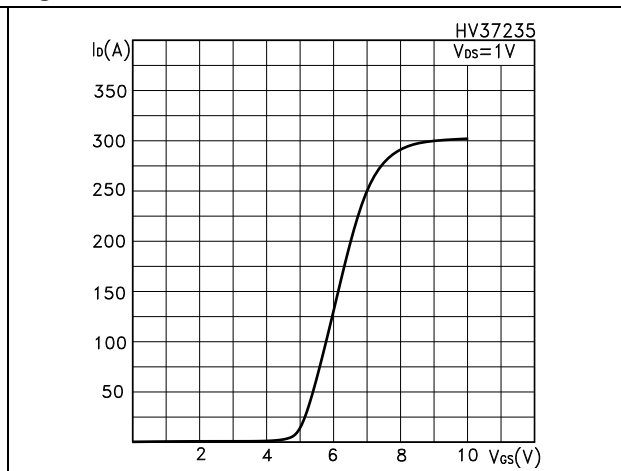


Figure 6. Normalized  $B_{V_{DSS}}$  vs temperature

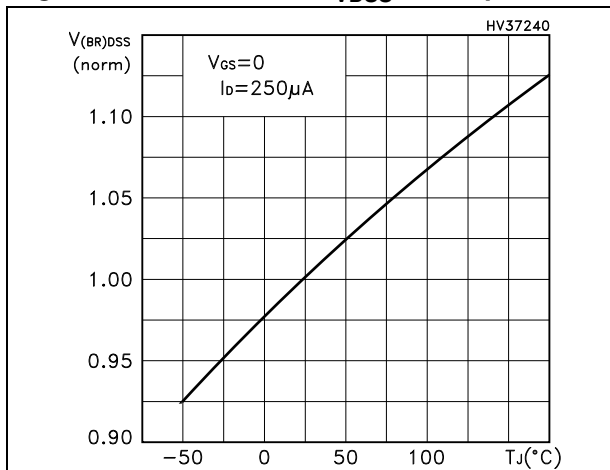


Figure 7. Static drain-source on resistance

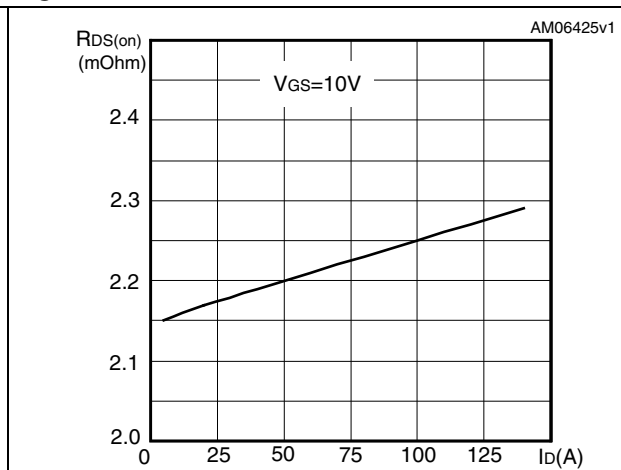


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

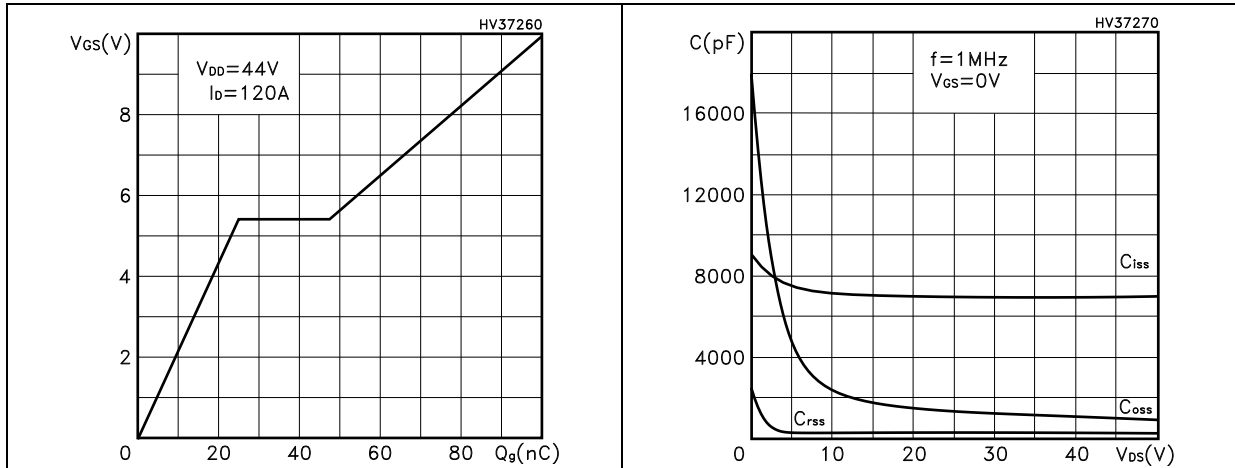


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

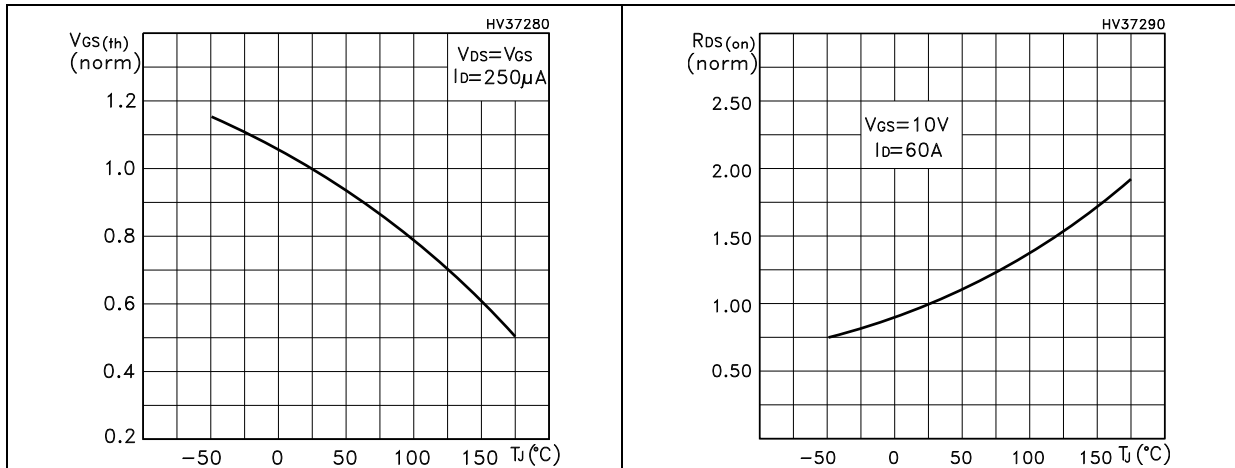
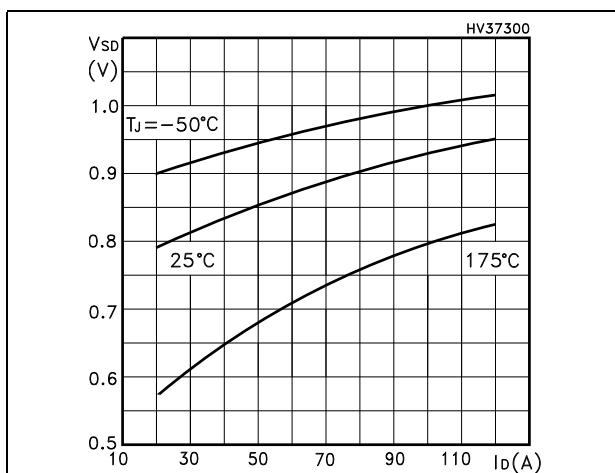
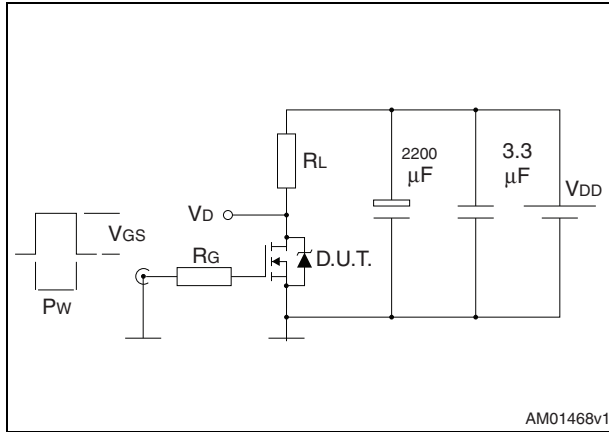


Figure 12. Source-drain diode forward characteristics

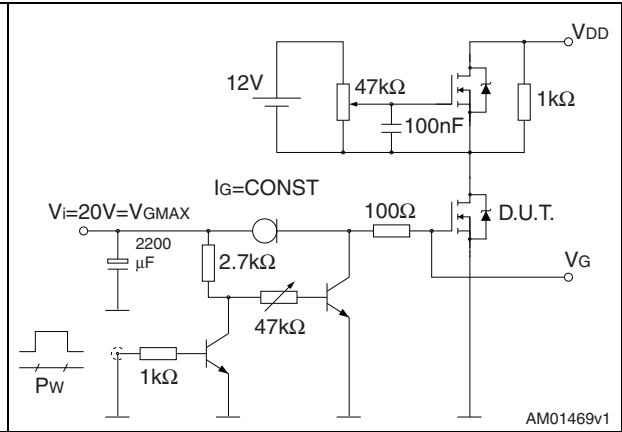


### 3 Test circuits

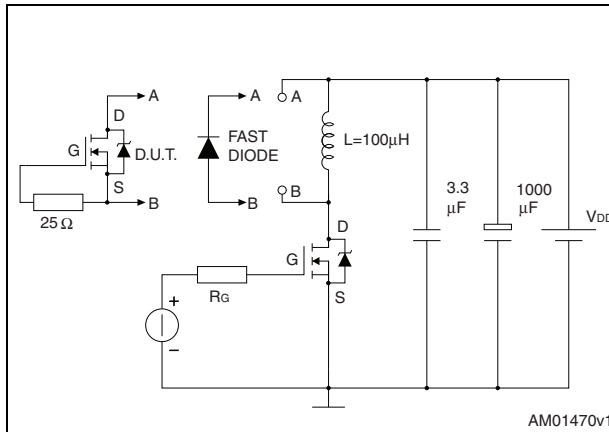
**Figure 13. Switching times test circuit for resistive load**



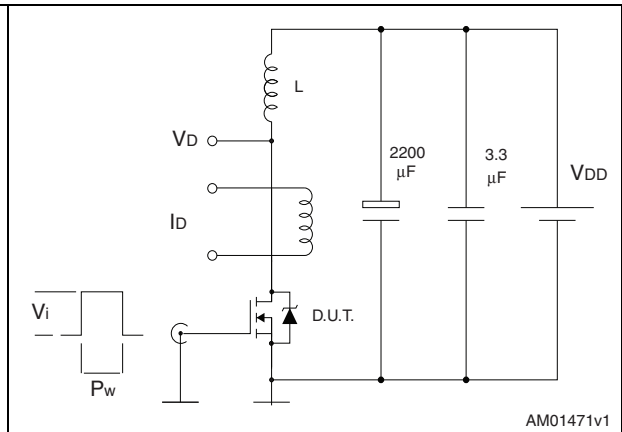
**Figure 14. Gate charge test circuit**



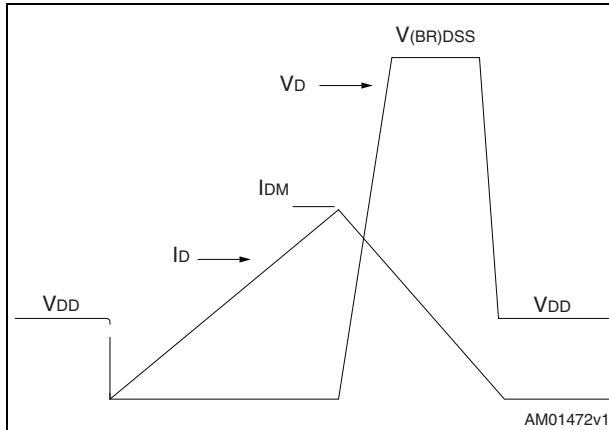
**Figure 15. Test circuit for inductive load switching and diode recovery times**



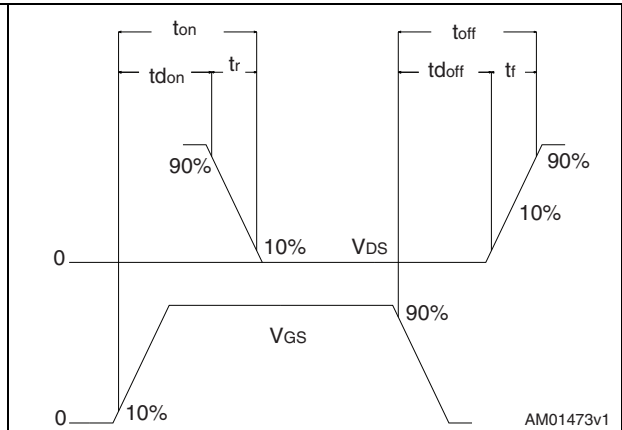
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 7. H<sup>2</sup>PAK-6 mechanical data**

| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 4.30  |      | 4.80  |
| A1   | 0.03  |      | 0.20  |
| C    | 1.17  |      | 1.37  |
| e    | 2.34  |      | 2.74  |
| e1   | 4.88  |      | 5.28  |
| e2   | 7.42  |      | 7.82  |
| E    | 0.45  |      | 0.60  |
| F    | 0.50  |      | 0.70  |
| H    | 10.00 |      | 10.40 |
| H1   | 7.80  |      | 8.20  |
| L    | 14.75 |      | 15.25 |
| L1   | 1.27  |      | 1.40  |
| L2   | 4.35  |      | 4.95  |
| L3   | 7.45  |      | 7.85  |
| L4   | 1.5   |      | 1.75  |
| M    | 1.90  |      | 2.50  |
| R    | 0.20  |      | 0.60  |
| V    | 0°    |      | 8°    |

Figure 19. H<sup>2</sup>PAK-6 drawing

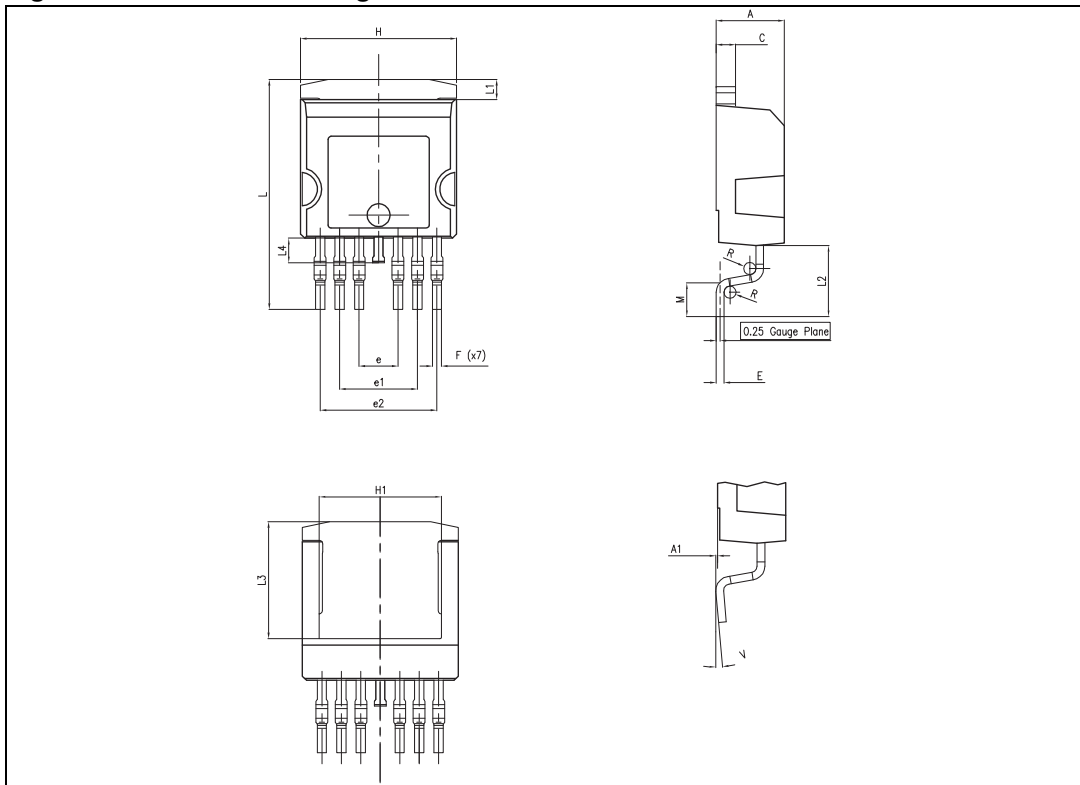
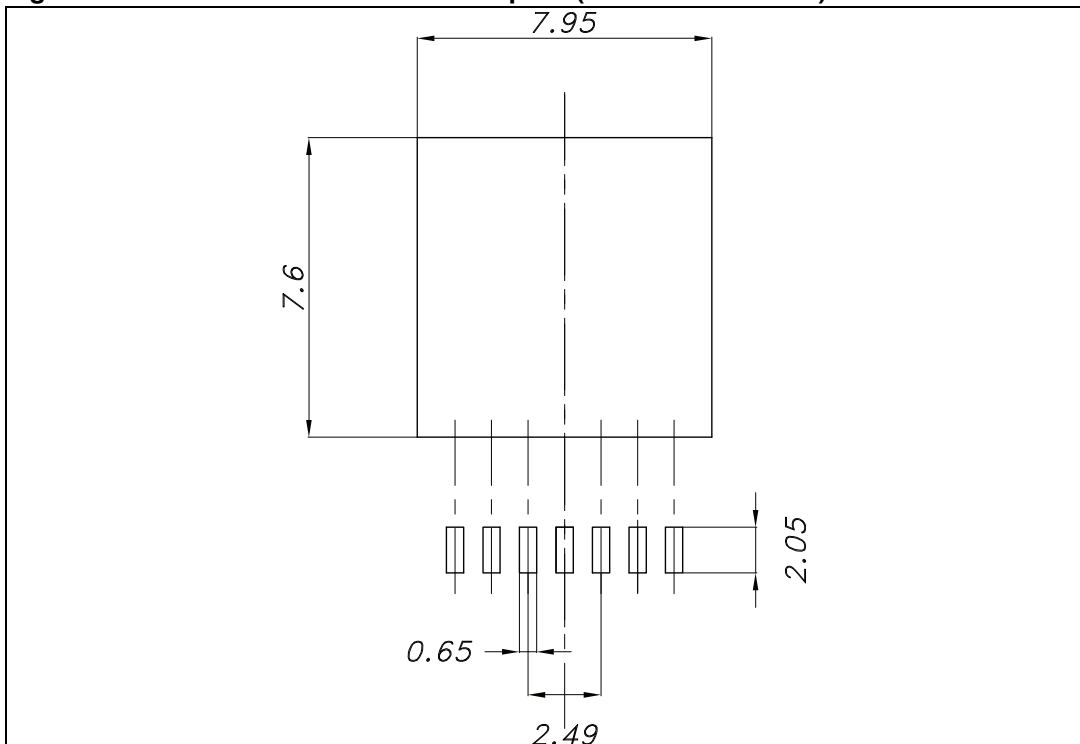
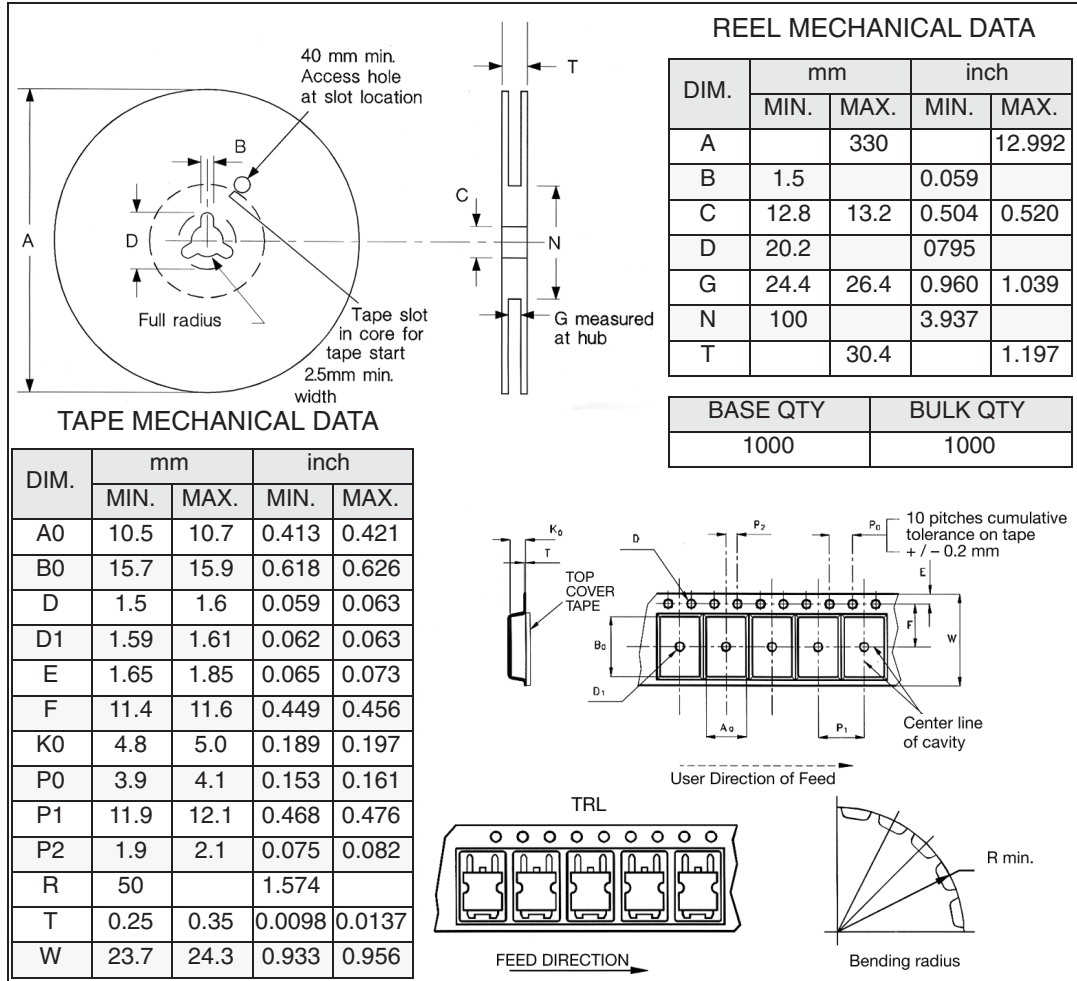


Figure 20. H<sup>2</sup>PAK-6 recommended footprint (dimensions in mm)



# 5 Packaging mechanical data

Figure 21. H<sup>2</sup>PAK-6 tape and reel



## 6 Revision history

**Table 8. Revision history**

| Date        | Revision | Changes       |
|-------------|----------|---------------|
| 01-Oct-2010 | 1        | First release |

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