

#### **STL120N2VH5**

N-channel 20 V, 0.002 Ω, 28 A STripFET™ V Power MOSFET in PowerFLAT™ 5x6 package

#### **Features**

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL120N2VH5	20 V	< 0.003 Ω	28 A

- Improved die-to-footprint ratio
- Very low profile package
- Very low thermal resistance
- Conduction losses reduced
- Switching losses reduced
- 2.5 V gate drive
- Very low threshold device

#### **Applications**

Switching applications

#### **Description**

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™V technology. The device has been optimized to achieve very low on-state resistance, contributing to an FOM that is among the best in its class.

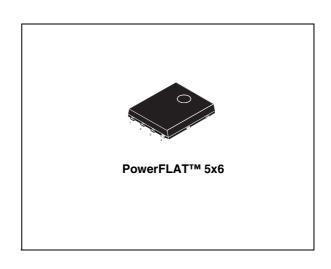


Figure 1. Internal schematic diagram

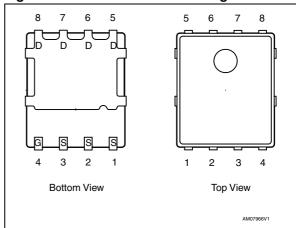


Table 1. Device summary

Order code	Marking	Package	Packaging	
STL120N2VH5	STL120N2VH5 120N2VH5		Tape and reel	

Contents STL120N2VH5

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STL120N2VH5 Electrical ratings

## 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage	20	V
V <sub>GS</sub>	Gate-source voltage	± 8	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	120	Α
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 100 °C	75	Α
I <sub>D</sub> <sup>(2)</sup>	Drain current (continuous) at T <sub>pcb</sub> = 25 °C	28	Α
I <sub>DM</sub> (2),(3)	Drain current (pulsed)	112	Α
P <sub>TOT</sub> (1)	Total dissipation at T <sub>C</sub> = 25 °C	80	W
P <sub>TOT</sub> <sup>(2)</sup>	Total dissipation at T <sub>pcb</sub> = 25 °C	4	W
	Derating factor <sup>(2)</sup>	0.03	W/°C
T <sub>j</sub> T <sub>stg</sub>	Operating junction temperature storage temperature	- 55 to 150	°C

- 1. The value is rated according to Rthj-case
- 2. When mounted on FR-4 board of 1in², 2oz Cu. t < 10 sec
- 3. Pulse width limited by safe operating area

Table 3. Thermal data

	Symbol	Parameter	Value	Unit
Ī	R <sub>thj-case</sub>	Thermal resistance junction-case max.	1.56	°C/W
	R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max.	31.25	°C/W

<sup>1.</sup> When mounted on FR-4 board of 1in², 2oz Cu. t < 10 sec

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	20	А
E <sub>AS</sub>	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$ , $V_{DD} = 14$ V)	300	mJ

Electrical characteristics STL120N2VH5

## 2 Electrical characteristics

 $(T_{CASE} = 25 \, ^{\circ}C \text{ unless otherwise specified})$ 

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	20			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 20 V V <sub>DS</sub> =20 V, T <sub>C</sub> = 125 °C			1 10	μ <b>Α</b> μ <b>Α</b>
I <sub>GSS</sub>	Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 8 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	0.70			V
R <sub>DS(on)</sub>	Static drain-source on resistance	$V_{GS} = 4.5 \text{ V}, I_D = 14 \text{ A}$ $V_{GS} = 2.5 \text{ V}, I_D = 14 \text{ A}$		0.002 0.0028	0.003 0.004	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 15 V, f = 1 MHz, V <sub>GS</sub> = 0	-	4660 870 130		pF pF pF
$\begin{array}{c} t_{\text{d(on)}} \\ t_{\text{r}} \\ t_{\text{d(off)}} \\ t_{\text{f}} \end{array}$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 10 \text{ V}, I_{D} = 14 \text{ A}$ $R_{G} = 4.7 \Omega V_{GS} = 4.5 \text{ V}$ (see <i>Figure 13</i> )	-	21 60 76 55	-	ns ns ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 10 \text{ V}, I_{D} = 28 \text{ A},$ $V_{GS} = 2.5 \text{ V}$ (see <i>Figure 14</i> )	-	29 9.8 13	-	nC nC nC

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current Source-drain current (pulsed)		-		28 112	A A
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 28 A, V <sub>GS</sub> = 0	-		1.1	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}$ = 28 A, di/dt = 100 A/ $\mu$ s, $V_{DD}$ = 16 V (see <i>Figure 15</i> )	-	34 30 1.4		ns nC A
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 28 \text{ A},$ $di/dt = 100 \text{ A/}\mu\text{s},$ $V_{DD} = 16 \text{ V}, T_j = 150 ^{\circ}\text{C}$ (see <i>Figure 15</i> )	-	35 31 1.8		ns nC A

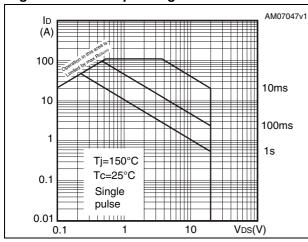
<sup>1.</sup> Pulse width limited by safe operating area.

<sup>2.</sup> Pulsed: Pulse duration =  $300 \mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

Figure 3. Thermal impedance



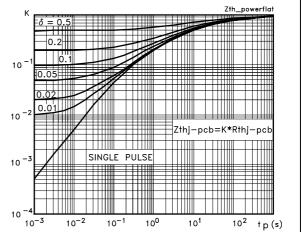
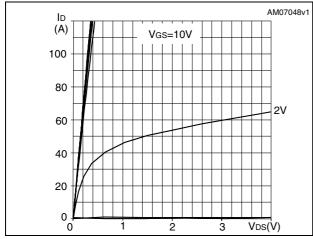


Figure 4. Output characteristics

Figure 5. Transfer characteristics



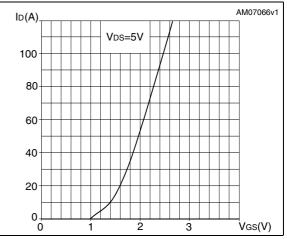
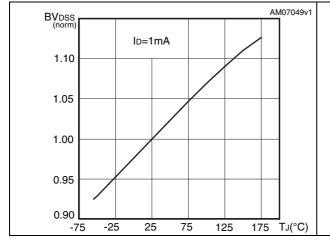
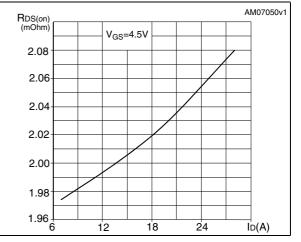


Figure 6. Normalized B<sub>VDSS</sub> vs temperature

Figure 7. Static drain-source on resistance





AM07051v1 AM07052v1 Vgs C (pF) (V) 7100 VDD=10V 10 ID=28A 6100 Ciss 8 5100 4100 6 3100 4 2100 Coss 2 1100 Crss 100 5 15 20 40 60 80 100 120 Qg(nC) 10 VDS(V)

Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

Figure 10. Normalized gate threshold voltage Figure 11. Normalized on resistance vs vs temperature temperature

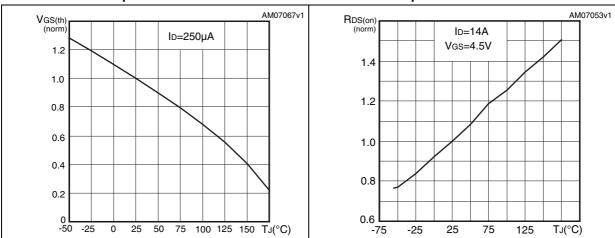
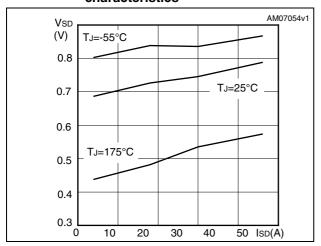


Figure 12. Source-drain diode forward characteristics



Test circuits STL120N2VH5

#### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

Figure 14. Gate charge test circuit

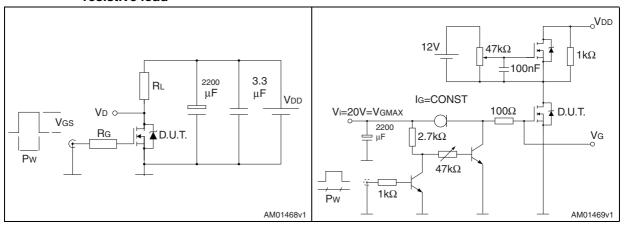


Figure 15. Test circuit for inductive load switching and diode recovery times

Figure 16. Unclamped inductive load test circuit

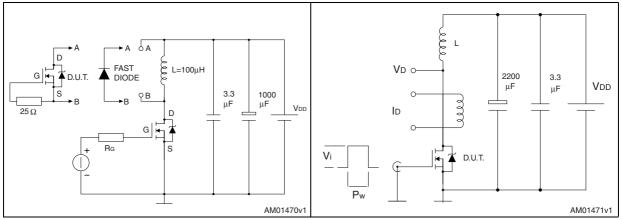
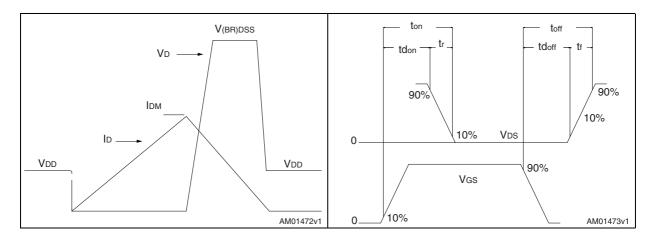


Figure 17. Unclamped inductive waveform

Figure 18. Switching time waveform



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## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 5x6 type C-B mechanical data

Dim.		mm	
Dilli.	Min.	Тур.	Max.
Α	0.80	0.83	0.93
A1	0	0.02	0.05
A3		0.20	
b	0.35	0.40	0.47
D		5.00	
D1		4.75	
D2	4.15	4.20	4.25
Е		6.00	
E1		5.75	
E2	3.43	3.48	3.53
E4	2.58	2.63	2.68
е		1.27	
L	0.70	0.80	0.90

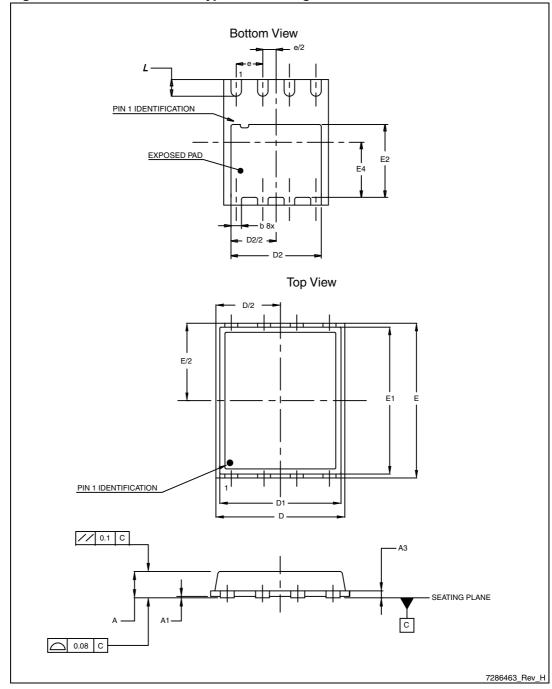


Figure 19. PowerFLAT™ 5x6 type C-B drawing

Table 9. PowerFLAT™ 5x6 type S-C mechanical data

Dim		mm	
Dim.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
е		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

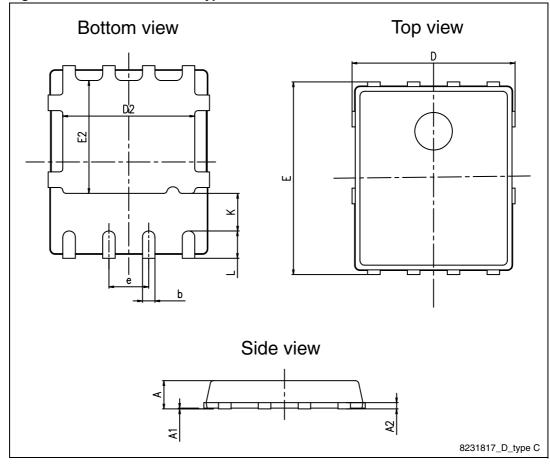


Figure 20. PowerFLAT™ 5x6 type S-C mechanical data

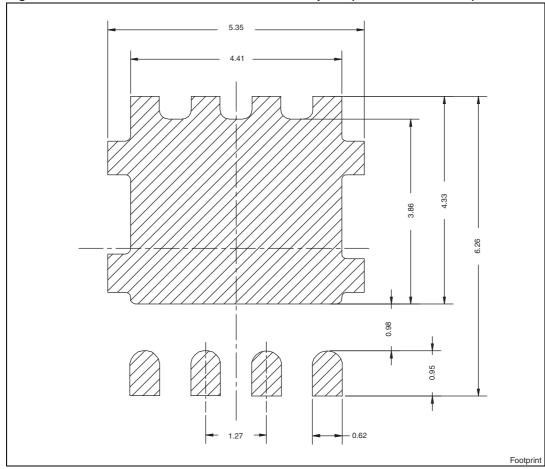


Figure 21. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)

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## 5 Packaging mechanical data

Figure 22. PowerFLAT™ 5x6 tape

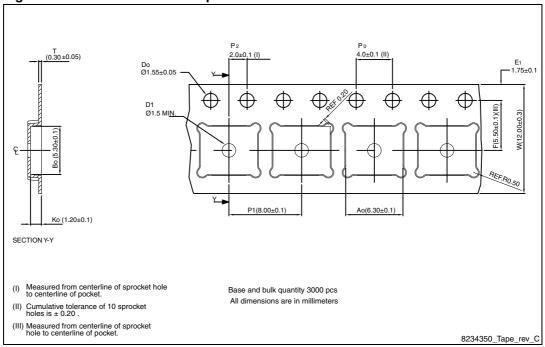
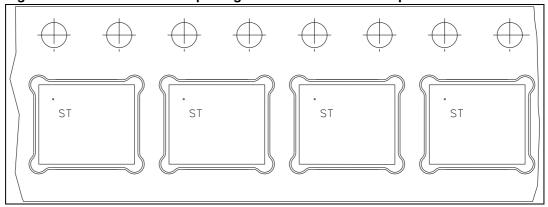


Figure 23. PowerFLAT™ 5x6 package orientation in carrier tape.



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A 330 (+0/-4.0) All dimensions are in millimeters 8234350\_Reel\_rev\_C

Figure 24. PowerFLAT™ 5x6 reel

Doc ID 15603 Rev 2

STL120N2VH5 Revision history

# 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Apr-2009	1	First issue.
01-Mar-2012	2	Document status promoted from preliminary data to datasheet  Section 4: Package mechanical data has been modified:  - Table 8: PowerFLAT™ 5x6 type C-B mechanical data,  Table 9: PowerFLAT™ 5x6 type S-C mechanical data,  Figure 19: PowerFLAT™ 5x6 type C-B drawing, Figure 20:  PowerFLAT™ 5x6 type S-C mechanical data and Figure 21:  PowerFLAT™ 5x6 recommended footprint (dimensions in mm) have been added.

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