

1.2V Drive Pch MOSFET

EM6J1

●Structure

Silicon P-channel MOSFET

●Features

- 1) Two Pch MOSFET are put in EMT6 package.
- 2) High-speed switching.
- 3) Ultra low voltage drive (1.2V drive).
- 4) Built-in G-S Protection Diode.

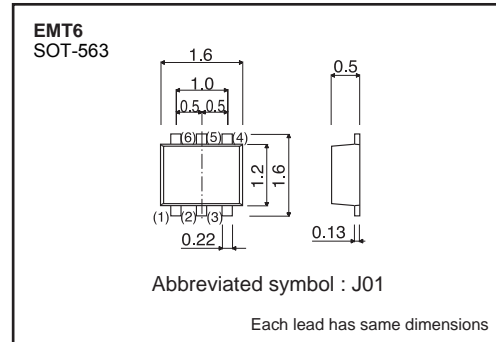
●Applications

Switching

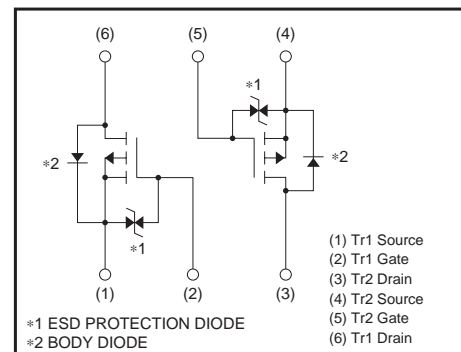
●Packaging specifications

Type	Package	Taping
	Code	T2R
	Basic ordering unit (pieces)	8000
EM6J1		○

●Dimensions (Unit : mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter	Symbol	Limits	Unit
Drain-source voltage	V_{DSS}	-20	V
Gate-source voltage	V_{GSS}	±10	V
Drain current	Continuous	±200	mA
	Pulsed	I_{DP}^{*1}	±800
Source current (Body Diode)	Continuous	-100	mA
	Pulsed	I_{SP}^{*1}	-800
Total power dissipation	P_D^{*2}	150	mW / TOTAL
		120	mW / ELEMENT
Channel temperature	T_{ch}	150	°C
Range of storage temperature	T_{stg}	-55 to +150	°C

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

*2 Each terminal mounted on a recommended land

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th}(ch-a)^*$	833	°C / W / TOTAL
		1042	°C / W / ELEMENT

* Each thermal mounted on a recommended land

●Electrical characteristics (Ta=25°C)

<It is the same ratings for the Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	± 10	μA	$V_{GS} = \pm 10V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	–20	–	–	V	$I_D = -1mA, V_{GS} = 0V$
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	$V_{DS} = -20V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	–0.3	–	–1.0	V	$V_{DS} = -10V, I_D = -100\mu A$
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	0.8	1.2	Ω	$I_D = -200mA, V_{GS} = -4.5V$
		–	1.0	1.5	Ω	$I_D = -100mA, V_{GS} = -2.5V$
		–	1.3	2.2	Ω	$I_D = -100mA, V_{GS} = -1.8V$
		–	1.6	3.5	Ω	$I_D = -40mA, V_{GS} = -1.5V$
		–	2.4	9.6	Ω	$I_D = -10mA, V_{GS} = -1.2V$
Forward transfer admittance	$ Y_{fs} $ *	0.2	–	–	S	$V_{DS} = -10V, I_D = -200mA$
Input capacitance	C_{iss}	–	115	–	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	–	10	–	pF	$V_{GS} = 0V$
Reverse transfer capacitance	C_{rss}	–	6	–	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$ *	–	6	–	ns	$V_{DD} = -10V$
Rise time	t_r *	–	4	–	ns	$I_D = -100mA$ $V_{GS} = -4.5V$
Turn-off delay time	$t_{d(off)}$ *	–	17	–	ns	$R_L = 100\Omega$
Fall time	t_f *	–	17	–	ns	$R_G = 10\Omega$
Total gate charge	Q_g *	–	1.4	–	nC	$V_{DD} = -10V, I_D = -200mA$
Gate-source charge	Q_{gs} *	–	0.3	–	nC	$V_{GS} = -4.5V$
Gate-drain charge	Q_{gd} *	–	0.3	–	nC	$R_L = 50\Omega, R_G = 10\Omega$

*Pulsed

●Body diode characteristics (Source-drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	$I_S = -200mA, V_{GS} = 0V$

*Pulsed

●Electrical characteristics curves

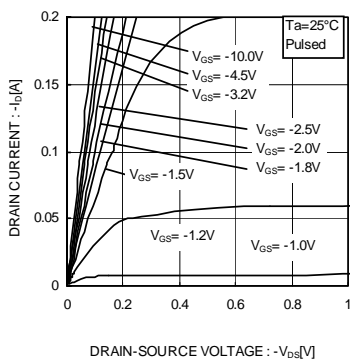


Fig.1 Typical output characteristics (I)

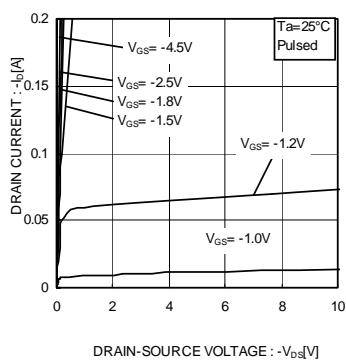


Fig.2 Typical output characteristics (II)

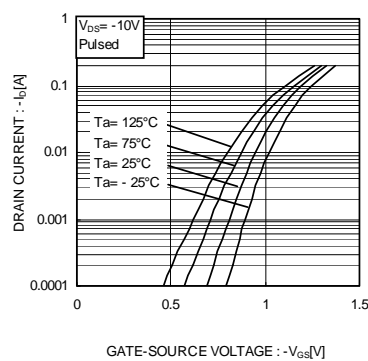


Fig.3 Typical Transfer Characteristics

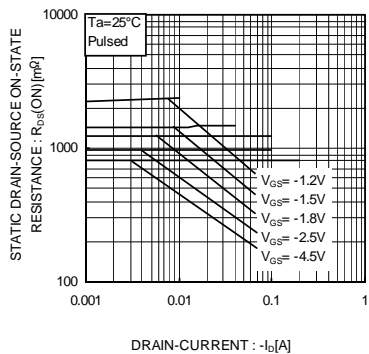


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (I)

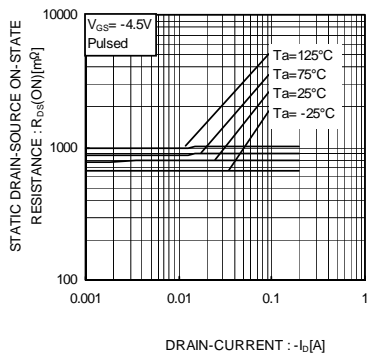


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current (II)

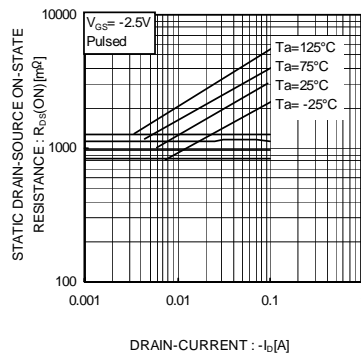


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current (III)

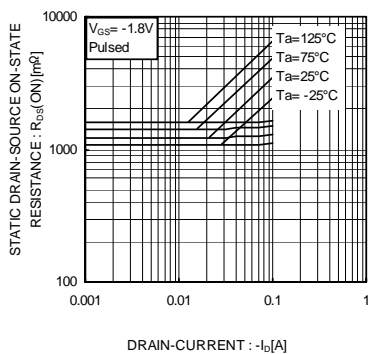


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current (IV)

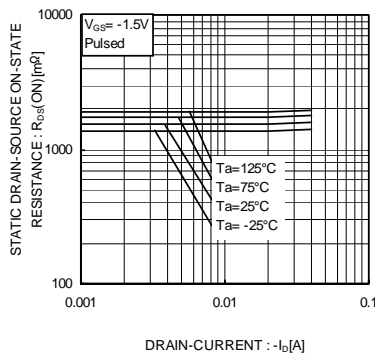


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current (V)

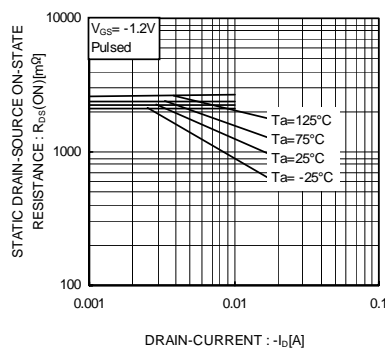


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current (VI)

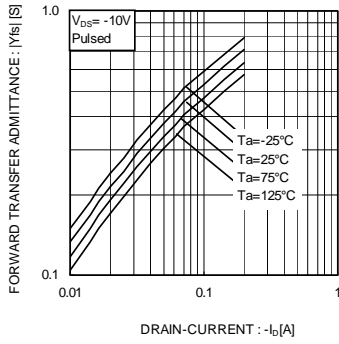


Fig.10 Forward Transfer Admittance vs. Drain Current

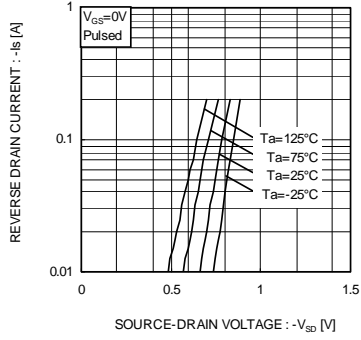


Fig.11 Reverse Drain Current vs. Source-Drain Voltage

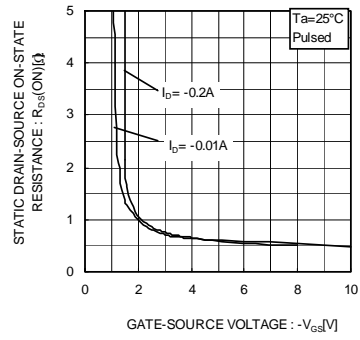


Fig.12 Static Drain-Source On-State Resistance vs. Gate Source Voltage

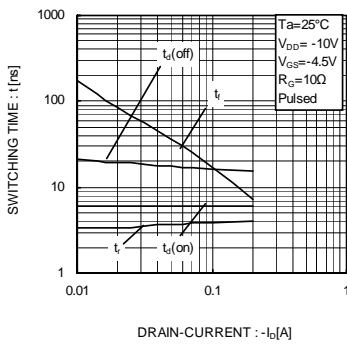


Fig.13 Switching Characteristics

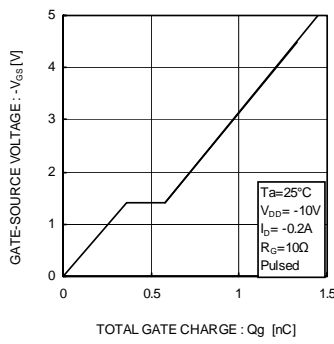


Fig.14 Dynamic Input Characteristics

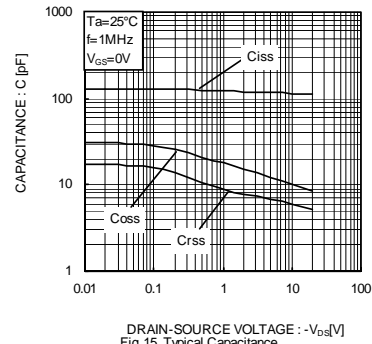


Fig.15 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuit

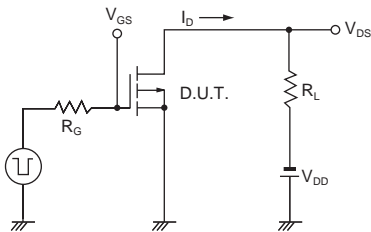


Fig.1-1 Switching Time Measurement Circuit

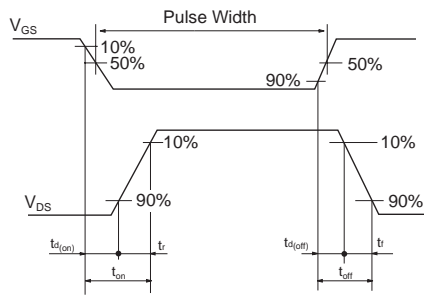


Fig.1-2 Switching Waveforms

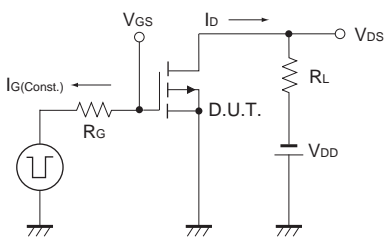


Fig.2-1 Gate Charge Measurement Circuit

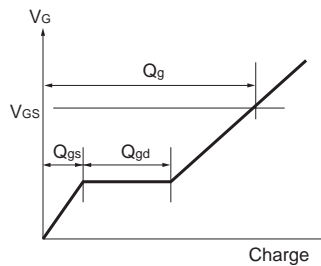


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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