MOS FET

Panasonic

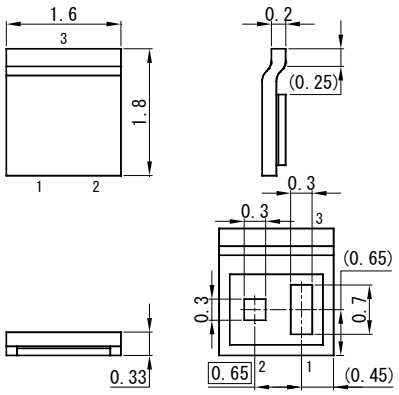
FK3P02110L

FK3P02110L

Silicon N-channel MOSFET

For Load-switching

■ Package dimension Unit: mm



1. Source
2. Gate
3. Drain

Panasonic	PMCP-1816-Z1
JEITA	—
Code	—

■ Features

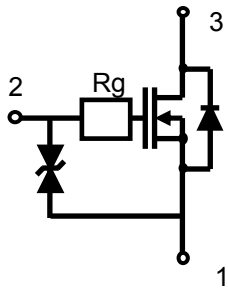
- Low drain-source ON resistance:RDS(on)typ. = 12.5mΩ（VGS = 2.5 V)
- High heat dissipated and ultra-compact package PMCP
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

■ Marking Symbol: A1

■ Packaging

Embossed type (Thermo-compression sealing) : 7 000 pcs / reel (standard)

■ Equivalent circuit, Pin name



1. Source
2. Gate
3. Drain

■ Absolute Maximum Ratings Ta = 25 °C

Parameter		Symbol	Rating	Unit
Drain-source voltage		VDS	24	V
Gate-source voltage		VGS	±12	V
Drain current	Ta = 25 °C, DC *2	ID1	3.0	A
	Ta = 25 °C, DC *3	ID2	6.0	
Drain current (Pulsed)	Ta = 25 °C *1 *2	IDp1	9.0	A
	Ta = 25 °C *1 *3	IDp2	18.0	
Total power dissipation	Ta = 25 °C, DC *2	PD1	200	mW
	Ta = 25 °C, DC *3	PD2	750	
Channel temperature		Tch	150	°C
Operating ambient temperature		Topr	-40 to +85	
Storage temperature range		Tstg	-55 to +150	

Note : *1 t = 10 μs, Duty Cycle < 1%
*2 When mounted on glass epoxy board typeA (Refer to Figure1)
*3 When mounted on glass epoxy board typeB (Refer to Figure2)

■ Electrical Characteristics Ta = 25 °C ±3 °C

Static Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	VDSS	ID = 1.0 mA, VGS = 0 V	24			V
Zero gate voltage drain current	IDSS	VDS = 24 V, VGS = 0 V			1.0	μA
Gate-source leakage current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate-source threshold voltage	Vth	ID = 1.0 mA, VDS = 10 V	0.4	0.85	1.4	V
Drain-source on-state resistance	RDS(on)	ID = 3.0 A, VGS = 2.5 V		12.5	20.0	mΩ

Dynamicic Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance *1	Ciss	VDS = 10 V, VGS = 0 V, f = 1 MHz		1500		pF
Output capacitance *1	Coss			140		
Reverse transfer capacitance *1	Crss			140		

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on delay time *1 *2	td(on)	VDD = 10 V, VGS = 0 to 4 V,ID = 3.0 A		0.6		µs
Rise time *1 *2	tr			0.9		
Turn-off delay time *1 *2	td(off)	VDD = 10 V, VGS = 4 to 0 V,ID = 3.0 A		5.0		µs
Fall time *1 *2	tf			2.3		

Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuringmethods for transistors.
2. *1 Assured by design
*2 Refer to figure3, measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time

Figure1: Glass epoxy board typeA
Material:FR4, Size:25.4mm x 25.4mm x t 1.0mm, Cu pad:tickness 36µm, 25.3mm^2

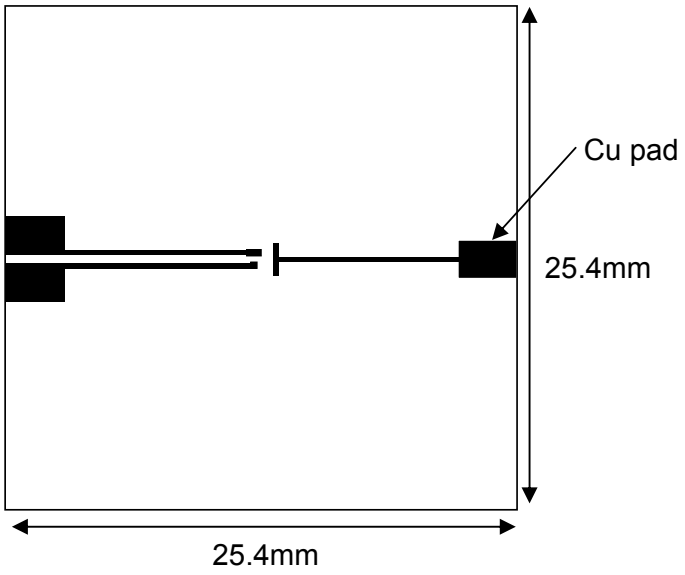

Figure2: Glass epoxy board typeB
Material:FR4, Size:25.4mm x 25.4mm x t 1.0mm, Cu pad:tickness 36µm, 82.0mm^2

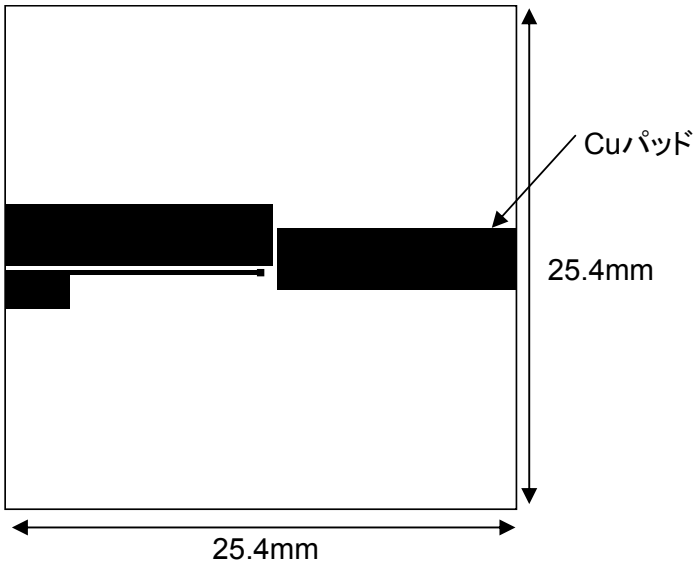

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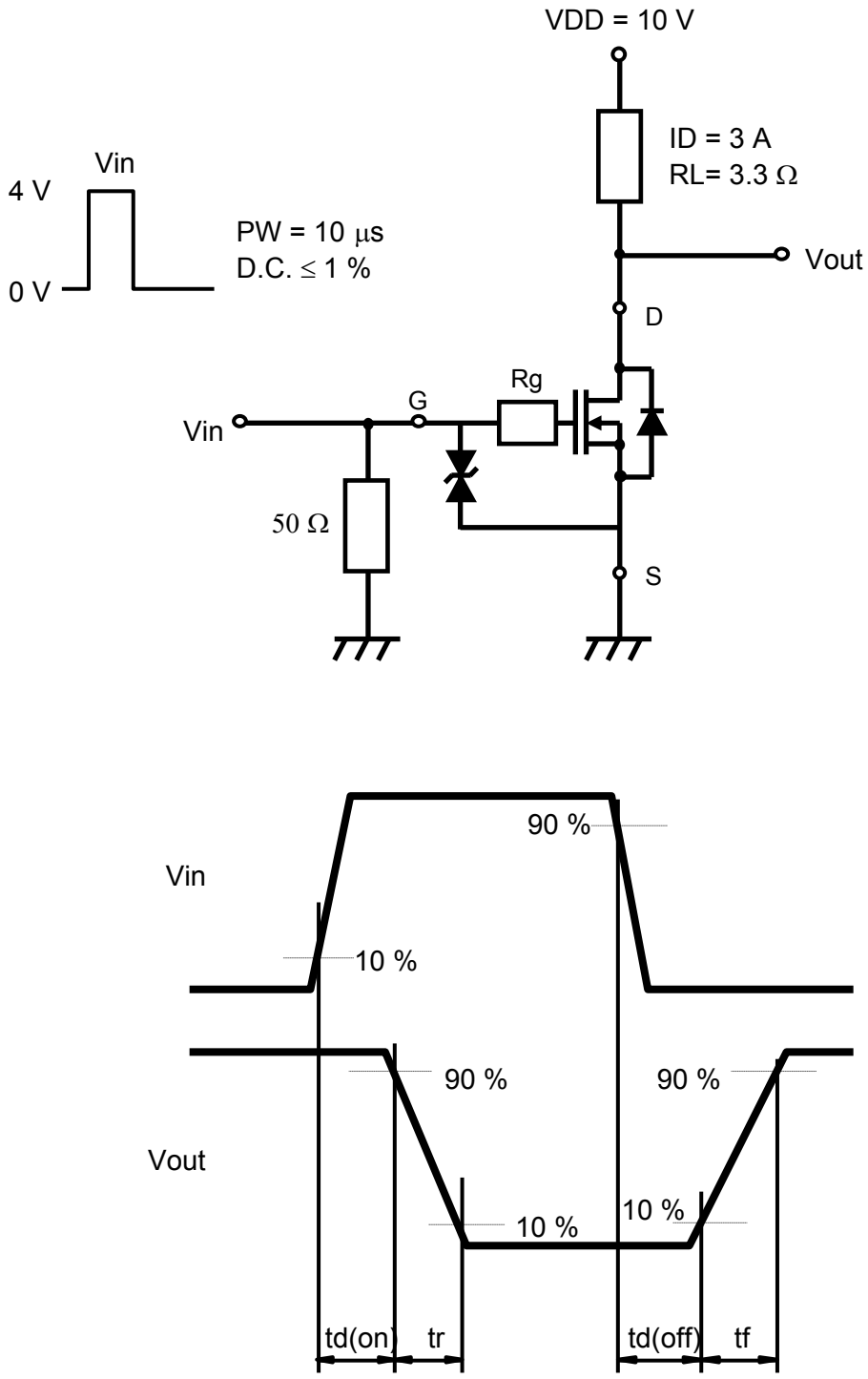
Figure3: Measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time



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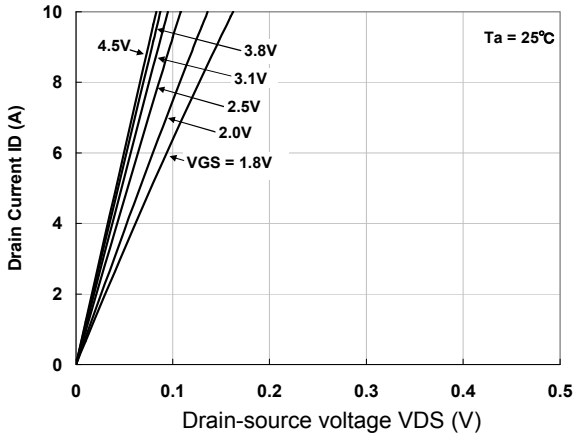
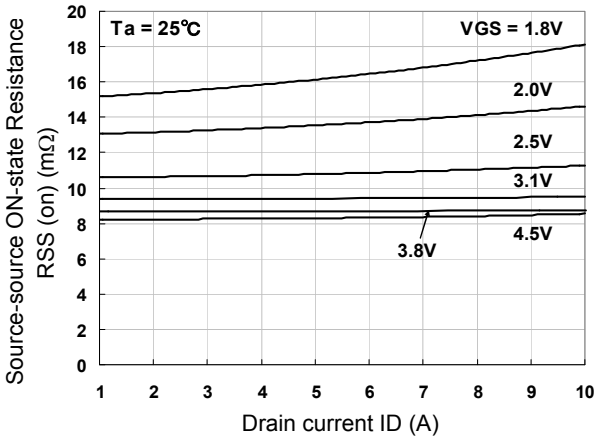
Technical Data (reference)

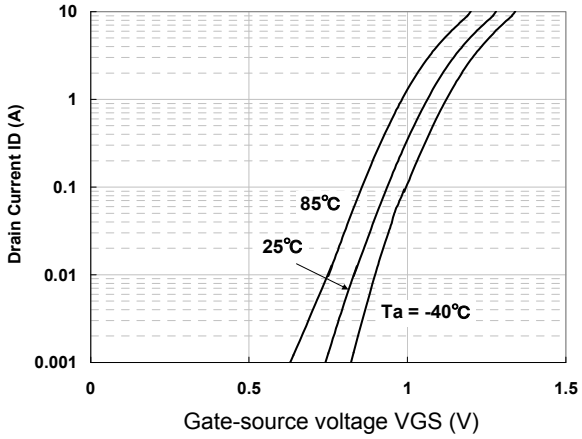
ID - VDS



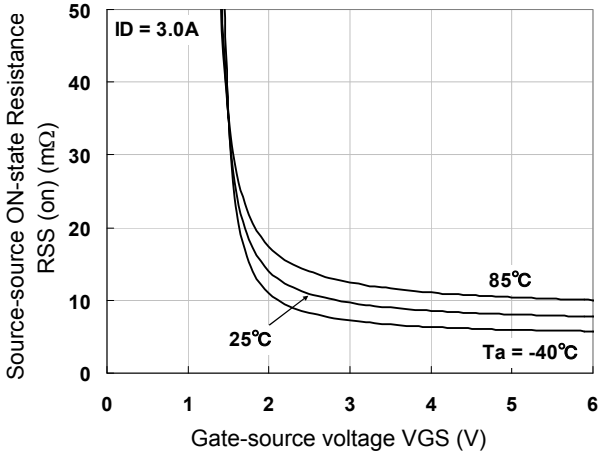
RDS(on) - ID



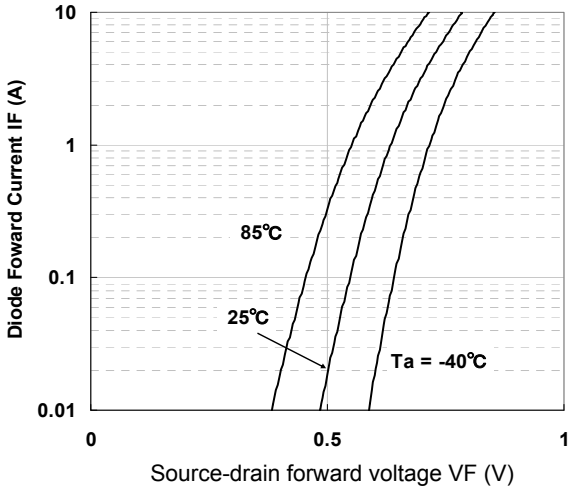
ID - VGS



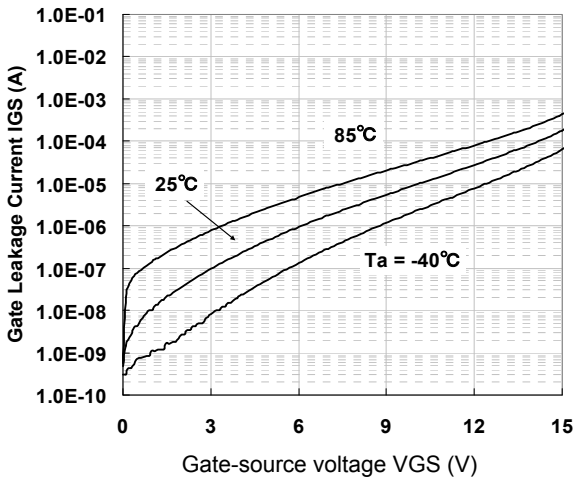
RDS(on) - VGS



IF - VF



IGS - VGS



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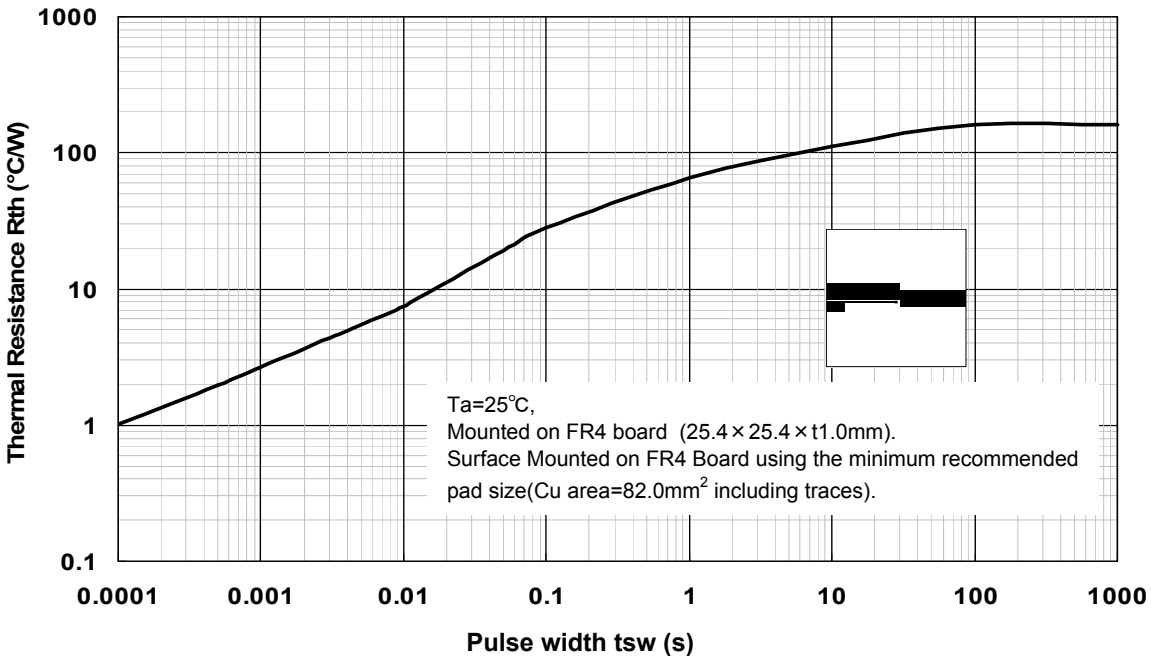
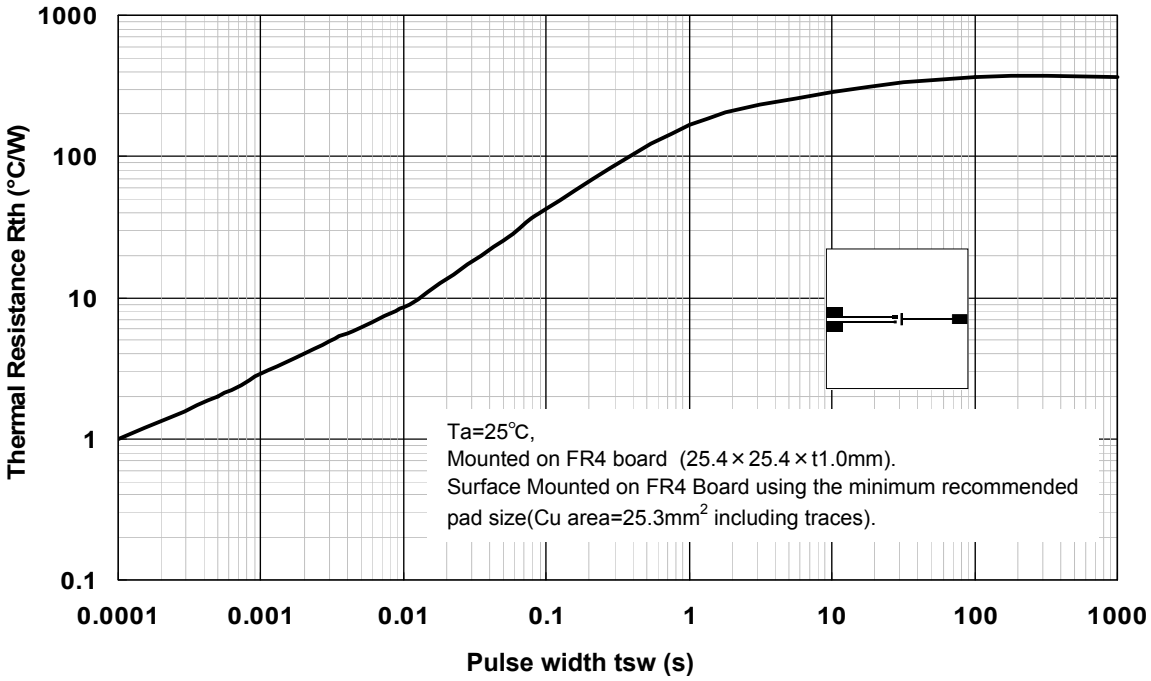
Technical Data (reference)

Rth - tsw



Rth - tsw



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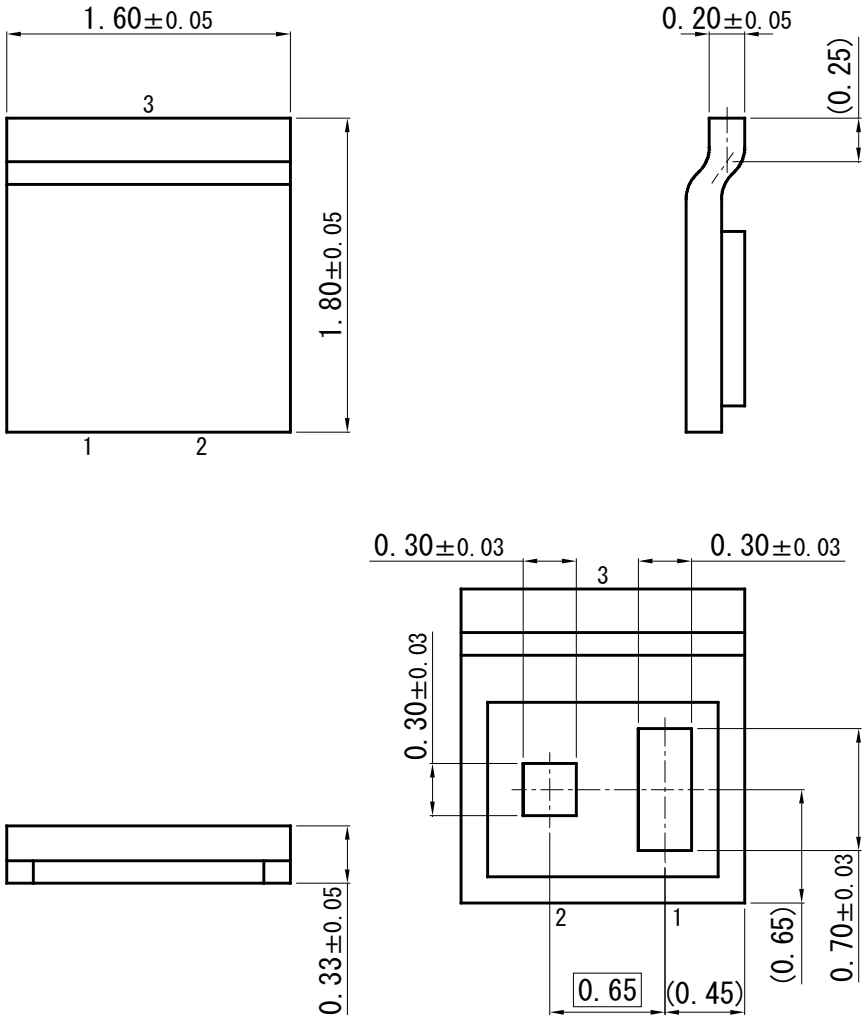
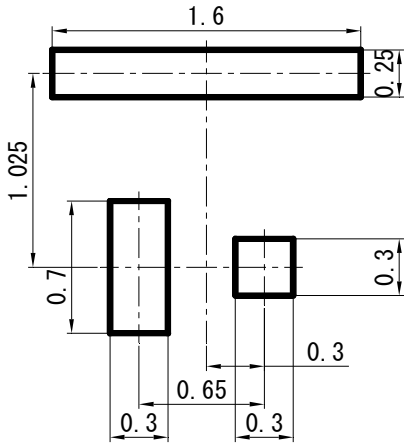
PMCP-1816-Z1

Unit: mm



■ Land Pattern (Reference) (Unit: mm)



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