

# NTR0202PL, NVTR0202PL

## Power MOSFET

-20 V, -400 mA, P-Channel  
SOT-23 Package



ON Semiconductor®

<http://onsemi.com>

### Features

- Low  $R_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life  
 $R_{DS(on)} = 0.80 \Omega$ ,  $V_{GS} = -10 \text{ V}$   
 $R_{DS(on)} = 1.10 \Omega$ ,  $V_{GS} = -4.5 \text{ V}$
- Miniature SOT-23 Surface Mount Package Saves Board Space
- AEC-Q101 Qualified and PPAP Capable – NVTR0202PL
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- DC-DC Converters
- Computers
- Printers
- PCMCIA Cards
- Cellular and Cordless Telephones

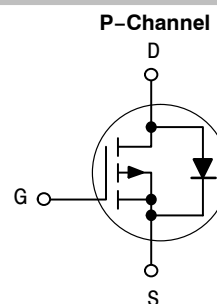
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-20	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	V
Continuous Drain Current @ $T_A = 25^\circ\text{C}$ Pulsed Drain Current ( $t_p \leq 10 \mu\text{s}$ )	$I_D$ $I_{DM}$	-0.4 -1.0	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)	$P_D$	225	mW
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Thermal Resistance – Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Source Current (Body Diode)	$I_S$	0.4	A
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 s	$T_L$	260	$^\circ\text{C}$

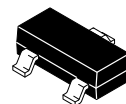
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

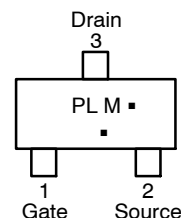
$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	$I_D$ MAX
-20 V	550 m $\Omega$ @ -10 V	-400 mA



### MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23  
CASE 318  
STYLE 21



PL = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
NTR0202PLT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel
NTR0202PLT3G	SOT-23 (Pb-Free)	10000 / Tape & Reel
NVTR0202PLT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTR0202PL, NVTR0202PL

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage ( $V_{GS} = 0\text{ V}$ , $I_D = -10\ \mu\text{A}$ ) (Positive Temperature Coefficient)	$V_{(BR)DSS}$	-20	33		V mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ( $V_{DS} = -20\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 25^\circ\text{C}$ ) ( $V_{DS} = -20\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 150^\circ\text{C}$ )	$I_{DSS}$			-1.0 -10	$\mu\text{A}$
Gate-Body Leakage Current ( $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$ )	$I_{GSS}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = -250\ \mu\text{A}$ ) (Negative Temperature Coefficient)	$V_{GS(th)}$	-1.1	-1.9 3.0	-2.3	V mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance ( $V_{GS} = -10\text{ V}$ , $I_D = -200\text{ mA}$ ) ( $V_{GS} = -4.5\text{ V}$ , $I_D = -50\text{ mA}$ )	$R_{DS(on)}$		0.55 0.80	0.80 1.10	$\Omega$
Forward Transconductance ( $V_{DS} = -10\text{ V}$ , $I_D = -200\text{ mA}$ )	$g_{fs}$		0.5		Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = -5.0\text{ V}$ , $V_{GS} = 0\text{ V}$ , $F = 1.0\text{ MHz})$	$C_{iss}$	70		pF
Output Capacitance		$C_{oss}$	74		
Reverse Transfer Capacitance		$C_{rss}$	26		

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$(V_{DD} = -15\text{ V}$ , $I_D = -200\text{ mA}$ , $V_{GS} = -10\text{ V}$ , $R_G = 6.0\ \Omega)$	$t_{d(on)}$	3.0		ns
Rise Time		$t_r$	6.0		
Turn-Off Delay Time		$t_{d(off)}$	18		
Fall Time		$t_f$	4		
Total Gate Charge	$(V_{DS} = -15\text{ V}$ , $I_D = -200\text{ mA}$ , $V_{GS} = -10\text{ V})$	$Q_{TOT}$	2.18		nC
Gate-Source Charge		$Q_{GS}$	0.41		
Gate-Drain Charge		$Q_{GD}$	0.40		

### BODY-DRAIN DIODE CHARACTERISTICS (Note 2)

Diode Forward Voltage (Note 2) ( $I_S = -400\text{ mA}$ , $V_{GS} = 0\text{ V}$ ) ( $I_S = -400\text{ mA}$ , $V_{GS} = 0\text{ V}$ , $T_J = 150^\circ\text{C}$ )	$V_{SD}$		-0.8 -0.65	-1.0	V
Reverse Recovery Time	$(I_S = -1.0\text{ A}$ , $V_{GS} = 0\text{ V}$ , $di_S/dt = 100\text{ A}/\mu\text{s})$	$t_{rr}$	11.8		ns
		$t_a$	9		
		$t_b$	3		
Reverse Recovery Stored Charge	$(I_S = -1.0\text{ A}$ , $V_{GS} = 0\text{ V}$ , $di_S/dt = 100\text{ A}/\mu\text{s})$	$Q_{RR}$	0.007		$\mu\text{C}$

2. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
3. Switching characteristics are independent of operating junction temperature.

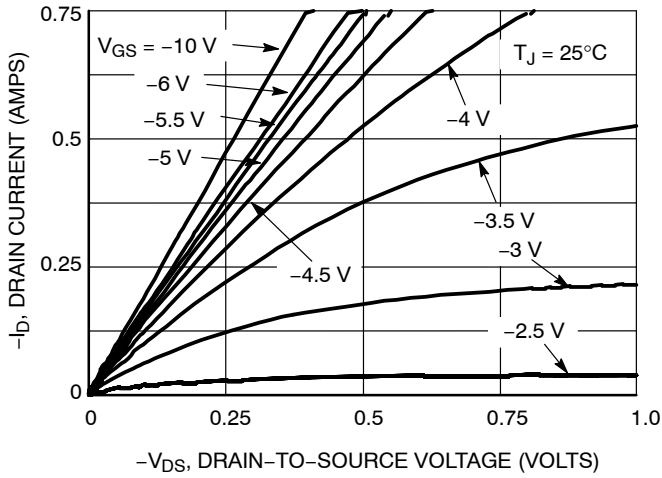


Figure 1. On-Region Characteristics

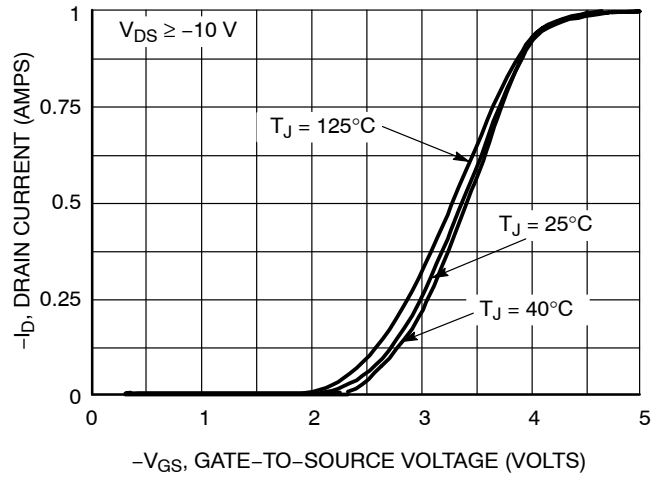


Figure 2. Transfer Characteristics

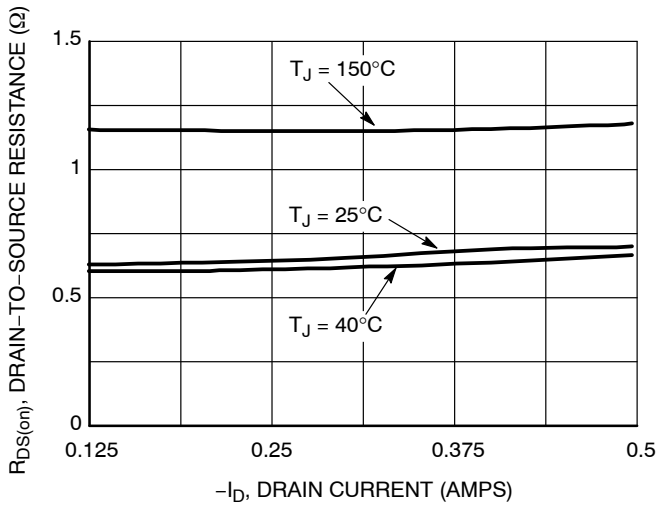


Figure 3. On-Resistance versus Drain Current

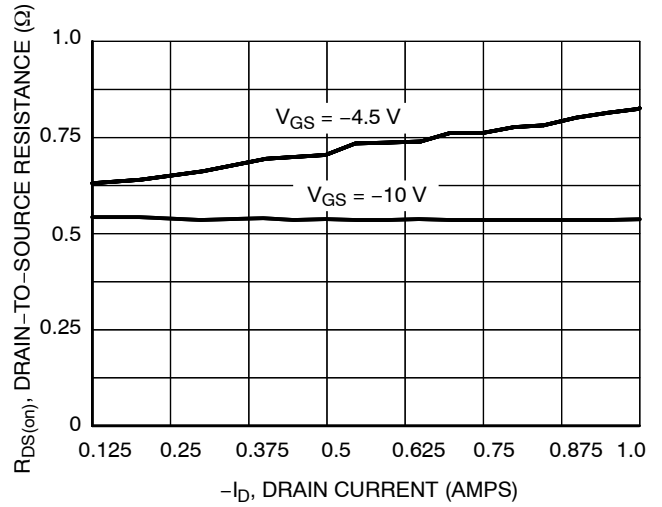


Figure 4. On-Resistance versus Drain Current and Gate Voltage

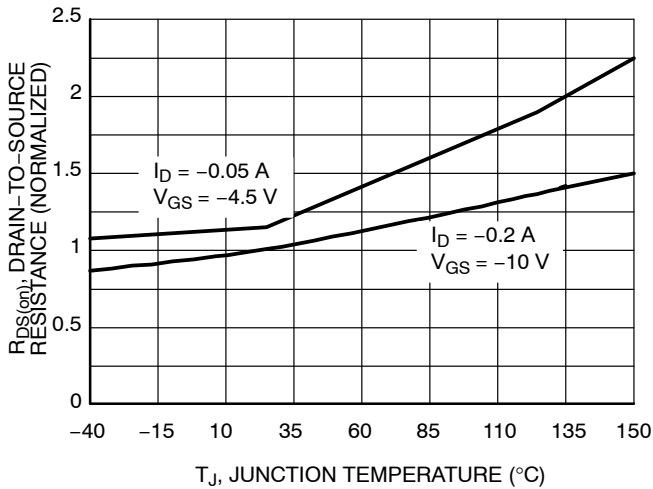


Figure 5. On-Resistance Variation with Temperature

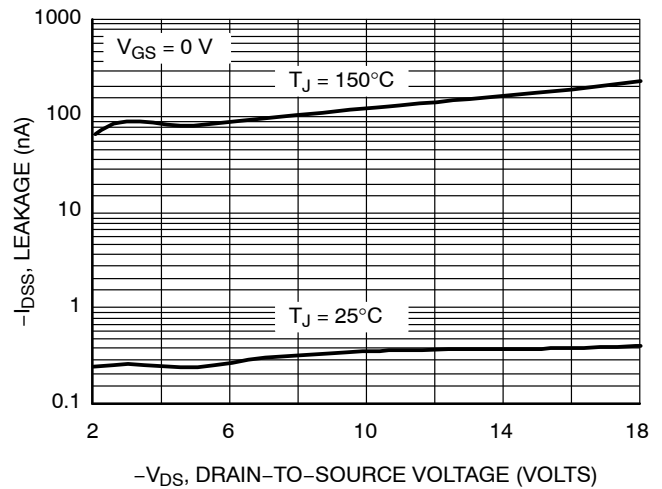


Figure 6. Drain-to-Source Leakage Current versus Voltage

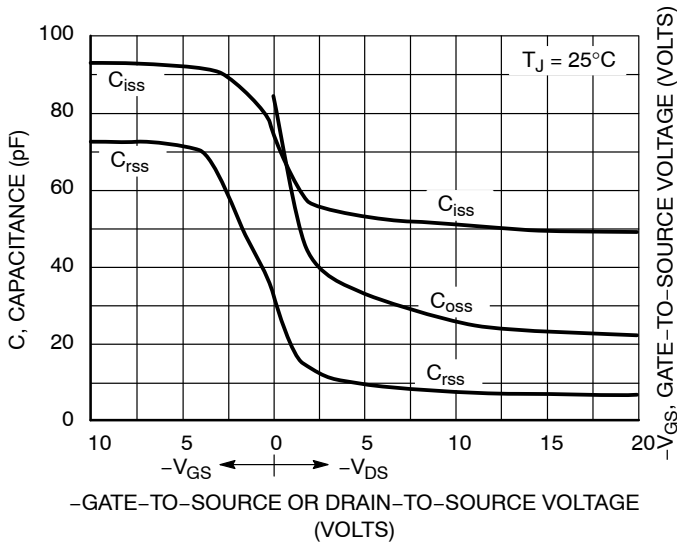


Figure 7. Capacitance Variation

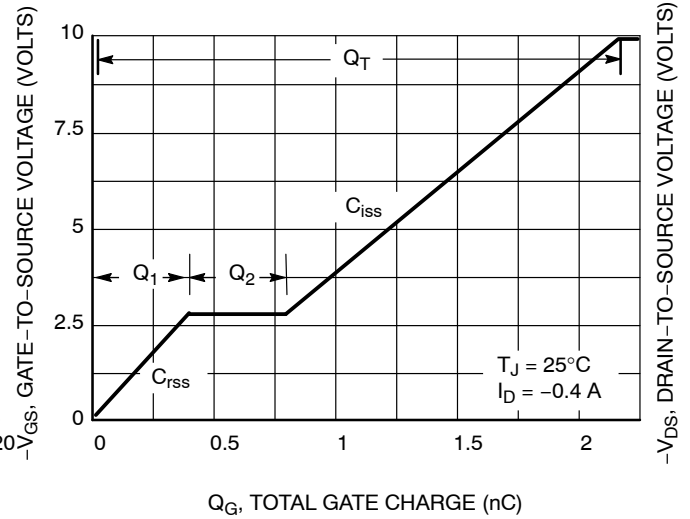


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Gate Charge

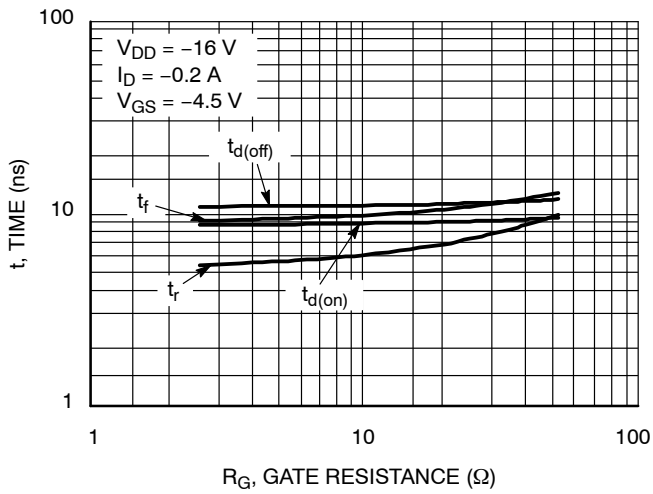


Figure 9. Resistive Switching Time Variation versus Gate Resistance

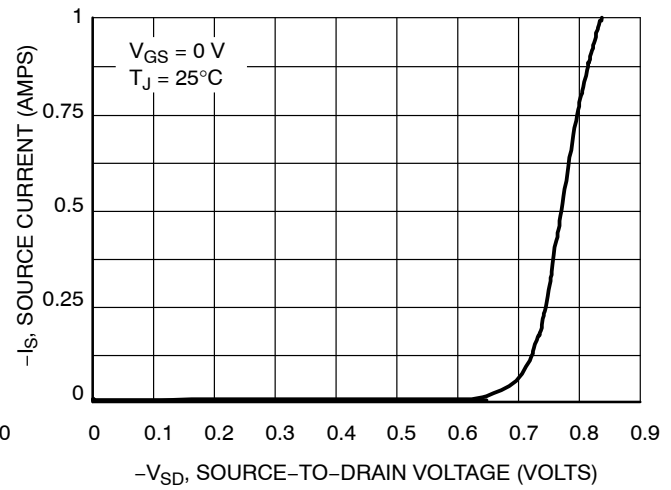
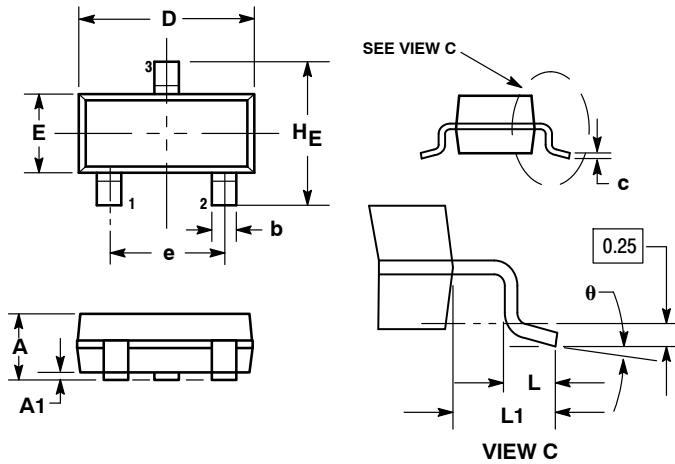


Figure 10. Diode Forward Voltage versus Current

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## PACKAGE DIMENSIONS

SOT-23 (TO-236)  
CASE 318-08  
ISSUE AP



NOTES:

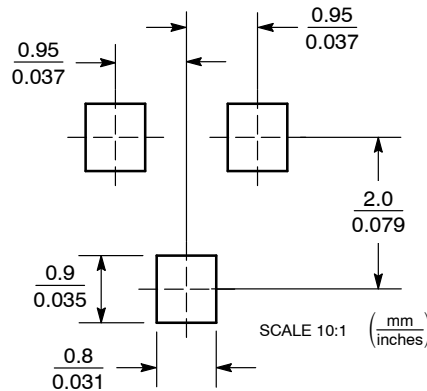
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

STYLE 21:

1. GATE
2. SOURCE
3. DRAIN

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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