MMJT350T1G

Bipolar Power Transistors

PNP Silicon

Bipolar power transistors are designed for use in line−operated applications such as low power, line−operated series pass and switching regulators requiring PNP capability.

Features

- High Collector−Emitter Sustaining Voltage
- Excellent DC Current Gain
- Epoxy Meets UL 94 V−0 @ 0.125 in
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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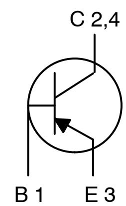
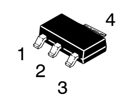
0.5 AMPERE
POWER TRANSISTOR
PNP SILICON
300 VOLTS, 2.75 WATTS

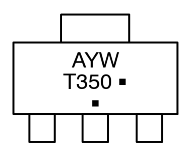


Schematic



SOT−223
CASE 318E
STYLE 1

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package
T350	= Device Code

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MMJT350T1G	SOT−223 (Pb−Free)	1,000 / Tape & Reel
SMMJT350T1G	SOT−223 (Pb−Free)	1,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	300	Vdc
Collector−Base Voltage	V_{CB}	300	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous	I_C	0.5	Adc
Collector Current − Peak	I_{CM}	0.75	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total P_D @ T_A = 25°C mounted on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material Total P_D @ T_A = 25°C mounted on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	P_D	 2.75 22 1.40 0.65	 W mW/°C W W
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C
ESD − Human Body Model	HBM	3B	V
ESD − Machine Model	MM	C	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction−to−Case Junction−to−Ambient on 1” sq. (645 sq. mm) Collector pad on FR−4 bd material Junction−to−Ambient on 0.012” sq. (7.6 sq. mm) Collector pad on FR−4 bd material	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 45 85 190	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8” from case for 5 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (I_C = 1.0 mAdc, I_B = 0 Adc)	$V_{CEO(SUS)}$	300	–	Vdc
Collector−Base Current (V_{CB} = Rated V_{CBO}, V_{EB} = 0)	I_{CBO}	–	100	nAdc
Emitter Cut−off Current (V_{BE} = 5.0 Vdc)	I_{EBO}	–	100	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 50 mAdc, V_{CE} = 10 Vdc) (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 30 20	 240 –	–

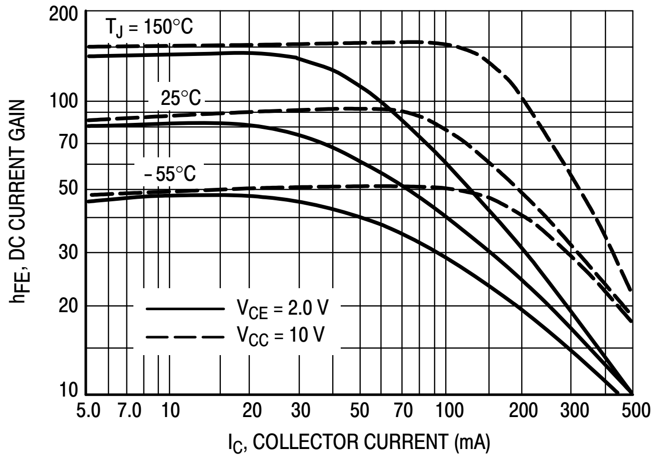


Figure 1. DC Current Gain

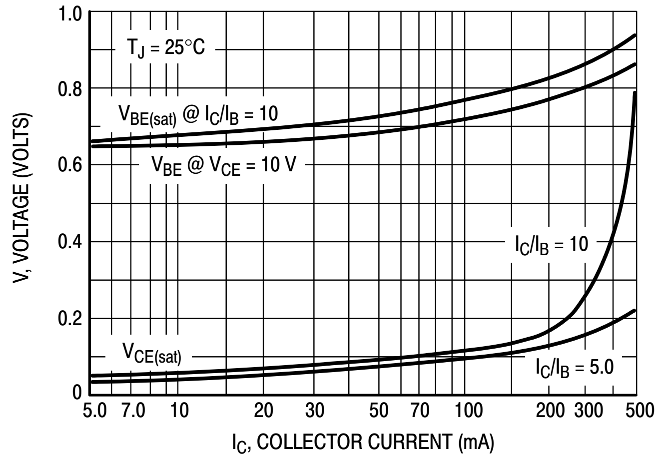


Figure 2. “On” Voltages

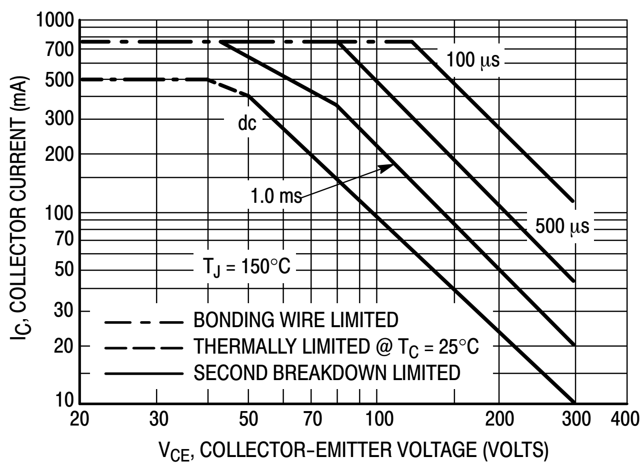


Figure 3. Active−Region Safe Operating Area

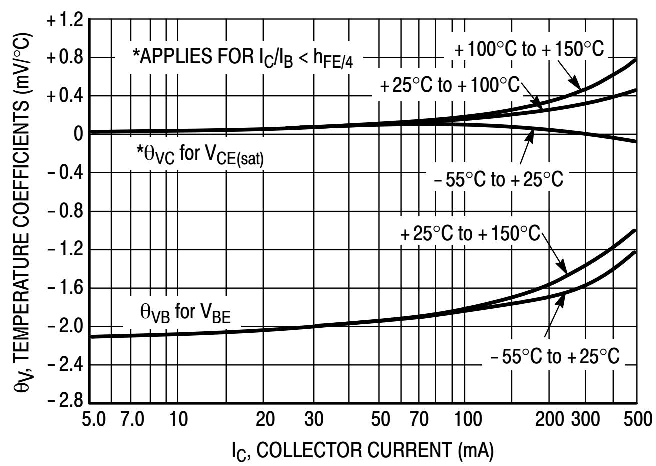


Figure 4. Temperature Coefficients

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 3 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150$°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

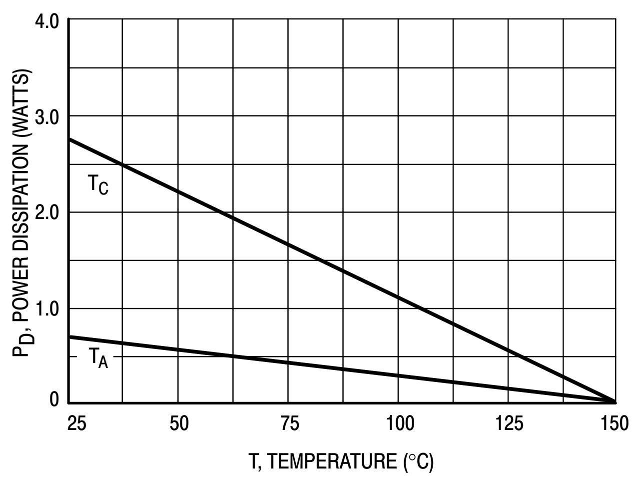
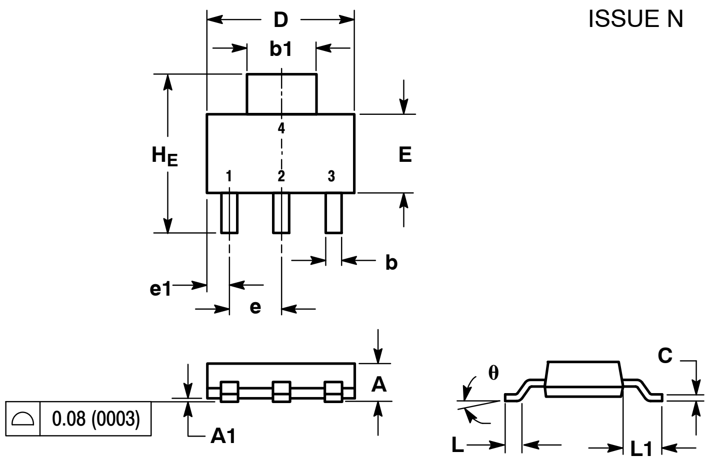


Figure 5. Power Derating

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE N

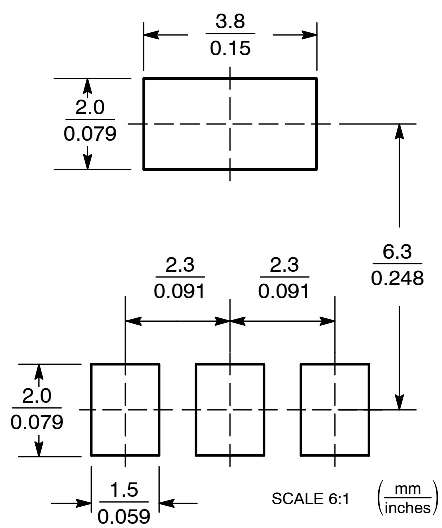


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	−−−	−−−	0.008	−−−	−−−
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	−	10°	0°	−	10°

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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