

# MUN5215DW1, NSBC114TDXV6, NSBC114TDP6

## Dual NPN Bias Resistor Transistors R1 = 10 kΩ, R2 = ∞ kΩ

### NPN Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable\*
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS

(T<sub>A</sub> = 25°C, common for Q1 and Q2, unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V <sub>CBO</sub>	50	Vdc
Collector-Emitter Voltage	V <sub>CEO</sub>	50	Vdc
Collector Current - Continuous	I <sub>C</sub>	100	mAdc
Input Forward Voltage	V <sub>IN(fwd)</sub>	40	Vdc
Input Reverse Voltage	V <sub>IN(rev)</sub>	6	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

#### ORDERING INFORMATION

Device	Package	Shipping†
MUN5215DW1T1G	SOT-363	3,000 / Tape & Reel
NSVMUN5215DW1T1G*	SOT-363	3,000 / Tape & Reel
NSBC114TDXV6T1G	SOT-563	4,000 / Tape & Reel
NSBC114TDXV6T5G	SOT-563	8,000 / Tape & Reel
NSBC114TDP6T5G	SOT-963	8,000 / Tape & Reel

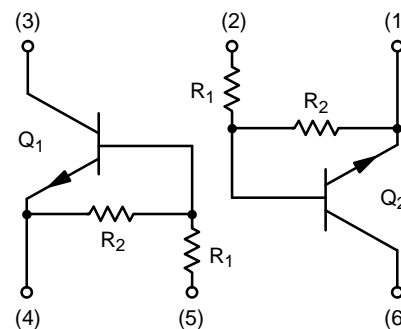
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



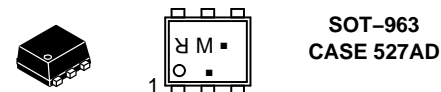
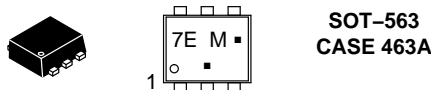
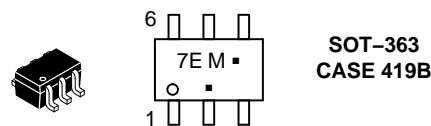
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#### PIN CONNECTIONS



#### MARKING DIAGRAMS



7E/R = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

# MUN5215DW1, NSBC114TDXV6, NSBC114TDP6

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
<b>MUN5215DW1 (SOT-363) One Junction Heated</b>			
Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	187	mW
Derate above $25^\circ\text{C}$		256	$\text{mW}/^\circ\text{C}$
		1.5	
		2.0	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	670	$^\circ\text{C}/\text{W}$
		490	

### MUN5215DW1 (SOT-363) Both Junction Heated (Note 3)

Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	250	mW
Derate above $25^\circ\text{C}$		385	$\text{mW}/^\circ\text{C}$
		2.0	
		3.0	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	493	$^\circ\text{C}/\text{W}$
		325	
Thermal Resistance, Junction to Lead	$R_{\theta JL}$	188	$^\circ\text{C}/\text{W}$
		208	
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

### NSBC114TDXV6 (SOT-563) One Junction Heated

Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	357	mW
Derate above $25^\circ\text{C}$		2.9	$\text{mW}/^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	350	$^\circ\text{C}/\text{W}$

### NSBC114TDXV6 (SOT-563) Both Junction Heated (Note 3)

Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	500	mW
Derate above $25^\circ\text{C}$		4.0	$\text{mW}/^\circ\text{C}$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	250	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

### NSBC114TDP6 (SOT-963) One Junction Heated

Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	231	mW
Derate above $25^\circ\text{C}$		269	$\text{mW}/^\circ\text{C}$
		1.9	
		2.2	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	540	$^\circ\text{C}/\text{W}$
		464	

### NSBC114TDP6 (SOT-963) Both Junction Heated (Note 3)

Total Device Dissipation $T_A = 25^\circ\text{C}$	$P_D$	339	mW
Derate above $25^\circ\text{C}$		408	$\text{mW}/^\circ\text{C}$
		2.7	
		3.3	
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	369	$^\circ\text{C}/\text{W}$
		306	
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 x 1.0 Inch Pad.
3. Both junction heated values assume total power is sum of two equally powered channels.
4. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces, still air.
5. FR-4 @ 500 mm<sup>2</sup>, 1 oz. copper traces, still air.

# MUN5215DW1, NSBC114TDXV6, NSBC114TDP6

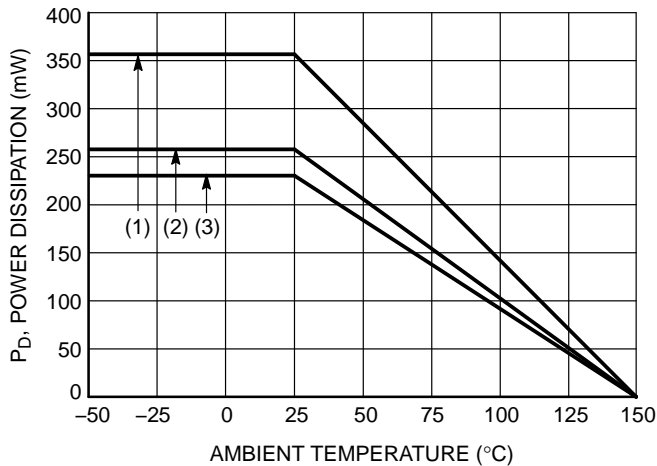
## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, common for Q<sub>1</sub> and Q<sub>2</sub>, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	100	nAdc
Collector–Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	500	nAdc
Emitter–Base Cutoff Current (V <sub>EB</sub> = 6.0 V, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	0.9	mAdc
Collector–Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (Note 6) (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	–	–	Vdc

## ON CHARACTERISTICS

DC Current Gain (Note 6) (I <sub>C</sub> = 5.0 mA, V <sub>CE</sub> = 10 V)	h <sub>FE</sub>	160	350	–	
Collector–Emitter Saturation Voltage (Note 6) (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 1.0 mA)	V <sub>CE(sat)</sub>	–	–	0.25	Vdc
Input Voltage (off) (V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 100 μA)	V <sub>i(off)</sub>	–	0.6	–	Vdc
Input Voltage (on) (V <sub>CE</sub> = 0.2 V, I <sub>C</sub> = 10 mA)	V <sub>i(on)</sub>	–	1.4	–	Vdc
Output Voltage (on) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 2.5 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OL</sub>	–	–	0.2	Vdc
Output Voltage (off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.25 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OH</sub>	4.9	–	–	Vdc
Input Resistor	R <sub>1</sub>	7.0	10	13	kΩ
Resistor Ratio	R <sub>1</sub> /R <sub>2</sub>	–	–	–	

6. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.



- (1) SOT–363; 1.0 x 1.0 inch Pad
- (2) SOT–563; Minimum Pad
- (3) SOT–963; 100 mm<sup>2</sup>, 1 oz. copper trace

Figure 1. Derating Curve

TYPICAL CHARACTERISTICS  
MUN5215DW1, NSBC114TDXV6

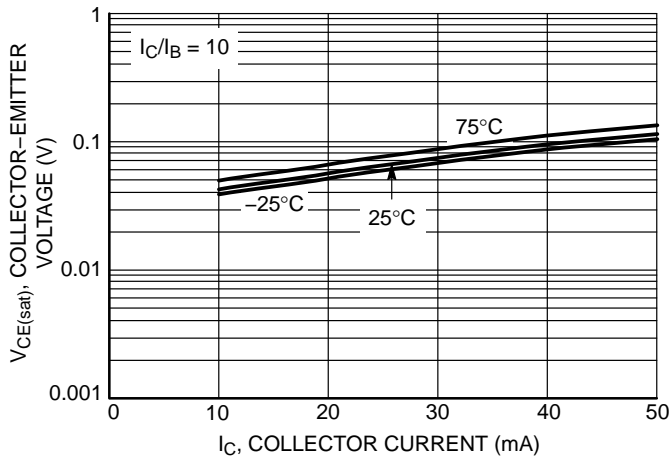


Figure 2.  $V_{CE(sat)}$  vs.  $I_C$

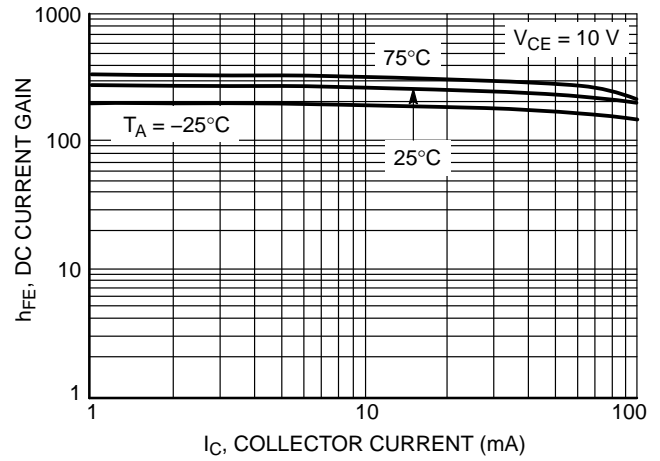


Figure 3. DC Current Gain

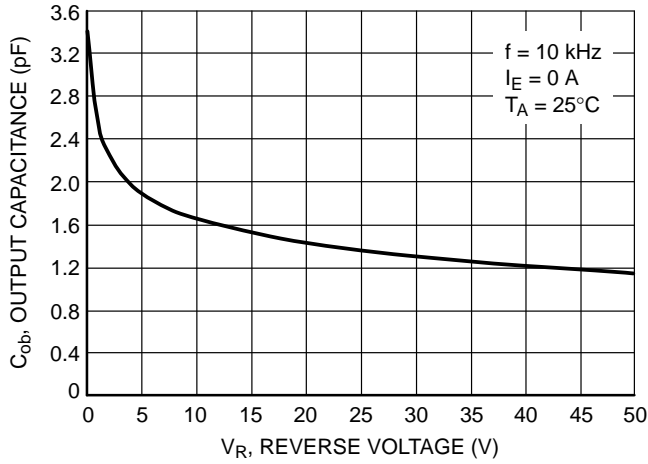


Figure 4. Output Capacitance

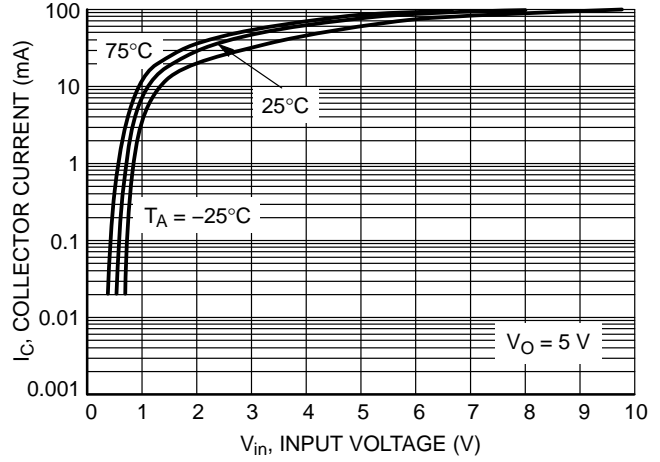


Figure 5. Output Current vs. Input Voltage

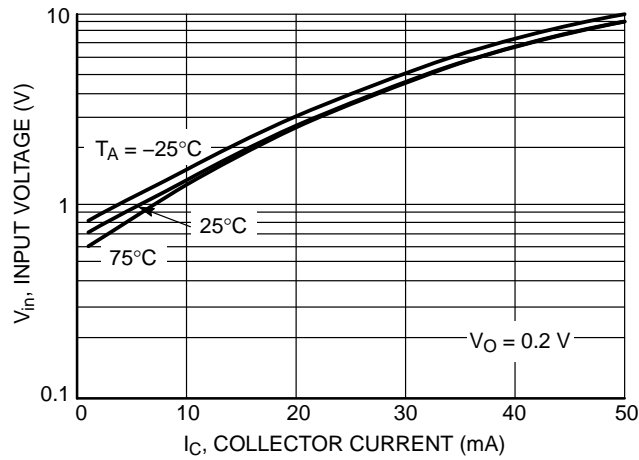


Figure 6. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS – NSBC114TF3

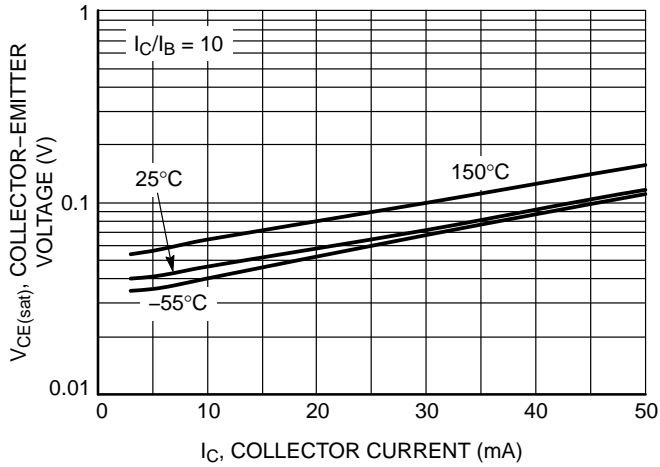


Figure 7.  $V_{CE(sat)}$  vs.  $I_C$

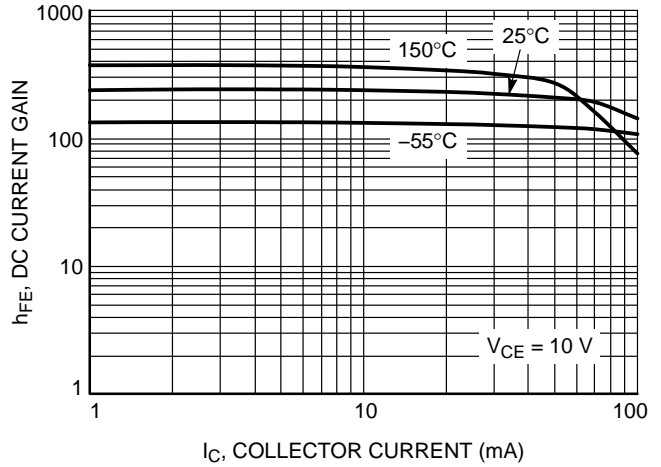


Figure 8. DC Current Gain

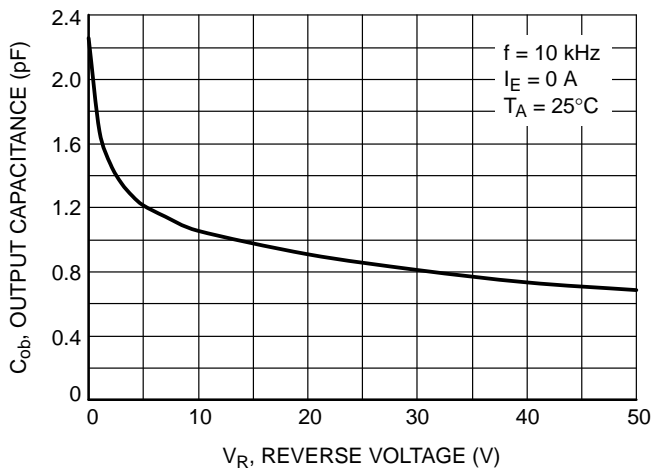


Figure 9. Output Capacitance

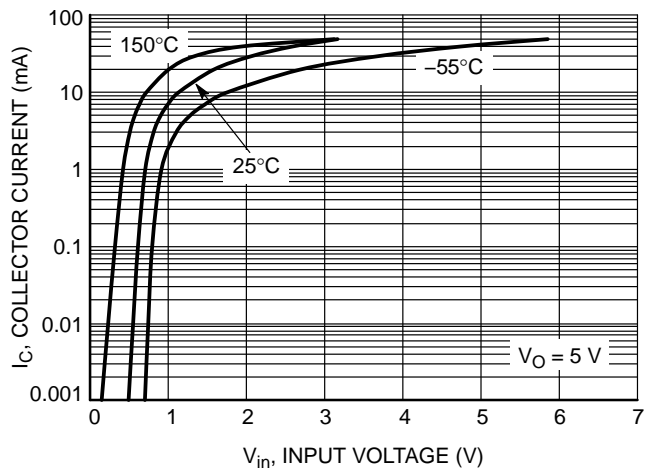


Figure 10. Output Current vs. Input Voltage

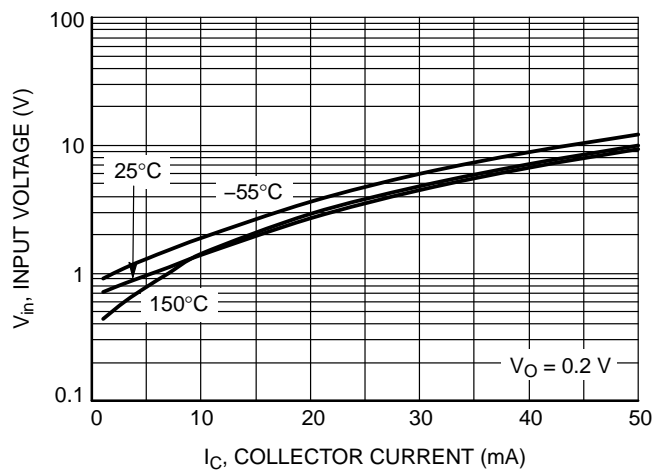
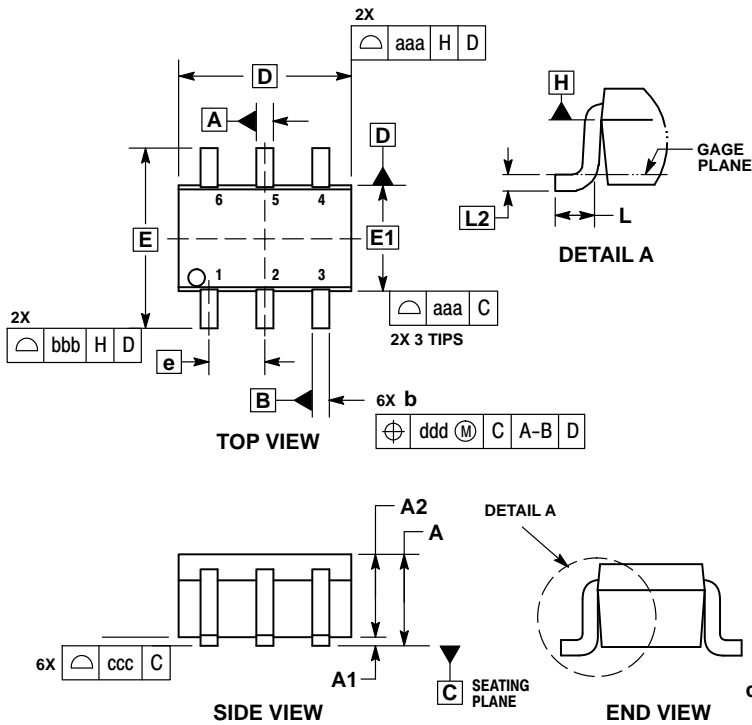


Figure 11. Input Voltage vs. Output Current

# MUN5215DW1, NSBC114TDXV6, NSBC114TDP6

## PACKAGE DIMENSIONS

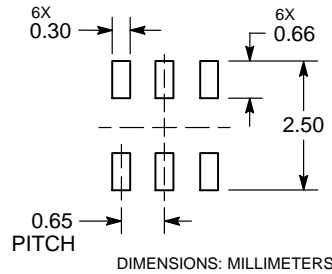
SC-88/SC70-6/SOT-363  
CASE 419B-02  
ISSUE Y



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
  4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
  5. DATUMS A AND B ARE DETERMINED AT DATUM H.
  6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
  7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.00	---	0.10	0.000	---	0.004
A2	0.70	0.90	1.00	0.027	0.035	0.039
b	0.15	0.20	0.25	0.006	0.008	0.010
C	0.08	0.15	0.22	0.003	0.006	0.009
D	1.80	2.00	2.20	0.070	0.078	0.086
E	2.00	2.10	2.20	0.078	0.082	0.086
E1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.26	0.36	0.46	0.010	0.014	0.018
L2	0.15 BSC			0.006 BSC		
aaa	0.15			0.006		
bbb	0.30			0.012		
ccc	0.10			0.004		
ddd	0.10			0.004		

### RECOMMENDED SOLDERING FOOTPRINT\*

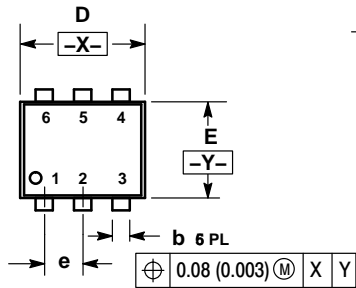


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MUN5215DW1, NSBC114TDXV6, NSBC114TDP6

## PACKAGE DIMENSIONS

SOT-563, 6 LEAD  
CASE 463A  
ISSUE F

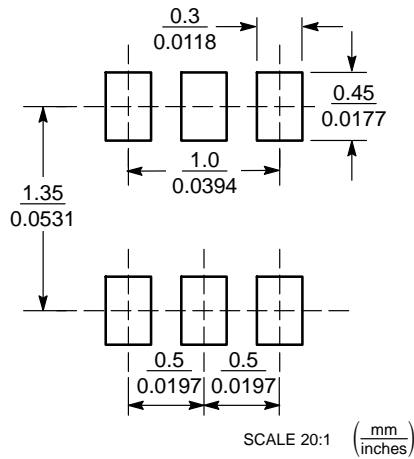


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H <sub>E</sub>	1.50	1.60	1.70	0.059	0.062	0.066

### SOLDERING FOOTPRINT\*

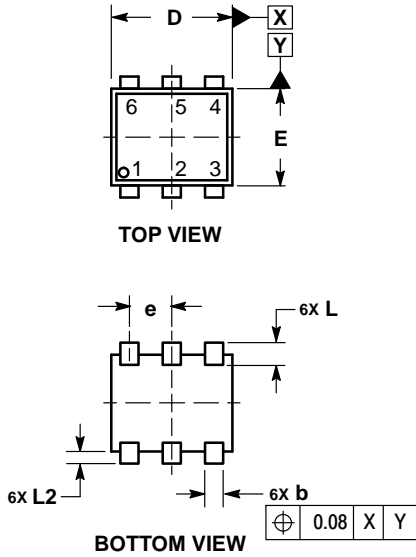


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MUN5215DW1, NSBC114TDXV6, NSBC114TDP6

## PACKAGE DIMENSIONS

SOT-963  
CASE 527AD  
ISSUE E

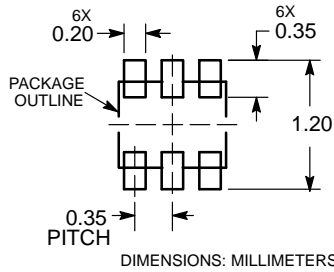


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
He	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15

### RECOMMENDED MOUNTING FOOTPRINT



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