
# PSMN2R5-30YL

## N-channel 30 V 2.4 mΩ logic level MOSFET in LFPAK

Rev. 04 — 10 March 2011 Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in industrial and communications applications.

### 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

### 1.3 Applications

- Class-D amplifiers
- DC-to-DC converters
- Motor control
- Server power supplies

### 1.4 Quick reference data

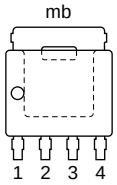
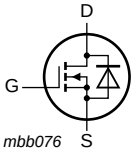
**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | - | 30 | V |
| $I_D$ | drain current | $T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1 | [1] | - | - | 100 | A |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25$ °C; see Figure 2 | | - | - | 88 | W |
| $T_j$ | junction temperature | | | -55 | - | 175 | °C |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 10$ V; $I_D = 15$ A; $T_j = 25$ °C | | - | 1.79 | 2.4 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS} = 4.5$ V; $I_D = 10$ A; $V_{DS} = 12$ V; see Figure 14; see Figure 15 | | - | 6.5 | - | nC |
| $Q_{G(tot)}$ | total gate charge | | | - | 27 | - | nC |
| **Avalanche ruggedness** | | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 100$ A; $V_{sup} \leq 30$ V; $R_{GS} = 50$ Ω; unclamped | | - | - | 103 | mJ |

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source |  |  |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |



**SOT669 (LFPAK)**

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN2R5-30YL | LFPAK | plastic single-ended surface-mounted package (LFPAK); 4 leads | SOT669 |

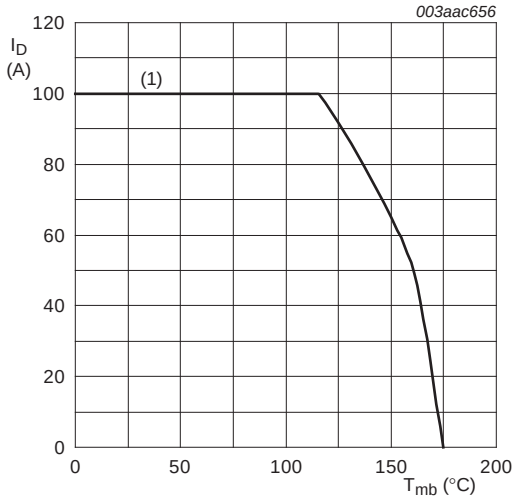
## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

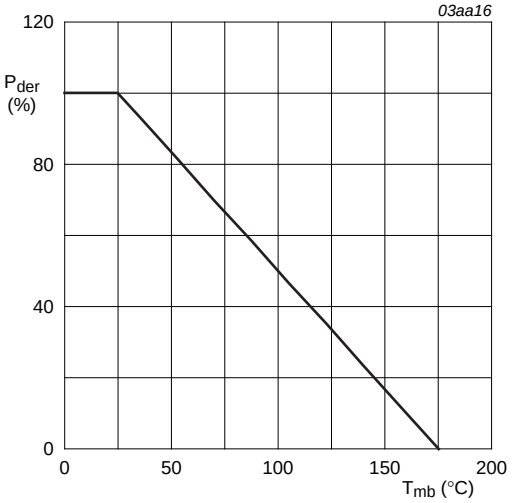
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | 30 | V |
| $V_{DSM}$ | peak drain-source voltage | $t_p \leq 25$ ns; f ≤ 500 kHz; $E_{DS(AL)} \leq 240$ nJ; pulsed | | - | 35 | V |
| $V_{DGR}$ | drain-gate voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C; $R_{GS}$ = 20 kΩ | | - | 30 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{mb}$ = 100 °C; see Figure 1 | [1] | - | 100 | A |
| | | $V_{GS}$ = 10 V; $T_{mb}$ = 25 °C; see Figure 1 | [1] | - | 100 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p \leq 10$ µs; $T_{mb}$ = 25 °C; see Figure 3 | | - | 580 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; see Figure 2 | | - | 88 | W |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | [1] | - | 100 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq 10$ µs; $T_{mb}$ = 25 °C | | - | 580 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 100 A; $V_{sup} \leq 30$ V; $R_{GS}$ = 50 Ω; unclamped | | - | 103 | mJ |

[1] Continuous current is limited by package.



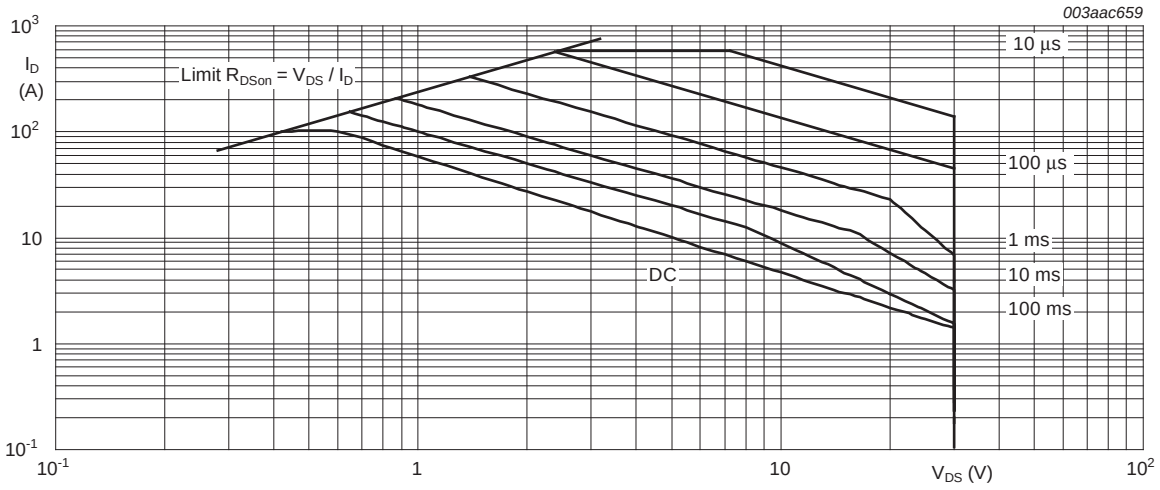

$V_{GS} \geq 10$ V; (1) Capped at 100 A due to package.

**Fig 1. Continuous drain current as a function of mounting base temperature**




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**




$V_{GS} \geq 10\,V$

(1) Capped at 100 A due to package.

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | - | 1.4 | K/W |

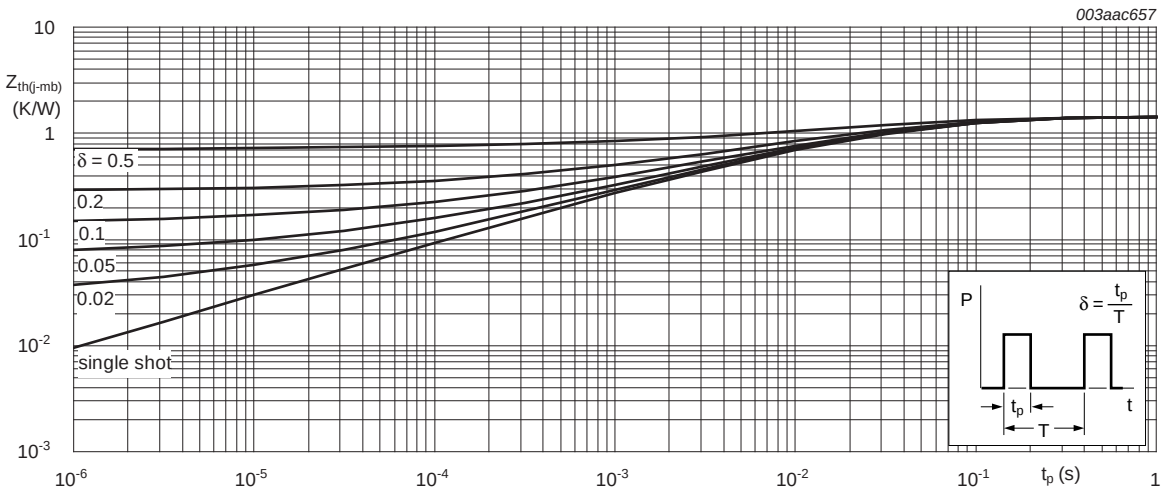



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

**Table 6. Characteristics**

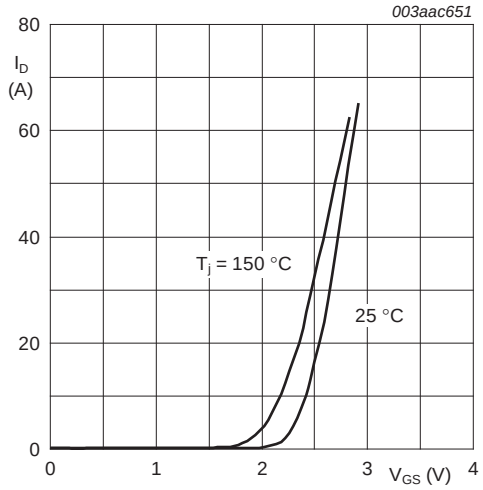
*Tested to JEDEC standards where applicable.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | 30 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 11; see Figure 12 | 1.3 | 1.7 | 2.15 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 150 °C; see Figure 12 | 0.65 | - | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; see Figure 12 | - | - | 2.45 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | - | 1 | µA |
| | | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V; $T_j$ = 150 °C | - | - | 100 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | - | 100 | nA |
| | | $V_{GS}$ = -16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | - | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 4.5 V; $I_D$ = 15 A; $T_j$ = 25 °C | - | 2.47 | 3.16 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 15 A; $T_j$ = 150 °C; see Figure 13 | - | - | 4.2 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 15 A; $T_j$ = 25 °C | - | 1.79 | 2.4 | mΩ |
| $R_G$ | gate resistance | f = 1 MHz | - | 0.67 | 1.5 | Ω |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 10 A; $V_{DS}$ = 12 V; $V_{GS}$ = 4.5 V; see Figure 14; see Figure 15 | - | 27 | - | nC |
| | | $I_D$ = 0 A; $V_{DS}$ = 0 V; $V_{GS}$ = 10 V | - | 52 | - | nC |
| | | $I_D$ = 10 A; $V_{DS}$ = 12 V; $V_{GS}$ = 10 V; see Figure 14; see Figure 15 | - | 57 | - | nC |
| $Q_{GS}$ | gate-source charge | $I_D$ = 10 A; $V_{DS}$ = 12 V; $V_{GS}$ = 4.5 V; see Figure 14; see Figure 15 | - | 8.5 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 5.7 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 2.8 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 6.5 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $V_{DS}$ = 12 V; see Figure 14; see Figure 15 | - | 2.35 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 12 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; see Figure 16 | - | 3468 | - | pF |
| $C_{oss}$ | output capacitance | | - | 710 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 314 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 12 V; $R_L$ = 0.5 Ω; $V_{GS}$ = 4.5 V; $R_{G(ext)}$ = 4.7 Ω | - | 39 | - | ns |
| $t_r$ | rise time | | - | 62 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 61 | - | ns |
| $t_f$ | fall time | | - | 25 | - | ns |

**Table 6. Characteristics** *...continued*

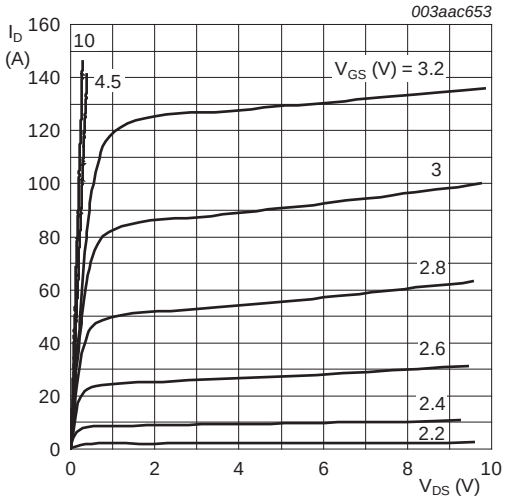
*Tested to JEDEC standards where applicable.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; see Figure 17 | - | 0.79 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V | - | 39 | - | ns |
| $Q_r$ | recovered charge | | - | 38 | - | nC |



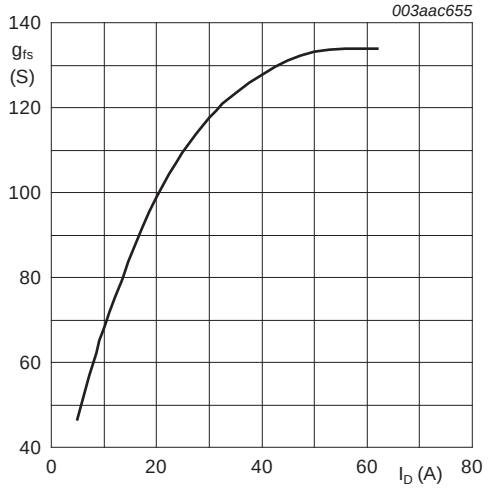

$V_{DS} = 10V$

**Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



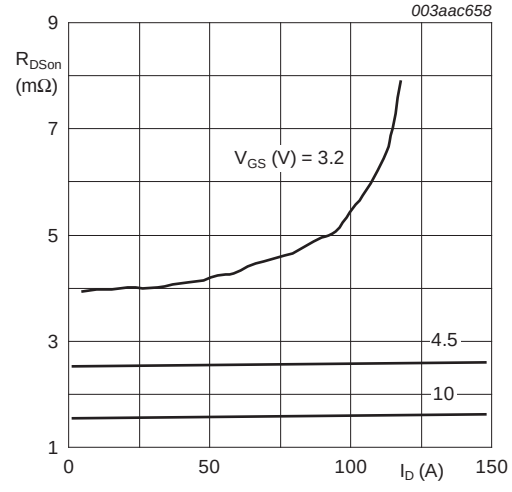

$T_j = 25\,°C;\ t_p = 300\mu s$

**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



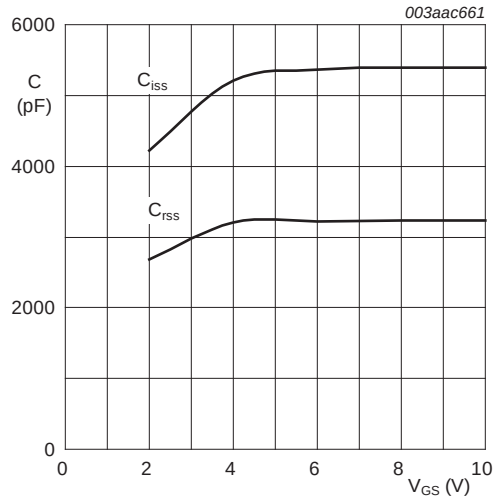

$T_j = 25\,°C; V_{DS} = 15V$

**Fig 7. Forward transconductance as a function of drain current; typical values**



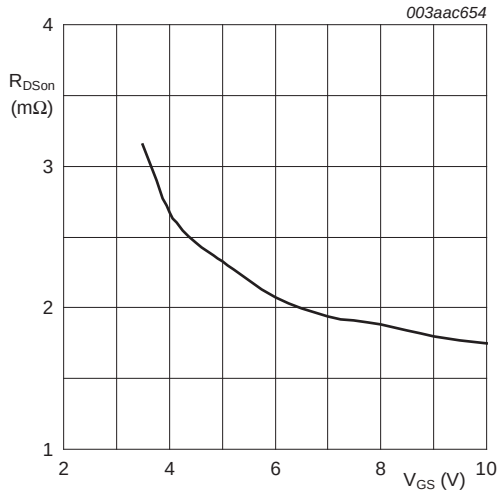

$T_j = 25\,°C;\ t_p = 300\mu s$

**Fig 8. Drain-source on-state resistance as a function of drain current; typical values**



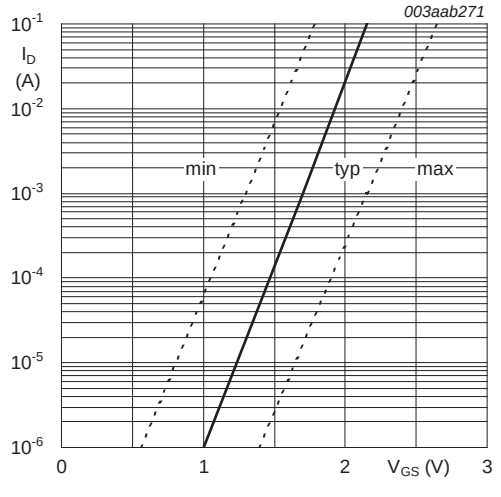

$V_{DS} = 0V; f = 1MHz$

**Fig 9. Input and reverse transfer capacitances as a function of gate-source voltage; typical values**



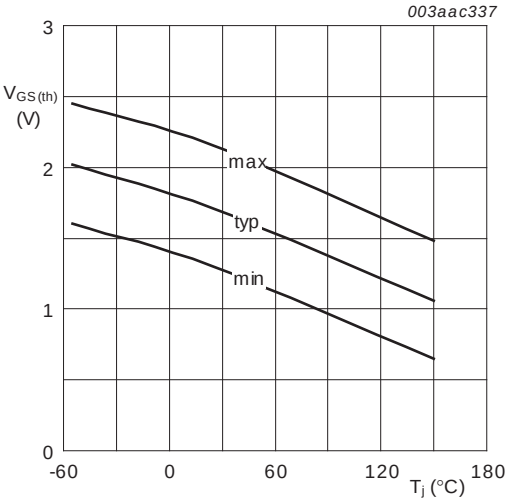

$T_j = 25°C; I_D = 15A$

**Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values**



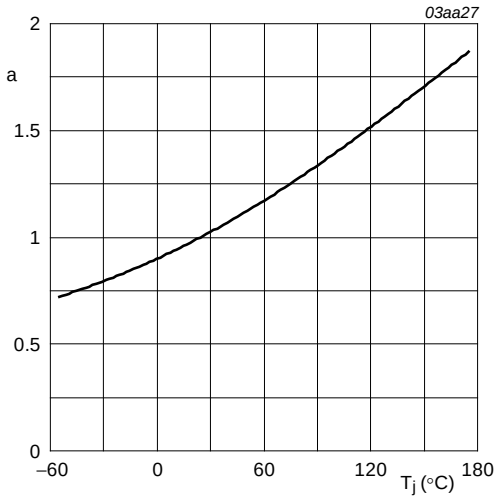

$T_j = 25°C; V_{DS} = 5V$

**Fig 11. Sub-threshold drain current as a function of gate-source voltage**




$I_D = 1mA; V_{DS} = V_{GS}$

**Fig 12. Gate-source threshold voltage as a function of junction temperature**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature**

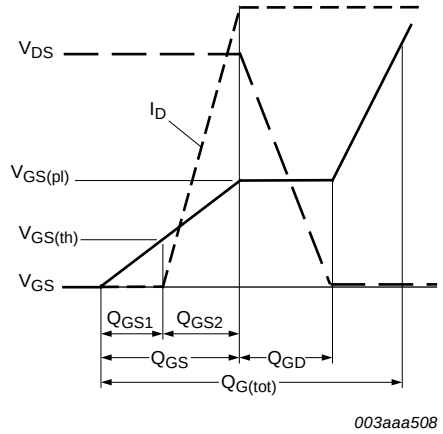
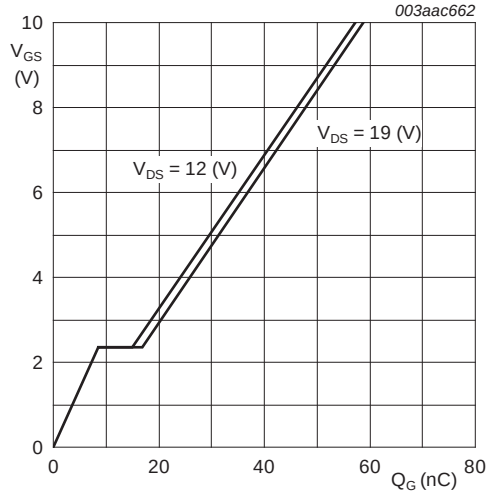
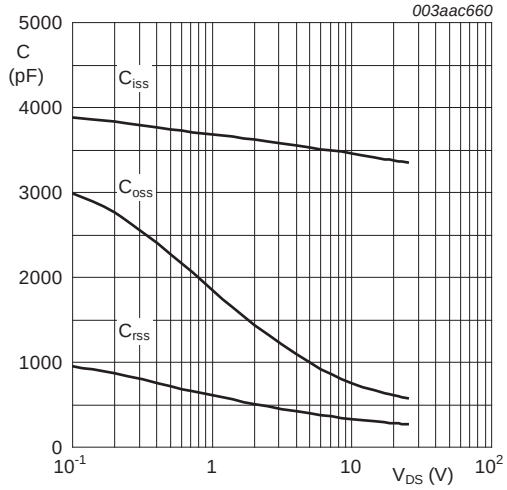



**Fig 14. Gate charge waveform definitions**



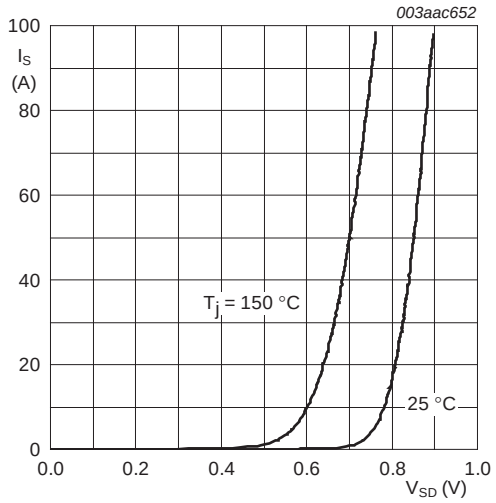

$$T_j = 25\,°C; I_D = 10\,A$$

**Fig 15. Gate-source voltage as a function of gate charge; typical values**




$$V_{GS} = 0\,V; f = 1\,MHz$$

**Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

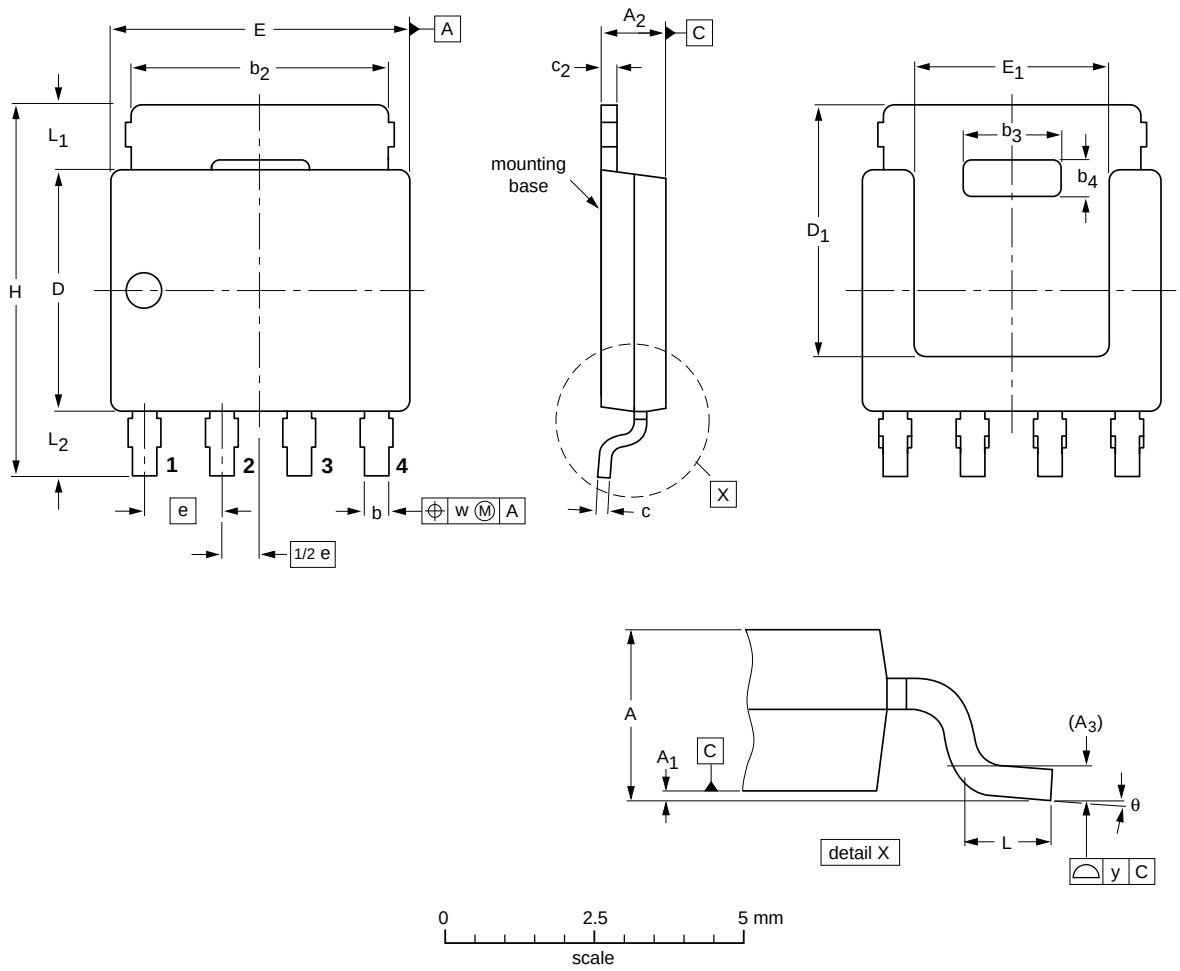



$V_{GS} = 0\,V$

**Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

# 7. Package outline

**Plastic single-ended surface-mounted package (LFPAK); 4 leads** **SOT669**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | $b_3$ | $b_4$ | c | $c_2$ | $D^{(1)}$ | $D_1^{(1)}$ max | $E^{(1)}$ | $E_1^{(1)}$ | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.20<br>1.01 | 0.15<br>0.00 | 1.10<br>0.95 | 0.25 | 0.50<br>0.35 | 4.41<br>3.62 | 2.2<br>2.0 | 0.9<br>0.7 | 0.25<br>0.19 | 0.30<br>0.24 | 4.10<br>3.80 | 4.20 | 5.0<br>4.8 | 3.3<br>3.1 | 1.27 | 6.2<br>5.8 | 0.85<br>0.40 | 1.3<br>0.8 | 1.3<br>0.8 | 0.25 | 0.1 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | ~~04-10-13~~<br>06-03-16 |

**Fig 18. Package outline SOT669 (LFPAK)**

## 8. Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PSMN2R5-30YL v.4 | 20110310 | Product data sheet | - | PSMN2R5-30YL v.3 |
| Modifications: | • Various changes to content. | | | |
| PSMN2R5-30YL v.3 | 20091228 | Product data sheet | - | PSMN2R5-30YL v.2 |

# 9. Legal information

## 9.1 Data sheet status

| Document status [1] [2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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