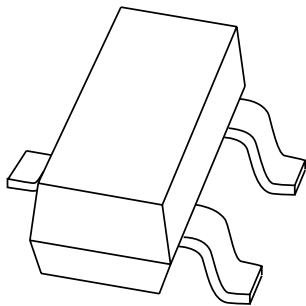


# DATA SHEET



## **BSH103**

**N-channel enhancement mode  
MOS transistor**

Product specification  
Supersedes data of 1998 Jan 30  
File under Discrete Semiconductors, SC13b

1998 Feb 11

# N-channel enhancement mode MOS transistor

**BSH103**

## FEATURES

- Very low threshold
- High-speed switching
- No secondary breakdown
- Direct interface to C-MOS, TTL etc.

## APPLICATIONS

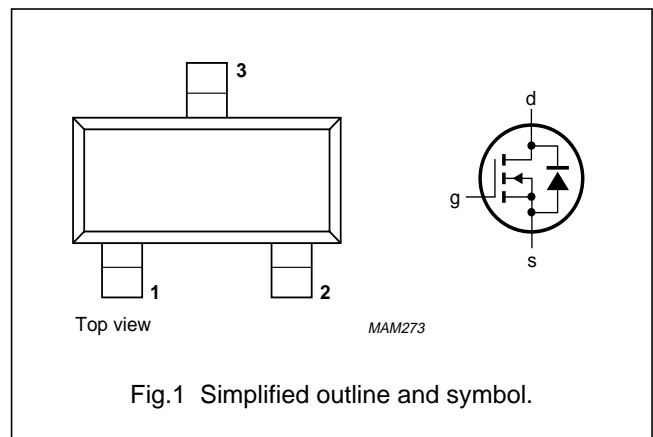
- Power management
- DC to DC converters
- Battery powered applications
- 'Glue-logic'; interface between logic blocks and/or periphery
- General purpose switch.

## DESCRIPTION

N-channel enhancement mode MOS transistor in a SOT23 SMD package.

## PINNING - SOT23

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	s	source
3	d	drain



## QUICK REFERENCE DATA

SYMBOL	PARAMETERS	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	30	V
$V_{SD}$	source-drain diode forward voltage	$V_{GD} = 0; I_S = 0.5 \text{ A}$	–	1	V
$V_{GS}$	gate-source voltage (DC)		–	$\pm 8$	V
$V_{GSth}$	gate-source threshold voltage	$V_{DS} = V_{GS}; I_D = 1 \text{ mA}$	0.4	–	V
$I_D$	drain current (DC)	$T_s = 80 \text{ }^\circ\text{C}$	–	0.85	A
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 2.5 \text{ V}; I_D = 0.5 \text{ A}$	–	0.5	$\Omega$
$P_{tot}$	total power dissipation	$T_s = 80 \text{ }^\circ\text{C}$	–	0.5	W

## CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

# N-channel enhancement mode MOS transistor

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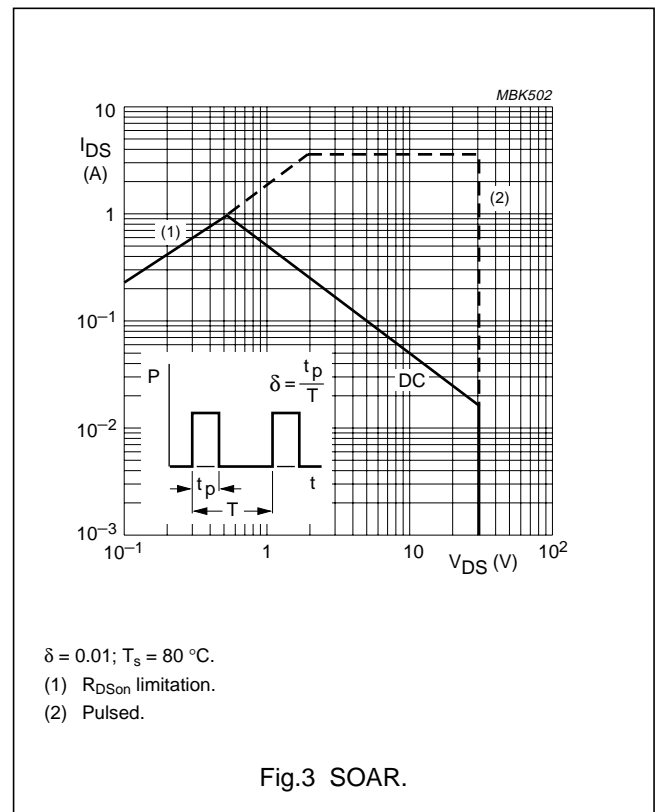
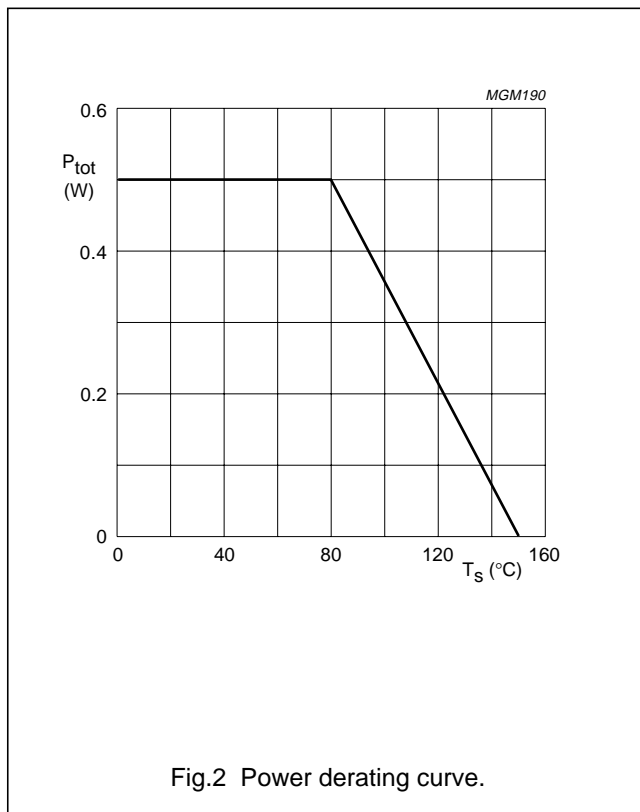
## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	30	V
$V_{GS}$	gate-source voltage (DC)		–	$\pm 8$	V
$I_D$	drain current (DC)	$T_s = 80\text{ }^\circ\text{C}$ ; note 1	–	0.85	A
$I_{DM}$	peak drain current	note 2	–	3.4	A
$P_{tot}$	total power dissipation	$T_s = 80\text{ }^\circ\text{C}$	–	0.5	W
		$T_{amb} = 25\text{ }^\circ\text{C}$ ; note 3	–	0.75	W
		$T_{amb} = 25\text{ }^\circ\text{C}$ ; note 4	–	0.54	W
$T_{stg}$	storage temperature		–55	+150	$^\circ\text{C}$
$T_j$	operating junction temperature		–55	+150	$^\circ\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current (DC)	$T_s = 80\text{ }^\circ\text{C}$	–	0.5	A
$I_{SM}$	peak pulsed source current	note 2	–	2	A

## Notes

- $T_s$  is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Device mounted on printed-circuit board with an  $R_{th\ a-tp}$  (ambient to tie-point) of 27.5 K/W.
- Device mounted on printed-circuit board with an  $R_{th\ a-tp}$  (ambient to tie-point) of 90 K/W.



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	140	K/W

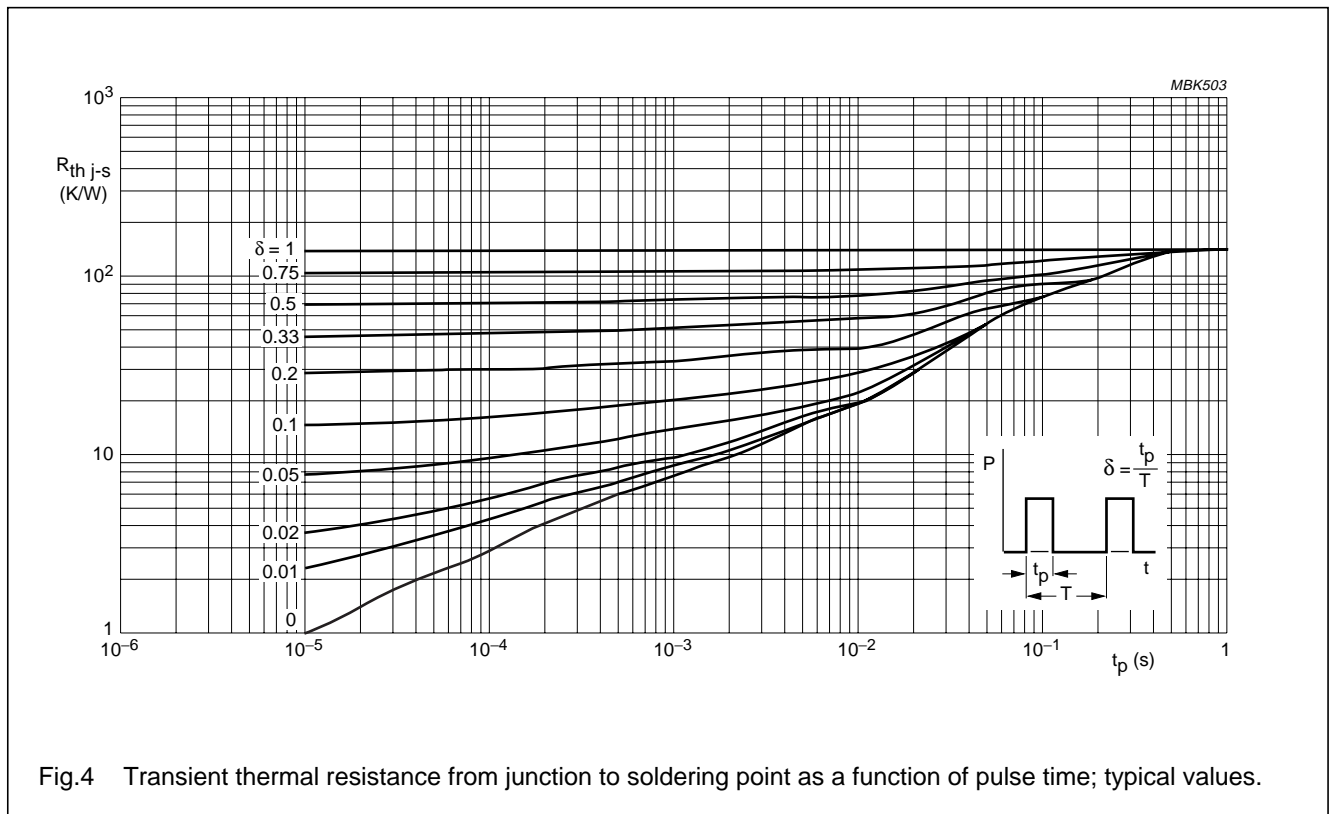


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

# N-channel enhancement mode MOS transistor

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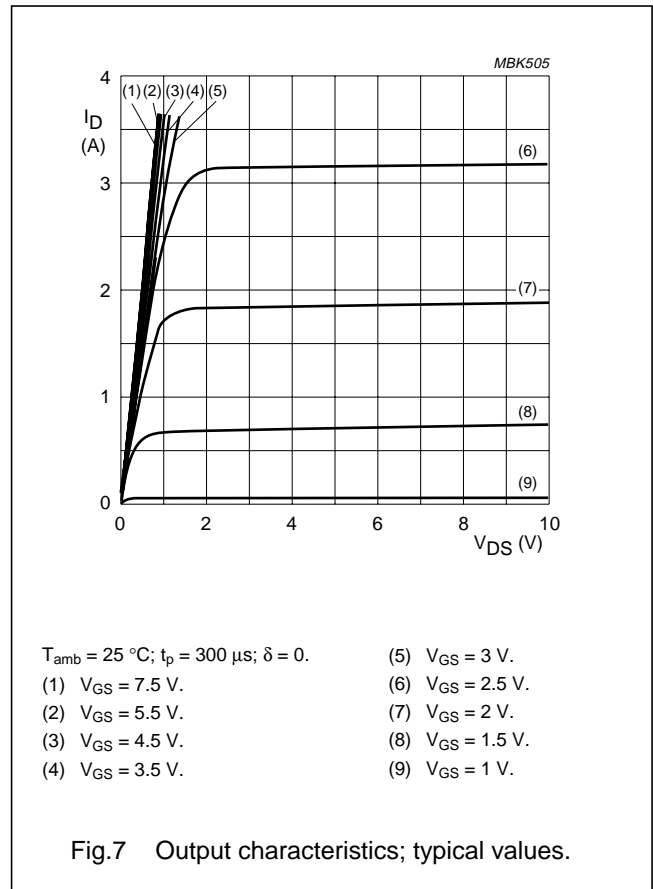
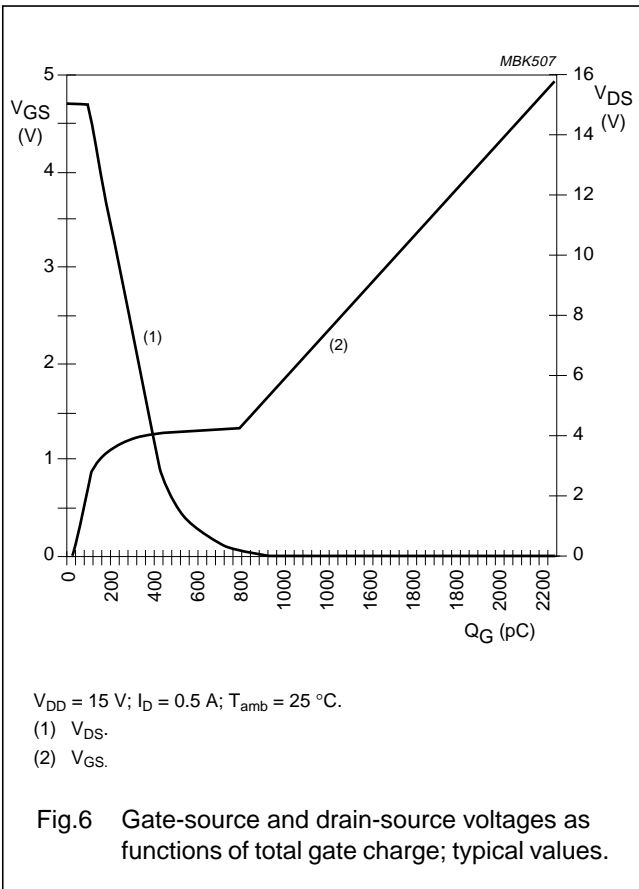
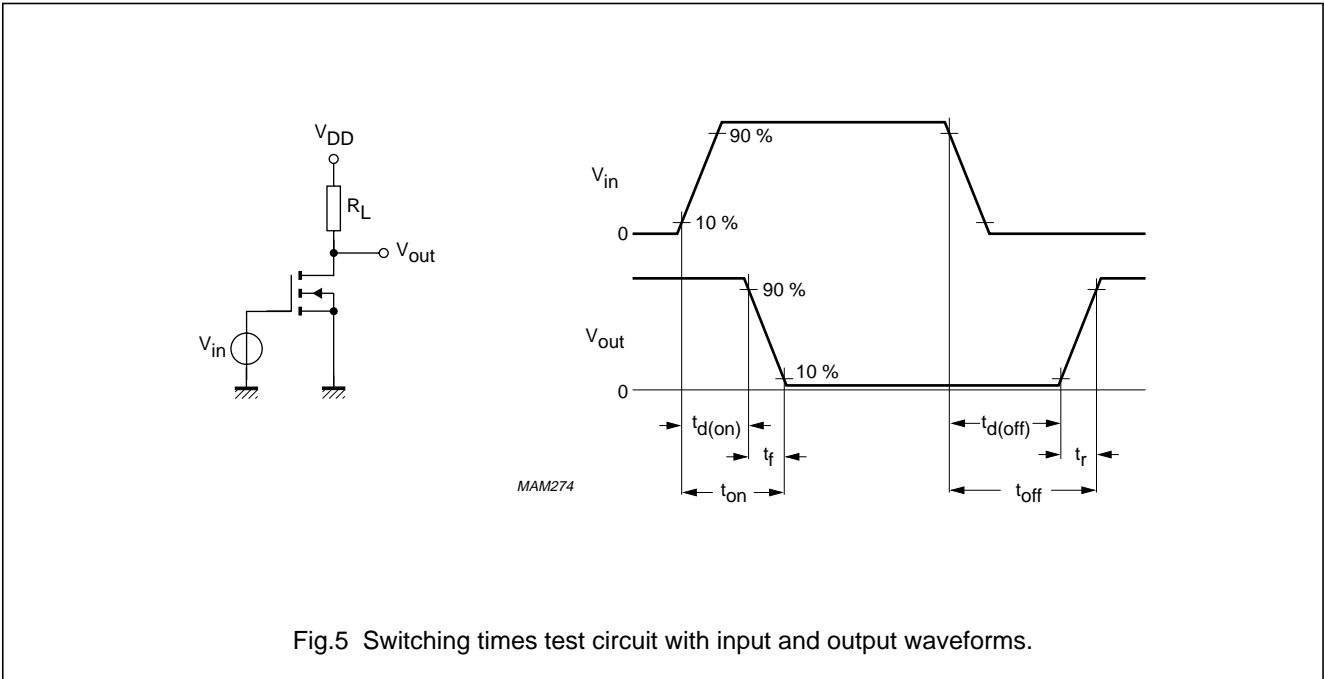
### CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = 10\ \mu\text{A}$	30	–	–	V
$V_{GSth}$	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = 1\ \text{mA}$	0.4	–	–	V
$I_{DSS}$	drain-source leakage current	$V_{GS} = 0; V_{DS} = 24\ \text{V}$	–	–	100	nA
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 8\ \text{V}; V_{DS} = 0$	–	–	$\pm 100$	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\ \text{V}; I_D = 0.5\ \text{A}$	–	–	0.4	$\Omega$
		$V_{GS} = 2.5\ \text{V}; I_D = 0.5\ \text{A}$	–	–	0.5	$\Omega$
		$V_{GS} = 1.8\ \text{V}; I_D = 0.25\ \text{A}$	–	–	0.6	$\Omega$
$C_{iss}$	input capacitance	$V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$	–	83	–	pF
$C_{oss}$	output capacitance	$V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$	–	27	–	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = 24\ \text{V}; f = 1\ \text{MHz}$	–	14	–	pF
$Q_G$	total gate charge	$V_{GS} = 4.5\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 0.5\ \text{A}; T_{amb} = 25\text{ °C}$	–	2100	–	pC
$Q_{GS}$	gate-source charge	$V_{DD} = 15\ \text{V}; I_D = 0.5\ \text{A}; T_{amb} = 25\text{ °C}$	–	95	–	pC
$Q_{GD}$	gate-drain charge	$V_{DD} = 15\ \text{V}; I_D = 0.5\ \text{A}; T_{amb} = 25\text{ °C}$	–	670	–	pC
<b>Switching times</b>						
$t_{d(on)}$	turn-on delay time	$V_{GS} = 0\ \text{to}\ 8\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 0.5\ \text{A}; R_{gen} = 6\ \Omega$	–	2.5	–	ns
$t_f$	fall time	$V_{GS} = 0\ \text{to}\ 8\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 0.5\ \text{A}; R_{gen} = 6\ \Omega$	–	3.5	–	ns
$t_{on}$	turn-on switching time	$V_{GS} = 0\ \text{to}\ 8\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 0.5\ \text{A}; R_{gen} = 6\ \Omega$	–	6	–	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = 8\ \text{to}\ 0\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 0.5\ \text{A}; R_{gen} = 6\ \Omega$	–	20	–	ns
$t_r$	rise time	$V_{GS} = 8\ \text{to}\ 0\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 0.5\ \text{A}; R_{gen} = 6\ \Omega$	–	7	–	ns
$t_{off}$	turn-off switching time	$V_{GS} = 8\ \text{to}\ 0\ \text{V}; V_{DD} = 15\ \text{V}; I_D = 0.5\ \text{A}; R_{gen} = 6\ \Omega$	–	27	–	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain diode forward voltage	$V_{GD} = 0; I_S = 0.5\ \text{A}$	–	–	1	V
$t_{rr}$	reverse recovery time	$I_S = 0.5\ \text{A}; di/dt = -100\ \text{A}/\mu\text{s}$	–	25	–	ns

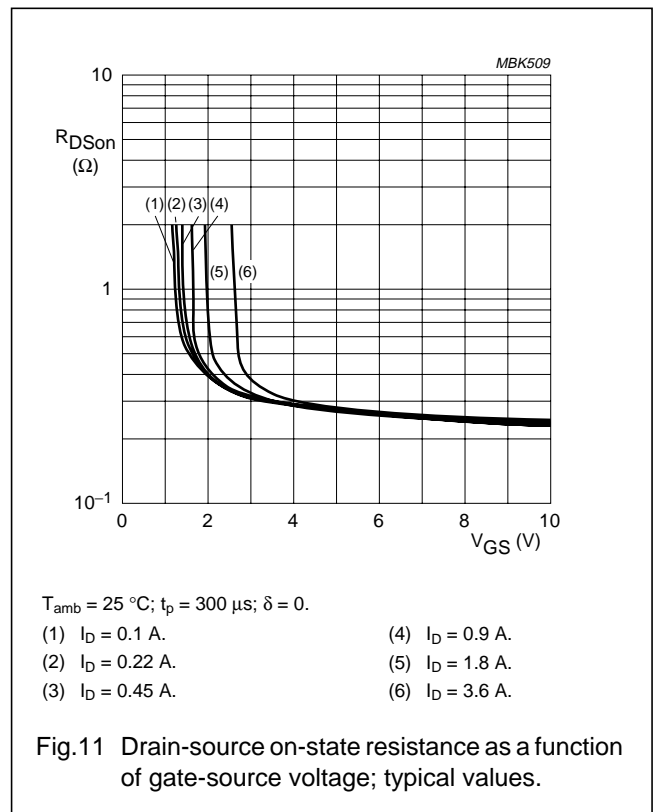
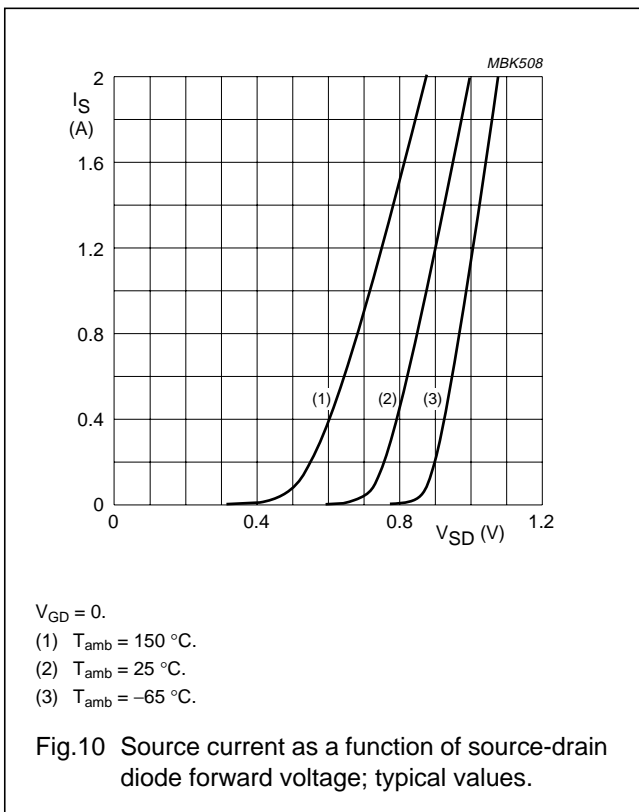
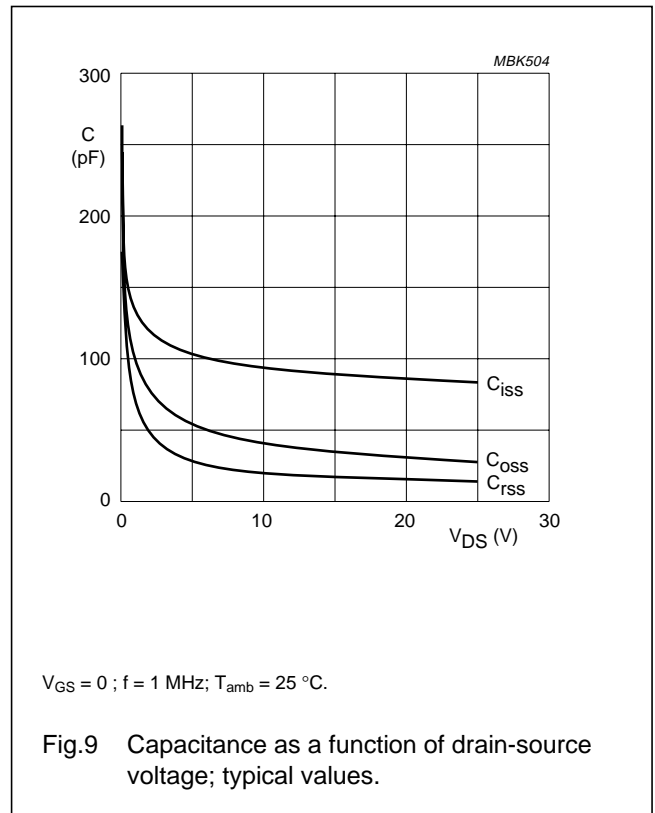
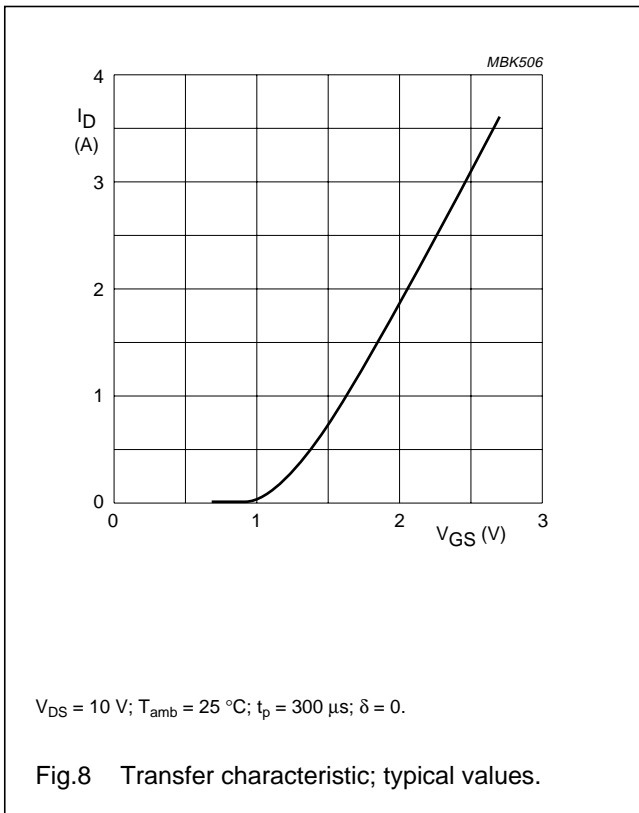
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MOS transistor

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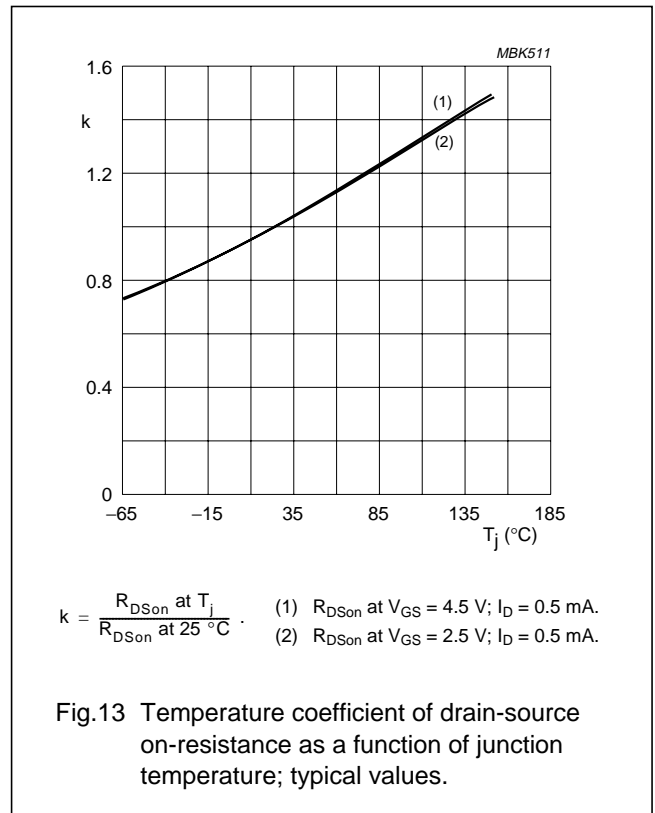
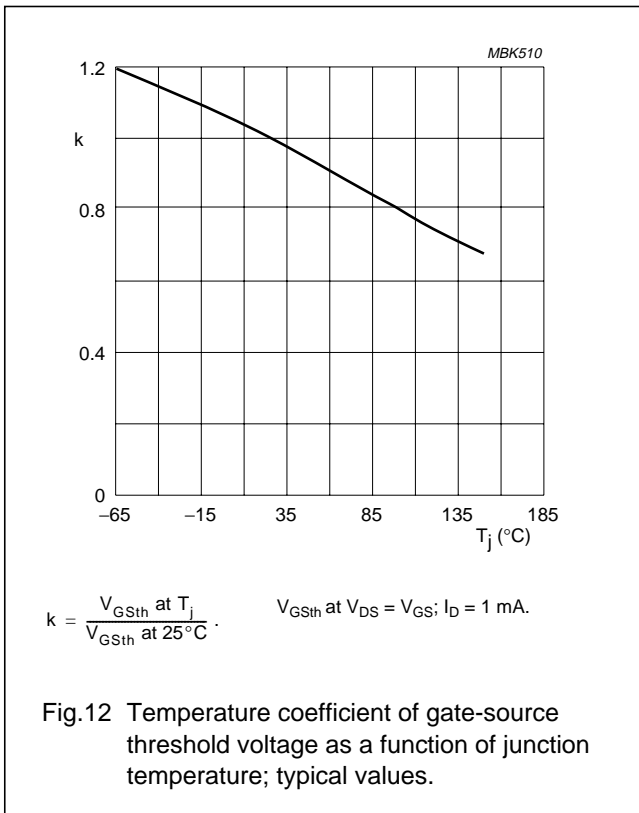
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N-channel enhancement mode  
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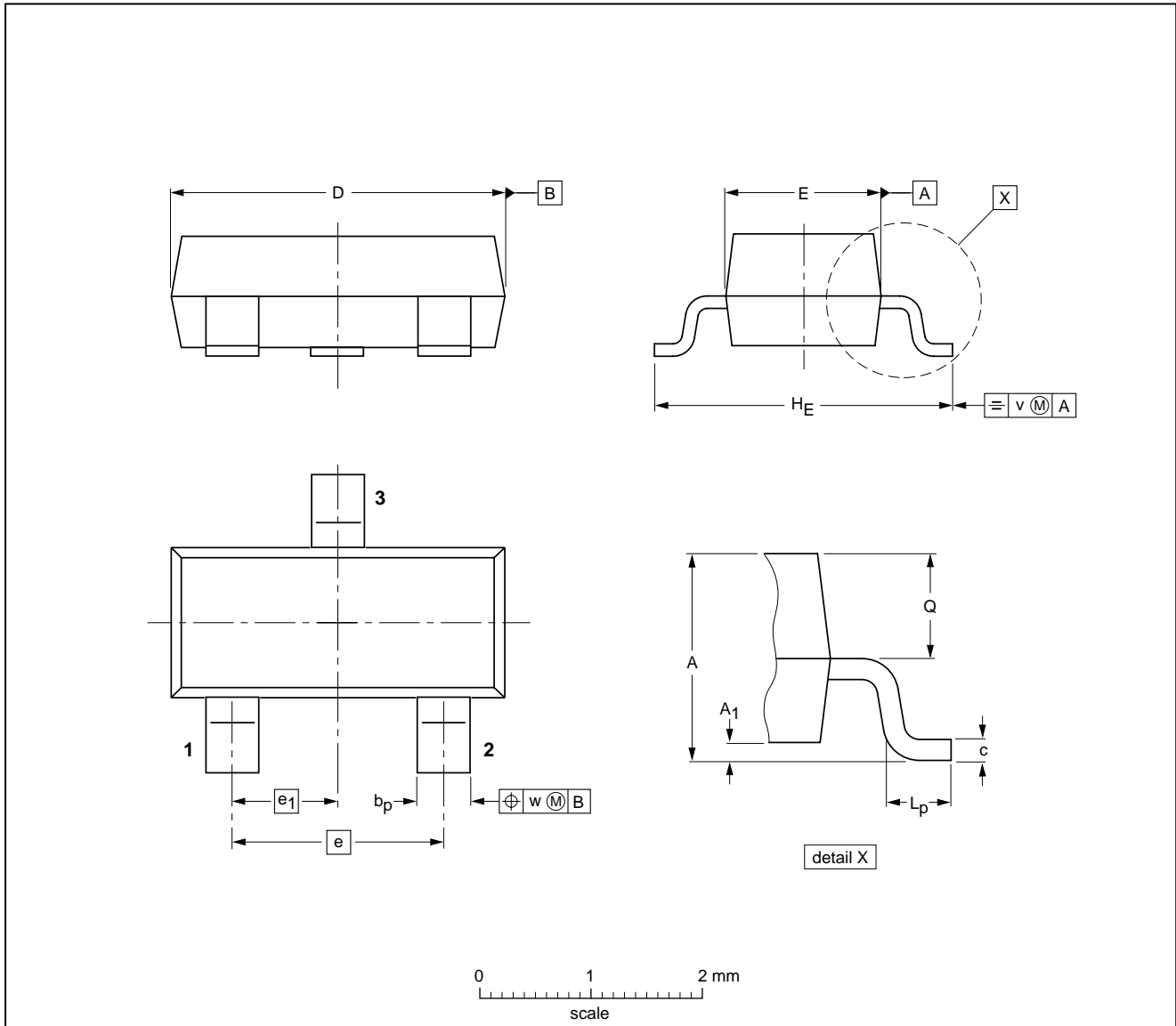
N-channel enhancement mode  
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PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max.	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

# N-channel enhancement mode MOS transistor

## BSH103

### DEFINITIONS

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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MOS transistor

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