ACT108-600D

AC Thyristor power switch

20 August 2014 **Product data sheet**

1. General description

AC Thyristor power switch in a SOT54 plastic package with self-protective capabilities against low and high energy transients

2. Features and benefits

- Exclusive negative gate triggering
- Full cycle AC conduction
- High noise immunity
- Remote gate separates the gate driver from the effects of the load current
- Very sensitive gate for lowest gate trigger current
- Safe clamping of low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients

3. Applications

- Fan motor circuits
- Pump motor circuits
- Lower-power highly inductive, resistive and safety loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	600	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 2; Fig. 3		-	-	8	A
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq$ 71 °C; Fig. 1		-	-	0.8	A
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; Fig. 4		-	-	2	kV
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 6		0.5	-	5	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 6		0.5	-	5	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; $T_j \leq$ 125 °C		650	-	-	V

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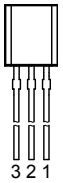
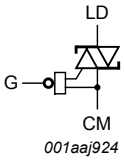
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 TO-92 (SOT54)	
2	G	gate		
3	LD	load		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACT108-600D	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54
ACT108-600D/DG	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

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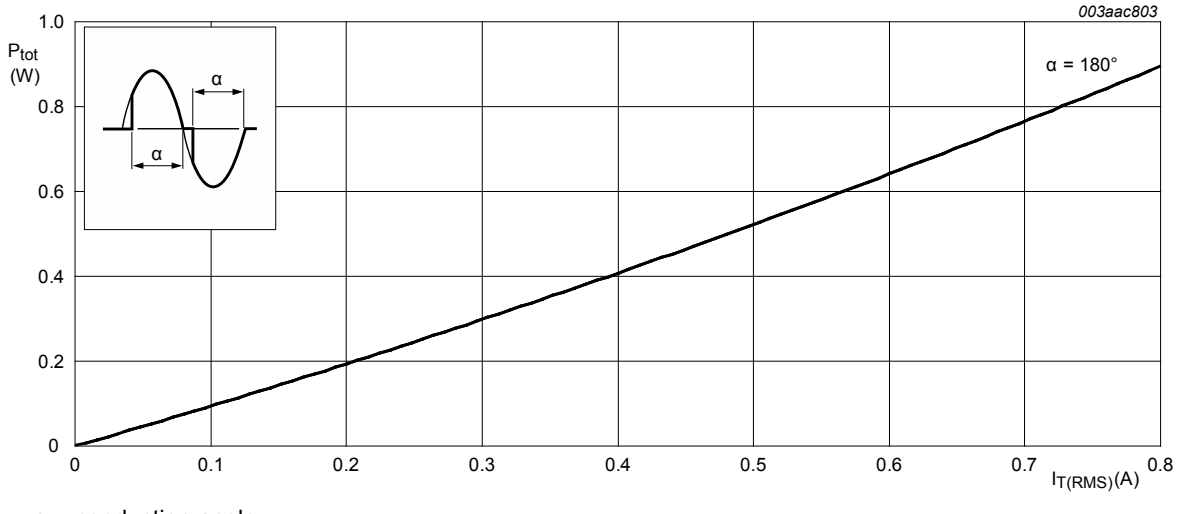
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 71$ °C; Fig. 1		-	0.8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	8.8	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 2; Fig. 3		-	8	A
I^2t	I2t for fusing	$t_p = 10$ ms; SIN		-	0.32	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 1$ A; $I_G = 10$ mA; $dI_G/dt = 0.2$ A/µs		-	50	A/µs
I_{GM}	peak gate current	t = 20 µs		-	1	A
V_{GM}	peak gate voltage			-	15	V
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C
V_{PP}	peak pulse voltage	$T_j = 25$ °C; non-repetitive, off-state; Fig. 4		-	2	kV



α = conduction angle

Fig. 1. Total power dissipation as a function of RMS on-state current; maximum values

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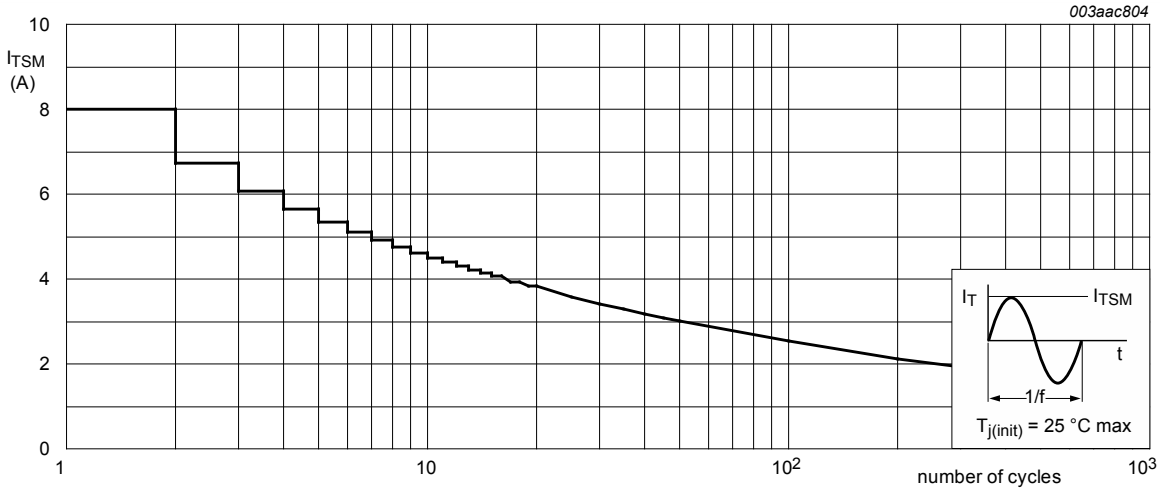
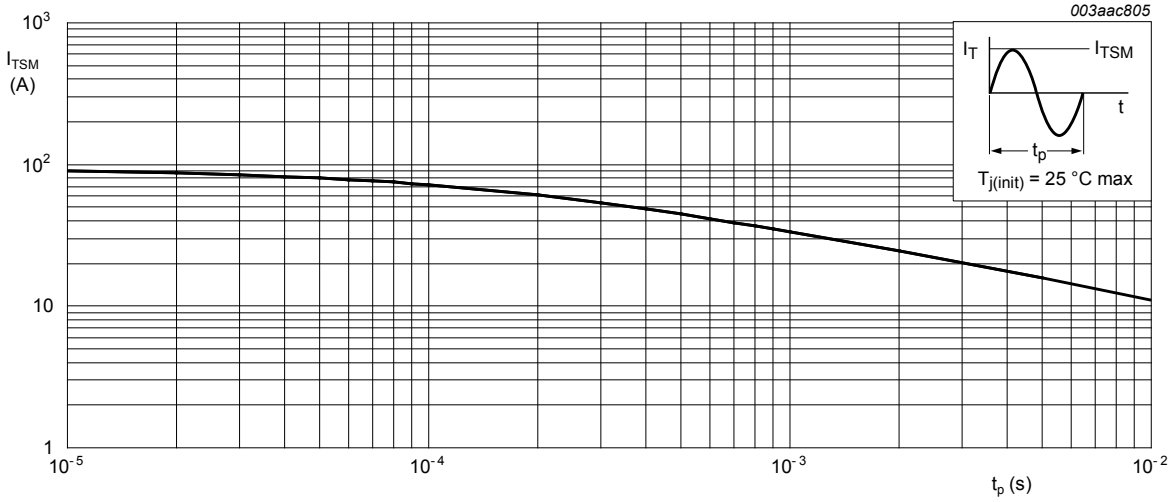


f = 50 Hz

Fig. 2. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

Fig. 3. Non-repetitive peak on-state current as a function of pulse width; maximum values

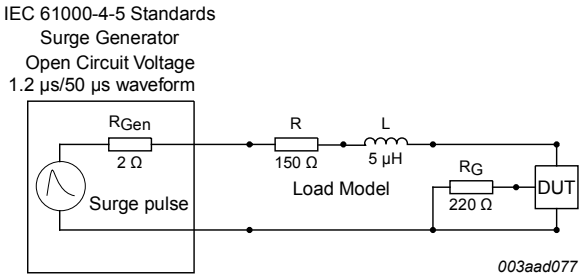


Fig. 4. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

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8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}lead)}$	thermal resistance from junction to lead	full cycle with heatsink compound; Fig. 5		-	-	60	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	full cycle; printed-circuit board mounted; lead length 4 mm		-	150	-	K/W

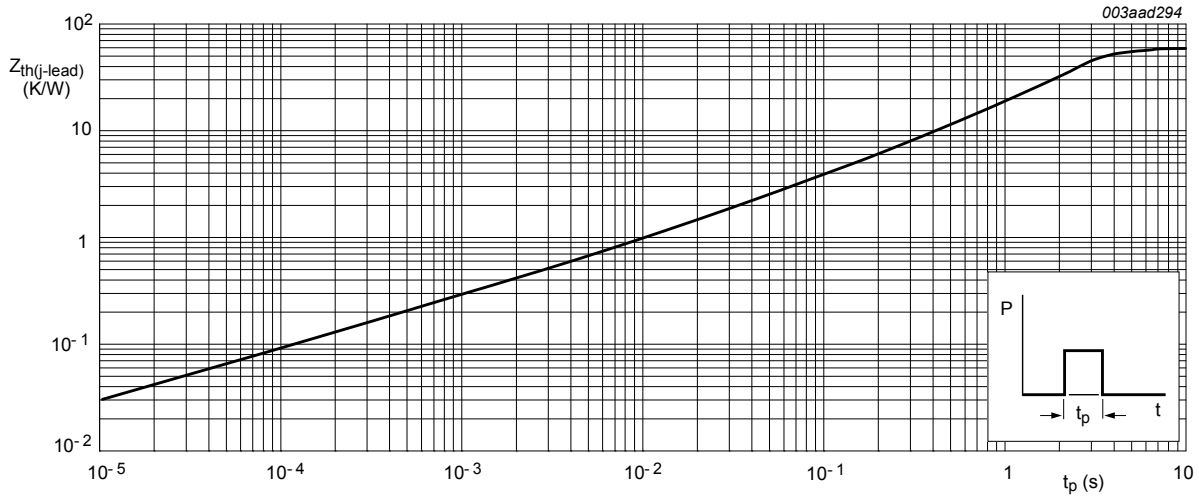

Fig. 5. Transient thermal impedance from junction to lead as a function of pulse width

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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 6		0.5	-	5	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 6		0.5	-	5	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; Fig. 7		-	-	25	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; Fig. 7		-	-	25	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 8		-	-	20	mA
V_T	on-state voltage	I_T = 1.1 A; T_j = 25 °C; Fig. 9		-	-	1.3	V
V_{GT}	gate trigger voltage	V_D = 400 V; I_T = 100 mA; T_j = 125 °C		0.15	-	-	V
		V_D = 12 V; I_T = 100 mA; T_j = 25 °C		-	-	0.9	V
I_D	off-state current	V_D = 600 V; T_j = 25 °C		-	-	2	µA
		V_D = 600 V; T_j = 125 °C		-	-	0.2	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j ≤ 125 °C		650	-	-	V
Dynamic charateristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 402 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 10		300	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ 1 A; dV_{com}/dt = 15 V/µs; gate open circuit; Fig. 11; Fig. 12		0.15	-	-	A/ms

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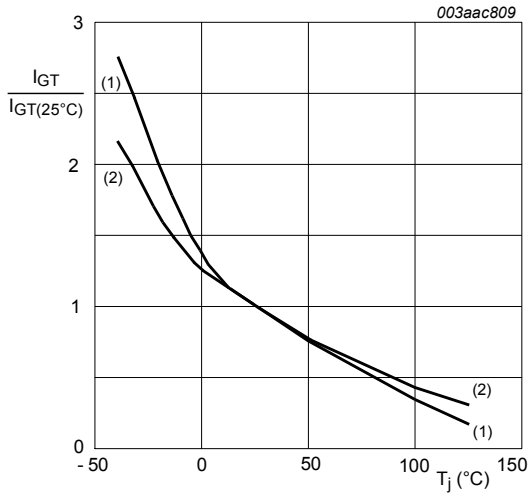


(1) LD+ G-
(2) LD- G-

Fig. 6. Normalized gate trigger current as a function of junction temperature

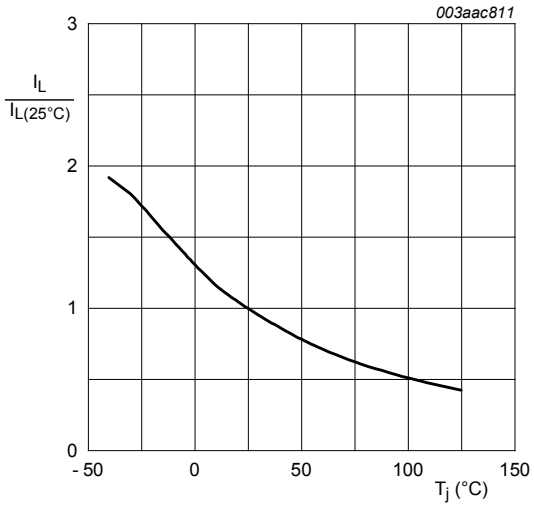


Fig. 7. Normalized latching current as a function of junction temperature

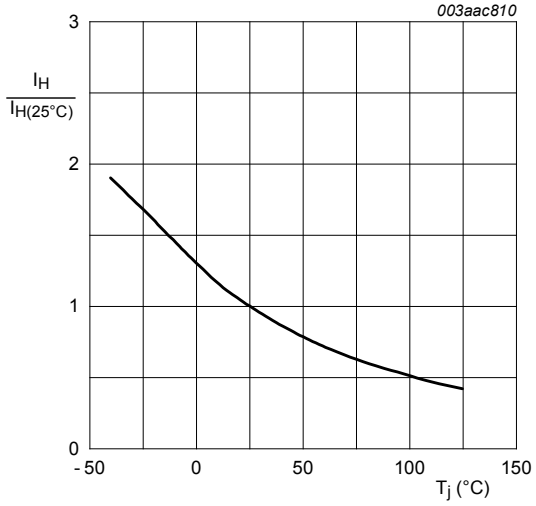
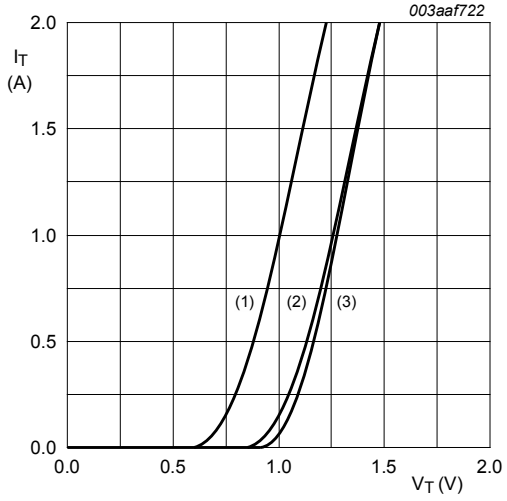


Fig. 8. Normalized holding current as a function of junction temperature



V_o = 0.758 V; R_s = 0.263 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 9. On-state current as a function of on-state voltage

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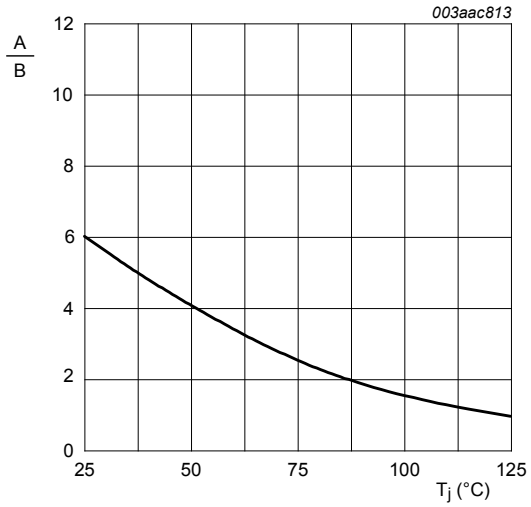
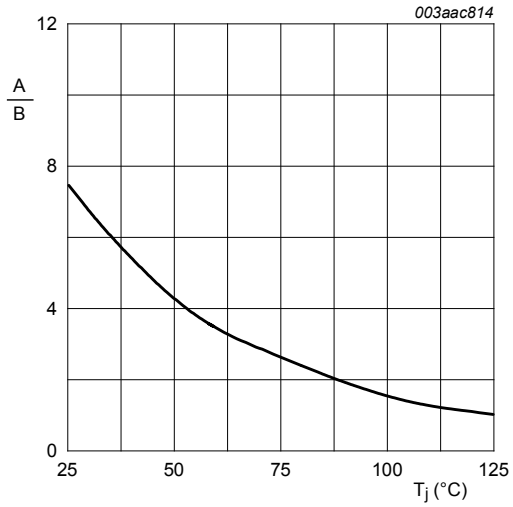


A = dV_D/dt at condition T_j °C

B = dV_D/dt at condition T_j [125] °C

Fig. 10. Normalized rate of rise of off-state voltage as a function of junction temperature

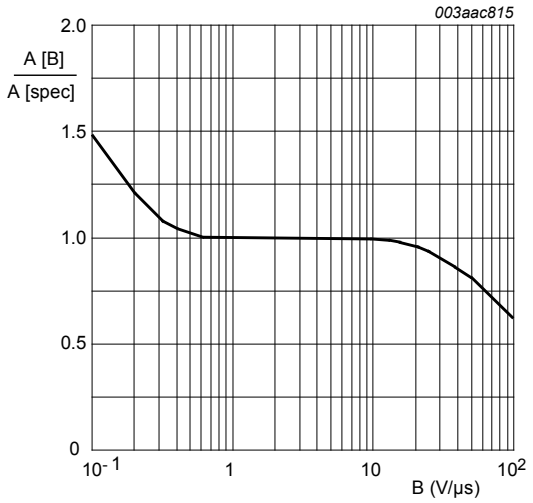


A = dI_{com}/dt at condition T_j °C

B = dI_{com}/dt at condition T_j [125] °C

V_D = 400 V

Fig. 11. Normalized critical rate of rise of commutating current as a function of junction temperature



A [B] = dI_{com}/dt at condition B, dV_{com}/dt

A [spec] is the data sheet value for dI_{com}/dt

turn-off time is less than 20 ms

Fig. 12. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

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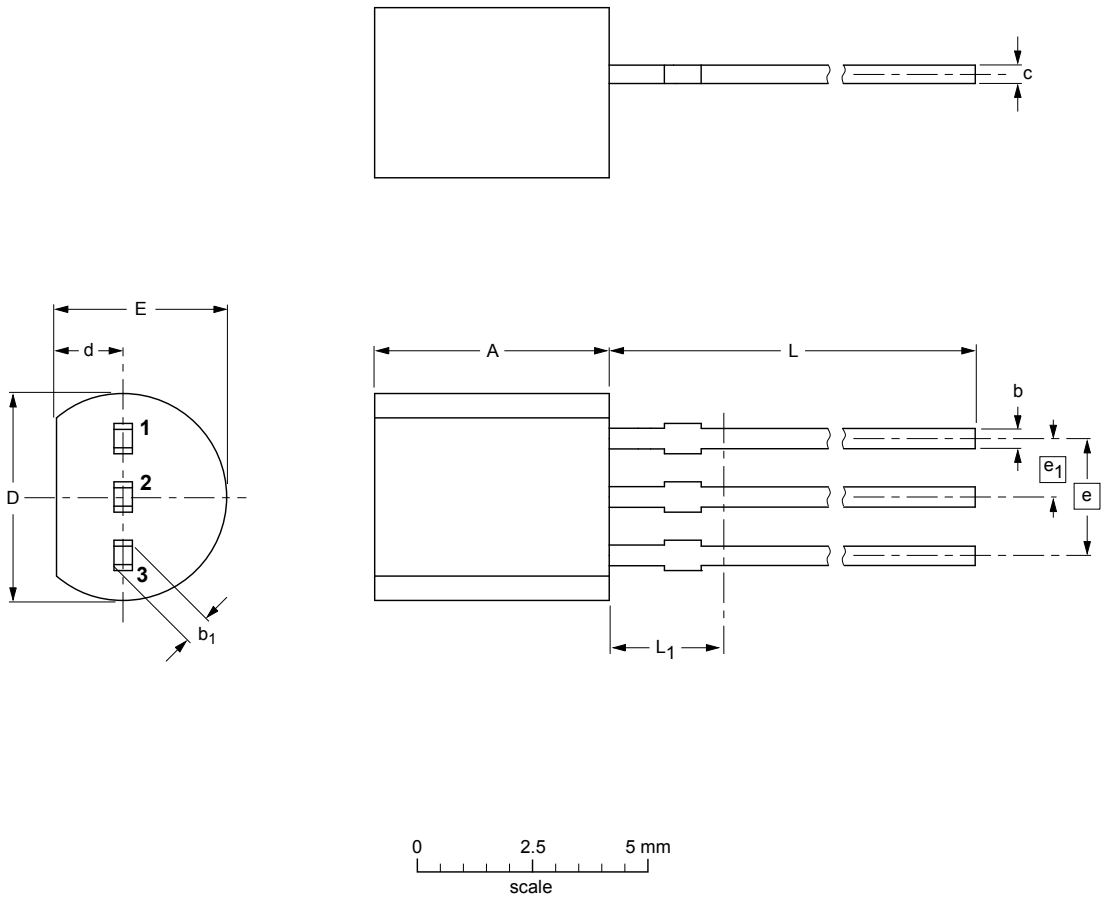
10. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1 (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig. 13. Package outline TO-92 (SOT54)

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