MAX15066/MAX15166 High-Efficiency, 4A, Step-Down DC-DC Regulators with Internal Power Switches

General Description

The MAX15066/MAX15166 current-mode, synchronous, DC-DC buck converters deliver an output current up to 4A with high efficiency. The devices operate from an input voltage of 4.5V to 16V and provides an adjustable output voltage from 0.606V to 90% of the input voltage. The devices are ideal for distributed power systems, notebook computers, nonportable consumer applications, and preregulation applications.

The devices feature a PWM mode operation with an internally fixed switching frequency of 500kHz (MAX15066) and 350kHz (MAX15166) capable of 90% maximum duty cycle. The devices automatically enter skip mode at light loads. The current-mode control architecture simplifies compensation design and ensures a cycle-by-cycle current limit and fast response to line and load transients. A high gain transconductance error amplifier allows flexibility in setting the external compensation, simplifying the design and allowing for an all-ceramic design.

The synchronous buck regulators feature internal MOSFETs that provide better efficiency than asynchronous solutions, while simplifying the design relative to discrete controller solutions. In addition to simplifying the design, the integrated MOSFETs minimize EMI, reduce board space, and provide higher reliability by minimizing the number of external components.

Additional features include an externally adjustable soft-start, independent enable input and power-good output for power sequencing, and thermal shutdown protection. The devices offer overcurrent protection (high-side sourcing) with hiccup mode during an output short-circuit condition. The devices ensure safe startup when powering into a prebiased output.

The MAX15066/MAX15166 are available in a 2mm x 2mm, 16-bump (4 x 4 array), 0.5mm pitch wafer-level package (WLP) and are fully specified from -40°C to +85°C.

Applications

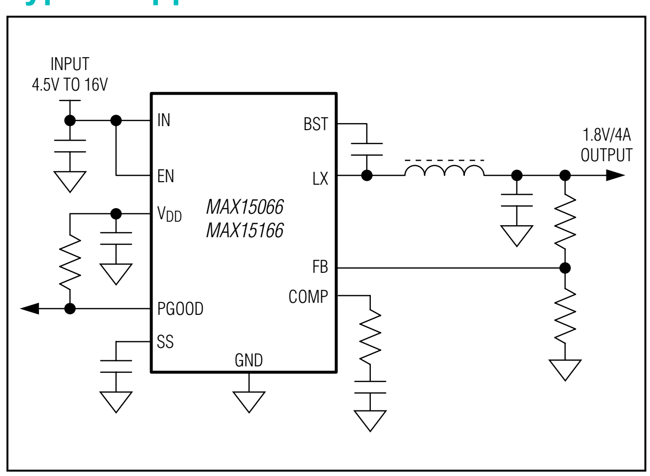
- Distributed Power Systems
- Preregulators for Linear Regulators
- Home Entertainment (TV and Set-Top Boxes)
- Network and Datacom
- Servers, Workstations, and Storage

Benefits and Features

- Feature Integration Shrinks Solution Size
  - Integrated 40mΩ (High-Side) and 18.5mΩ (Low-Side) R_{DS-ON} Power MOSFETs
  - Stable with Low-ESR Ceramic Output Capacitors
  - Enable Input and Power-Good Output
  - Cycle-by-Cycle Overcurrent Protection
  - Fully Protected Against Overcurrent (Hiccup Protection) and Overtemperature
- High Efficiency Conserves Power
  - Up to 96% Efficiency (5V Input and 3.3V Output)
  - Up to 93% Efficiency (12V Input and 3.3V Output)
  - Automatic Skip Mode During Light Loads
- Safe, Reliable, Accurate Operation
  - Continuous 4A Output Current
  - ±1% Output Accuracy Over Load, Line, and Temperature
  - Safe Startup Into Prebiased Output
  - Programmable Soft-Start
  - V_{DD} LDO Undervoltage Lockout
- Well Suited to Distributed Power, Networking, and Computing Applications
  - 4.5V to 16V Input Voltage Range
  - Adjustable Output Voltage Range from 0.606V to (0.9 x V_{IN})
- Available in EE-Sim® Design and Simulation Tool to Slash Design Time

Ordering Information ***appears at end of data sheet.***

Typical Application Circuit



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19-5224; Rev 5; 1/15

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Absolute Maximum Ratings

IN to GND .... -0.3V to +18V
EN to GND .... -0.3V to (V_{IN} + 0.3V)
LX to GND .... -0.3V to the lower of +18V and (V_{IN} + 0.3V)
LX to GND (for 50ns) .... -1V to the lower of +18V and (V_{IN} + 0.3V)
PGOOD to GND .... -0.3V to +6V
V_{DD} to GND .... -0.3V to the lower of +6V and (V_{IN} + 0.3V)
COMP, FB, SS to GND .... -0.3V to the lower of +6V and (V_{DD} + 0.3V)
BST to LX .... -0.3V to +6V
BST to GND .... -0.3V to +24V
BST to V_{DD} .... -0.3V to +18V
LX RMS Current (Note 1) .... 0 to 9A

Converter Output and V_{DD} Short-Circuit Duration .... Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Bump WLP (derate 20.4mW/°C above +70°C) Multilayer Board 1500mW
Thermal Resistance (θ_{JA}) (Note 2) .... 23.6°C/W
Operating Temperature Range .... -40°C to +85°C
Junction Temperature (Note 3) .... +150°C
Continuous Operating Temperature at Full Current (Note 3) .... +105°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (reflow) .... +260°C

Note 1: LX has internal clamp diodes to GND and IN. Applications that forward bias these diodes should take care not to exceed the device's package power dissipation.
Note 2: Package thermal resistances were obtained based on the MAX15066/MAX15166 evaluation kit.
Note 3: Continuous operation at full current beyond +105°C can degrade product life.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{IN} = 12V, C_{VDD} = 1µF, C_{IN} = 22µF, T_A = T_J = -40°C to +85°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-DOWN CONVERTER						
Input Voltage Range	V_{IN}		4.5		16	V
Quiescent Current	I_{IN}	Not switching		1.1	2	mA
Shutdown Input Supply Current		V_{EN} = 0V		2	6	µA
ENABLE INPUT						
EN Shutdown Threshold Voltage	V_{EN_SHDN}	V_{EN} rising		0.7		V
EN Shutdown Voltage Hysteresis	V_{EN_HYST}			70		mV
EN Lockout Threshold Voltage	V_{EN_LOCK}	V_{EN} rising	1.7	1.9	2.1	V
EN Lockout Threshold Hysteresis	$V_{EN\_LOCK\_HYST}$			200		mV
EN Input Current	I_{EN}	V_{EN} = 12V	0.8	2.6	5	µA
POWER-GOOD OUTPUT						
PGOOD Threshold	V_{PGOOD_TH}	V_{FB} rising	0.54	0.56	0.585	V
PGOOD Threshold Hysteresis	V_{PGOOD_HYST}			15		mV
PGOOD Output Low Voltage	V_{PGOOD_OL}	I_{PGOOD} = 5mA, V_{FB} = 0.5V		35	100	mV
PGOOD Leakage Current	I_{PGOOD}	V_{PGOOD} = 5V, V_{FB} = 0.7V			100	nA
ERROR AMPLIFIER						
Error-Amplifier Transconductance	g_{MV}			1.6		mS

Electrical Characteristics (continued)

(V_{IN} = 12V, C_{VDD} = 1µF, C_{IN} = 22µF, T_A = T_J = -40°C to +85°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Error-Amplifier Voltage Gain	A_{VEA}			90		dB
FB Set-Point Accuracy	V_{FB}		600	606	612	mV
FB Input Bias Current	I_{FB}	V_{FB} = 0.5V or 0.7V	-100		+100	nA
SOFT-START						
SS Current	I_{SS}	V_{SS} = 0.45V, sourcing	4.5	5	5.5	µA
SS Discharge Resistance	R_{SS}	I_{SS} = 10mA, sinking		6		Ω
CURRENT SENSE						
Current Sense to COMP Transconductance	g_{MC}			9		S
COMP Clamp Low		V_{FB} = 0.7V		0.68		V
PWM CLOCK						
Switching Frequency	f_{SW}	MAX15066	450	500	550	kHz
		MAX15166	315	350	385	
Maximum Duty Cycle	D_{MAX}			90		%
Minimum Controllable On-Time				150		ns
Slope Compensation Ramp Valley				840		mV
Slope Compensation Ramp Amplitude	V_{SLOPE}	Extrapolated to 100% duty cycle		667		mV
INTERNAL LDO OUTPUT (V_{DD})						
V_{DD} Output Voltage	V_{DD}	I_{VDD} = 1mA, V_{IN} = 6.5V to 16V	4.75	5.1	5.45	V
		I_{VDD} = 1mA to 25mA, V_{IN} = 6.5V	4.75	5.1	5.45	
V_{DD} Short-Circuit Current		V_{IN} = 6.5V	30	90		mA
V_{DD} LDO Dropout Voltage		I_{VDD} = 5mA, V_{DD} drops by 2%			100	mV
V_{DD} Undervoltage Lockout Threshold	V_{UVLO_TH}	V_{DD} rising, LX starts switching	3.7	3.9	4.1	V
V_{DD} Undervoltage Lockout Hysteresis	V_{UVLO_HYST}			150		mV
POWER SWITCH						
LX On-Resistance		High-side switch, I_{LX} = 0.4A		40		mΩ
		Low-side switch, I_{LX} = 0.4A		18.5		
High-Side Switch Source Current-Limit Threshold	I_{HSCL}		5.5	7.7		A
Low-Side Switch Zero-Crossing Current-Limit Threshold				0.21		A
High-Side Switch Skip Sourcing Current-Limit Threshold				0.58		A
LX Leakage Current		V_{BST} = 21V, V_{IN} = V_{LX} = 16V		0.01		µA
		V_{BST} = 5V, V_{IN} = 16V, V_{LX} = 0V		0.01		
BST Leakage Current		V_{BST} = 21V, V_{IN} = V_{LX} = 16V		0.01		µA
BST On-Resistance		I_{BST} = 5mA		10		Ω

Electrical Characteristics (continued)

(V_{IN} = 12V, C_{VDD} = 1µF, C_{IN} = 22µF, T_A = T_J = -40°C to +85°C, typical values are at T_A = T_J = +25°C, unless otherwise noted.) (Note 4)

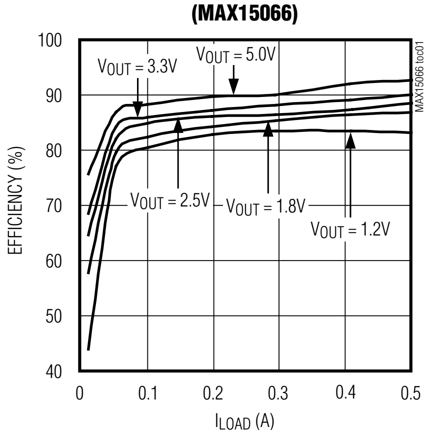
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HICCUP PROTECTION						
Blanking Time				21 x Soft-Start Time		
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Rising		160		°C
Thermal Shutdown Hysteresis				20		°C

Note 4: Specifications are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.

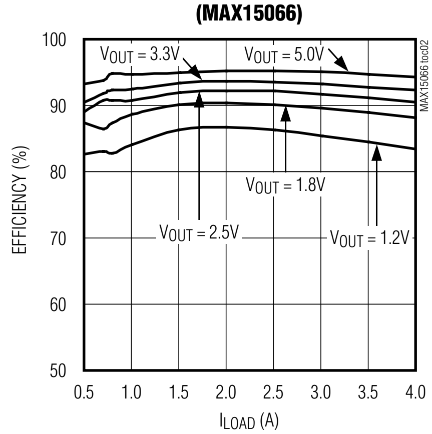
Typical Operating Characteristics

(V_{IN} = 12V, V_{OUT} = 1.8V, C_{VDD} = 1µF, C_{IN} = 22µF, C_{OUT} = 47µF, T_A = +25°C (Figure 1, MAX15066), unless otherwise noted.)

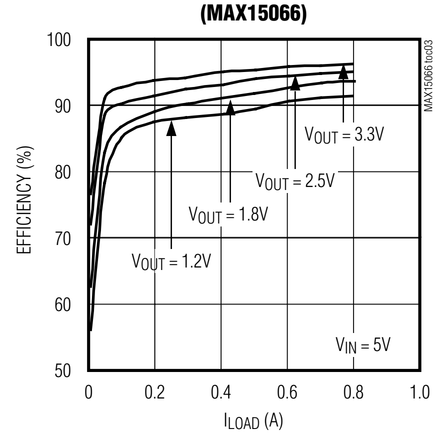
EFFICIENCY vs. LOAD CURRENT (MAX15066)



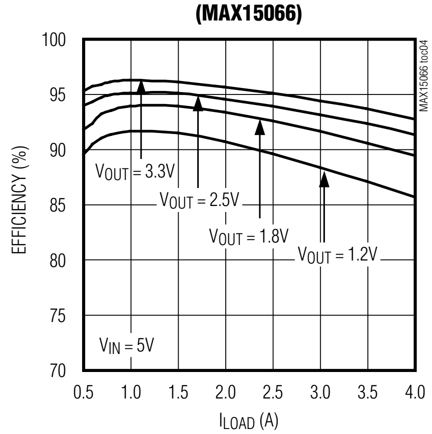
EFFICIENCY vs. LOAD CURRENT (MAX15066)



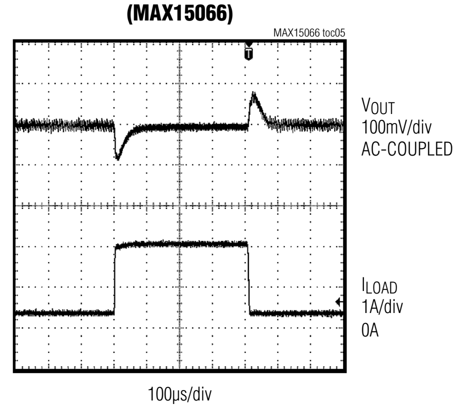
EFFICIENCY vs. LOAD CURRENT (MAX15066)



EFFICIENCY vs. LOAD CURRENT (MAX15066)

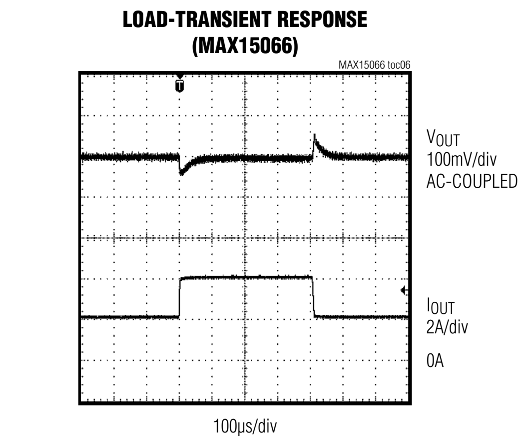


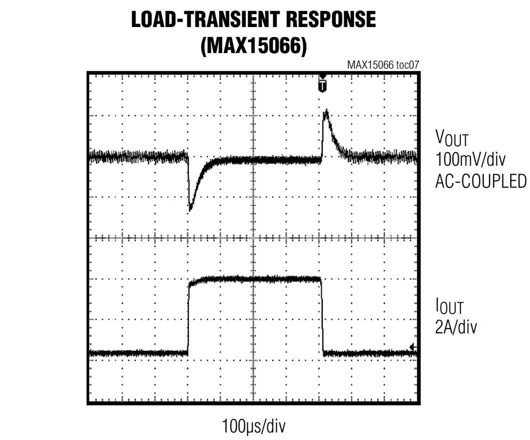
LOAD-TRANSIENT RESPONSE (MAX15066)

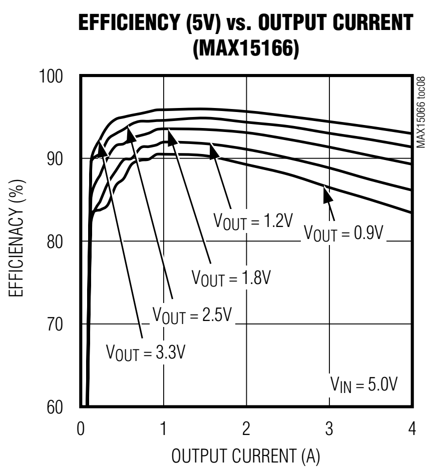


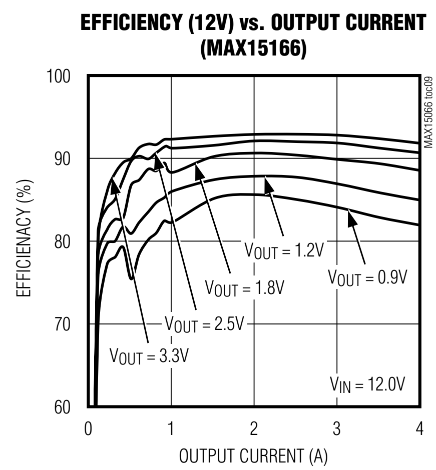
Typical Operating Characteristics (continued)

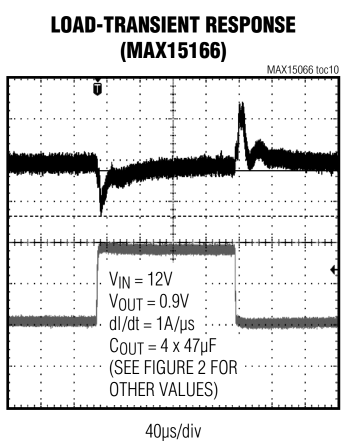
(V_{IN} = 12V, V_{OUT} = 1.8V, C_{VDD} = 1µF, C_{IN} = 22µF, C_{OUT} = 47µF, T_A = +25°C (Figure 1, MAX15066), unless otherwise noted.)

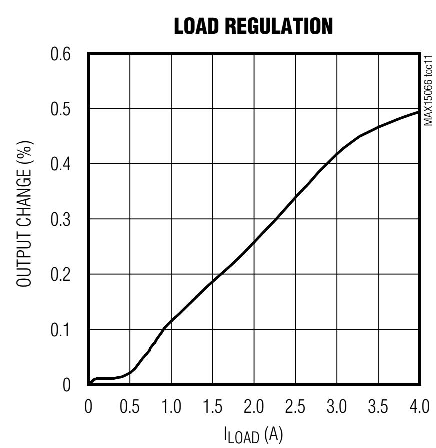






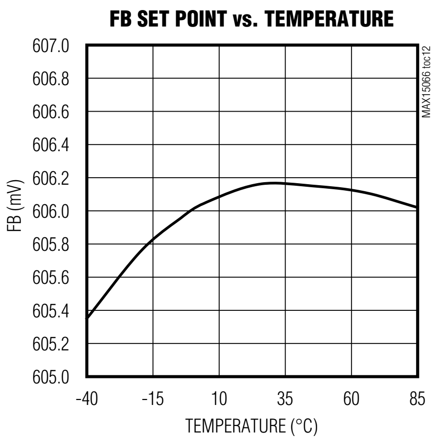


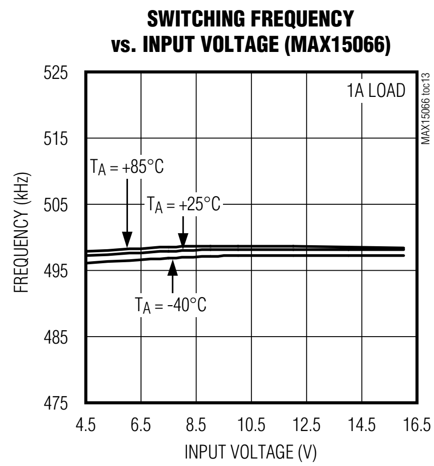


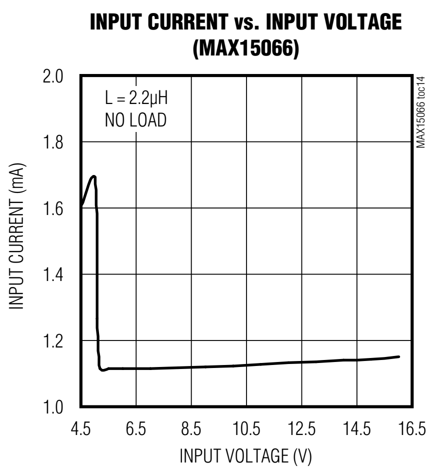


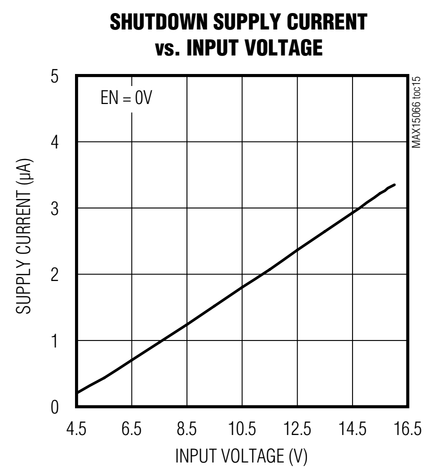
Typical Operating Characteristics (continued)

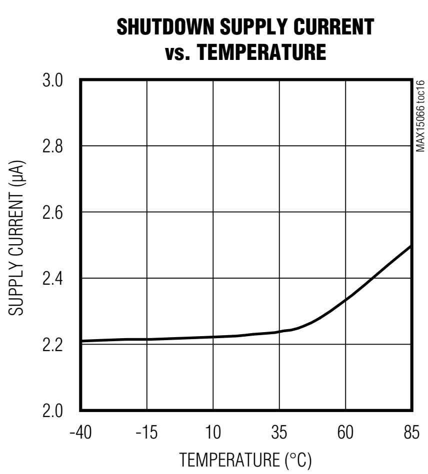
(V_{IN} = 12V, V_{OUT} = 1.8V, C_{VDD} = 1µF, C_{IN} = 22µF, C_{OUT} = 47µF, T_A = +25°C (Figure 1, MAX15066), unless otherwise noted.)

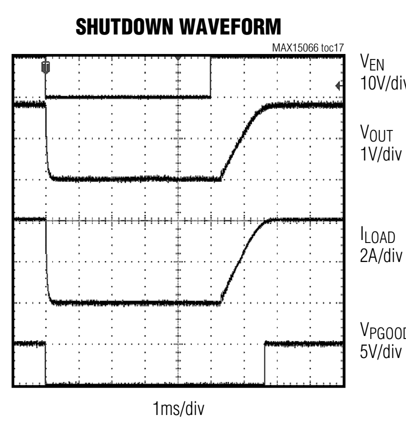








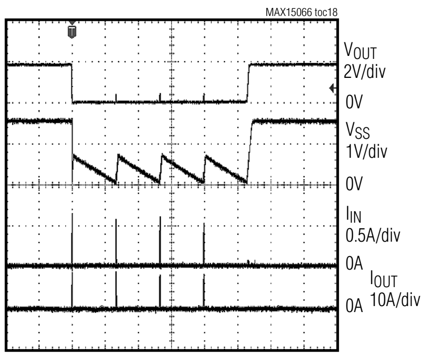




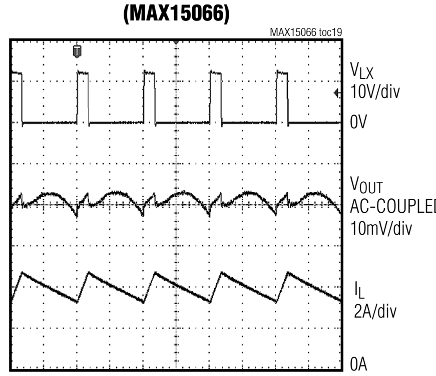
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 1.8V, C_{VDD} = 1µF, C_{IN} = 22µF, C_{OUT} = 47µF, T_A = +25°C (Figure 1, MAX15066), unless otherwise noted.)

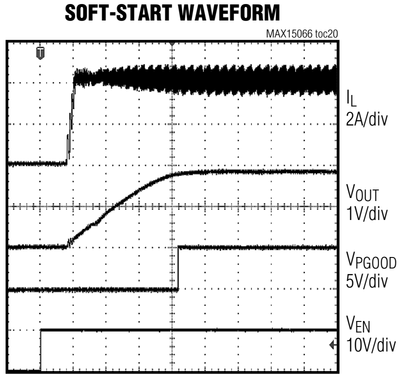
OUTPUT SHORT-CIRCUIT WAVEFORM



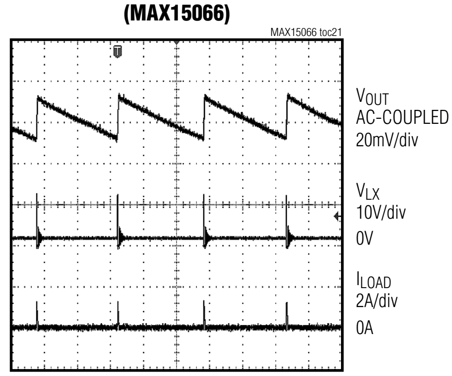
SWITCHING BEHAVIOR
(MAX15066)



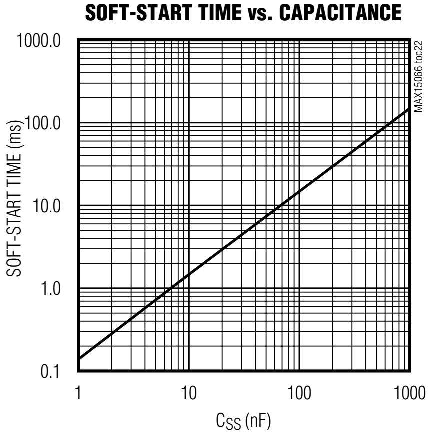
SOFT-START WAVEFORM



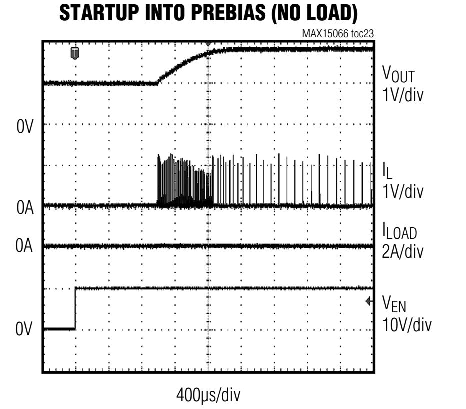
SKIP MODE WAVEFORM
(MAX15066)



SOFT-START TIME vs. CAPACITANCE



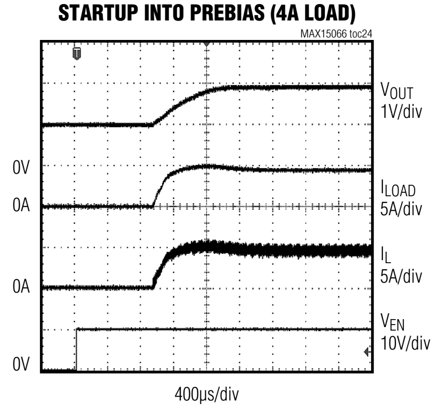
STARTUP INTO PREBIAS (NO LOAD)



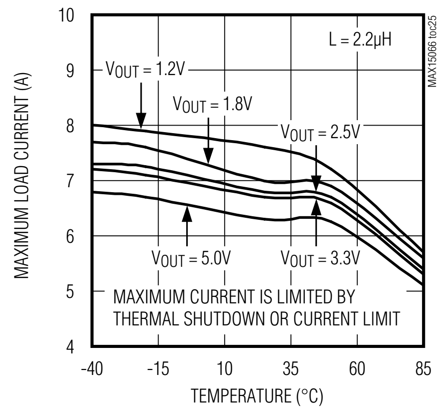
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 1.8V, C_{VDD} = 1µF, C_{IN} = 22µF, C_{OUT} = 47µF, T_A = +25°C (Figure 1, MAX15066), unless otherwise noted.)

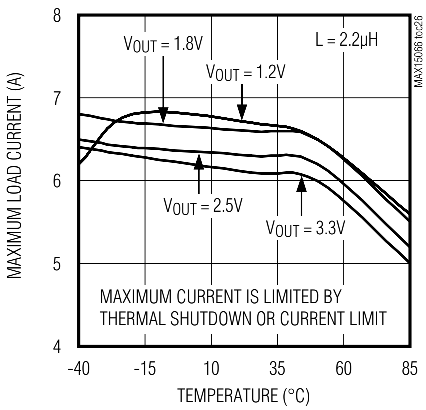
STARTUP INTO PREBIAS (4A LOAD)



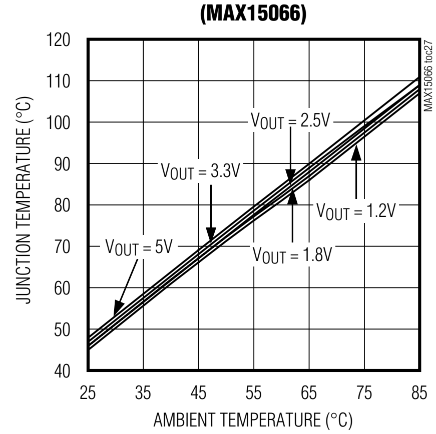
MAXIMUM LOAD CURRENT vs. TEMPERATURE (V_{IN} = 12V) (MAX15066)



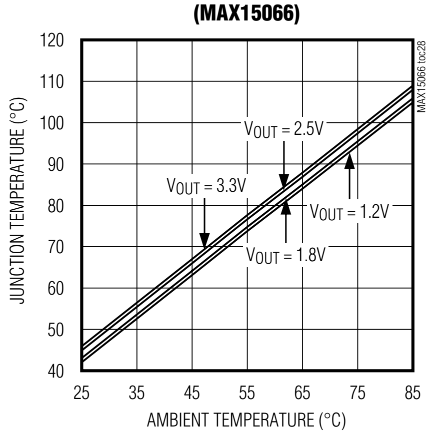
MAXIMUM LOAD CURRENT vs. TEMPERATURE (V_{IN} = 5V) (MAX15066)



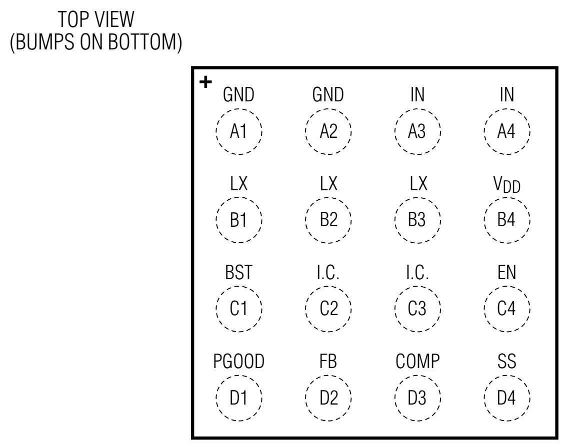
JUNCTION TEMPERATURE vs. AMBIENT TEMPERATURE (V_{IN} = 12V, L = 2.2µH, LOAD CURRENT = 4A) (MAX15066)



JUNCTION TEMPERATURE vs. AMBIENT TEMPERATURE (V_{IN} = 5V, L = 2.2µH, LOAD CURRENT = 4A) (MAX15066)



Pin Configuration

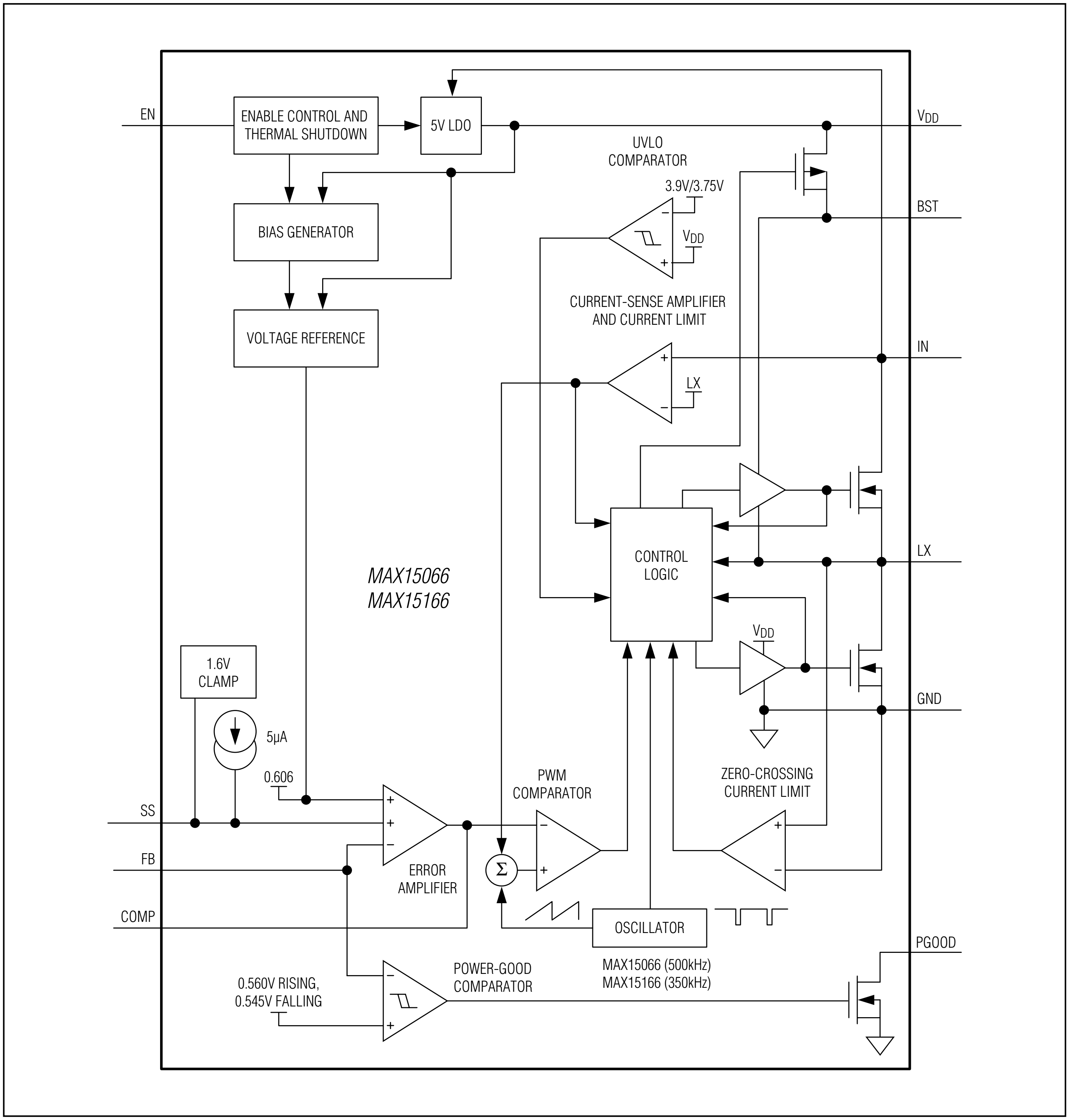


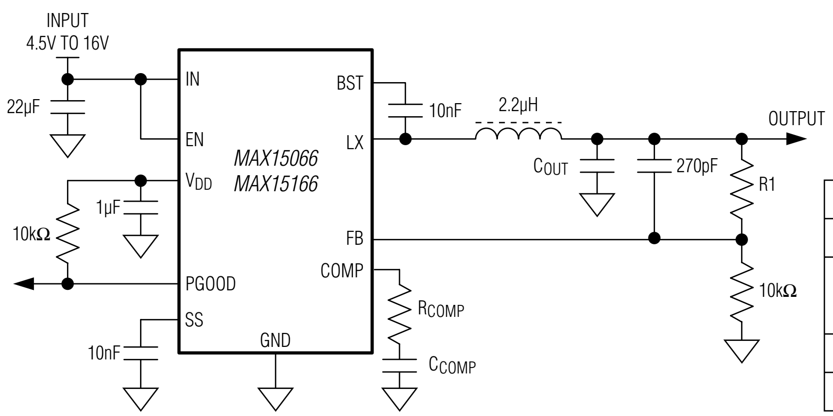
WLP

Pin Description

BUMP	NAME	FUNCTION
A1, A2	GND	Ground. Connect A1 and A2 together as close as possible to the device.
A3, A4	IN	Power-Supply Input. Input supply range is from 4.5V to 16V. Connect A3 and A4 together as close as possible to the device. Bypass IN to GND with a minimum 22µF ceramic capacitor as close as possible to the device.
B1–B3	LX	Inductor Connection. Connect an inductor between LX and the regulator output. LX is high impedance when the device is in shutdown mode. Connect all LX nodes together as close as possible to the device.
B4	V_{DD}	Internal 5V LDO Output. V_{DD} powers the internal analog core. Connect a minimum of 1µF ceramic capacitor from V_{DD} to GND.
C1	BST	High-Side MOSFET Driver Supply. Bypass BST to LX with a 0.01µF capacitor. BST is internally connected to the V_{DD} regulator through a pMOS switch.
C2, C3	I.C.	Internal Connection. Leave unconnected.
C4	EN	Enable Input. Connect EN to GND to disable the device. Set EN to above 1.9V (typ) to enable the device. EN can be shorted to IN for always-on operation.
D1	PGOOD	Power-Good Output. PGOOD is an open-drain output that goes high impedance when V_{FB} exceeds 0.56V (typ). PGOOD is internally pulled low when V_{FB} falls below 0.545V (typ). PGOOD is internally pulled low when the device is in shutdown mode, V_{DD} is below the UVLO threshold, or the device is in thermal shutdown.
D2	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to GND to set the output voltage from 0.606V to 90% of V_{IN}.
D3	COMP	Voltage-Error Amplifier Output. Connect the necessary compensation network from COMP to GND (see the *Compensation Design* section).
D4	SS	Soft-Start Timing Capacitor Connection. Connect a capacitor from SS to GND to set the startup time (see the *Setting the Soft-Start Time* section).

Block Diagram





COMPONENT	MAX15066	MAX15166
C_{OUT}	1 x 47µF	4 x 47µF
R_{COMP}	7.5kΩ	7.5kΩ
C_{COMP}	2700pF	2700pF
R1	20kΩ	5.1kΩ
V_{OUT}	1.8V	0.9V

Figure 1. Reference Circuit

Detailed Description

The MAX15066/MAX15166 are high-efficiency, peak current-mode, step-down DC-DC converters with integrated high-side (40mΩ) and low-side (18.5mΩ) power switches. The output voltage is set from 0.606V to 0.9 x V_{IN} by using an external resistive divider and can deliver up to 4A of load current. The input voltage range is 4.5V to 16V, making these devices ideal for distributed power systems, notebook computers, nonportable consumer applications, and preregulation applications.

The devices feature a PWM, internally fixed switching frequency of 500kHz (MAX15066) and 350kHz (MAX15166) with a 90% maximum duty cycle. PWM current-mode control allows for an all-ceramic capacitor solution. The devices include a high gain transconductance error amplifier. The current-mode control architecture simplifies compensation design, and ensures a cycle-by-cycle current limit and fast reaction to line and load transients. The low R_{DS-ON}, internal MOSFET switches ensure high efficiency at heavy loads and minimize critical inductances, reducing layout sensitivity.

The devices feature thermal shutdown, overcurrent protection (high-side sourcing and hiccup protection), and an internal 5V (25mA) LDO with undervoltage lockout. An externally adjustable voltage soft-start gradually ramps up the output voltage and reduces inrush current. At light loads, as soon as a low-side MOSFET zero-crossing event is detected, the devices automatically switch to pulse-skipping mode to keep the quiescent supply current low and enhances the light load efficiency. An independent enable input controls and the power-good output allow for flexible power sequencing.

The devices also provide the ability to start up into a prebiased output.

Controller Function—PWM Logic and Skip Mode

The devices employ PWM control with a constant switching frequency of 500kHz (MAX15066) or 350kHz (MAX15166) at medium and heavy loads, and skip mode at light loads. When EN is high, after a brief settling time, PWM operation starts when V_{SS} exceeds the FB voltage, at the beginning of soft-start.

The first operation is always a high-side turn-on at the beginning of the clock cycle. The high side is turned off when any of the following conditions occur:

1) COMP voltage exceeds the internal current-mode ramp waveform, which is the sum of the slope compensation ramp and the current-mode ramp derived from the inductor current waveform (through the current-sense block).
2) The high-side current limit is reached.
3) The maximum duty cycle of 90% is reached.

The low side turns off when the clock period ends or when the zero-crossing current threshold is intercepted. The devices monitor the inductor current during every switch cycle and automatically enters discontinuous mode when the inductor current valley intercepts the zero-crossing threshold (under light loads); under very light load conditions, skip mode is activated/deactivated on a cycle-by-cycle basis.

The devices enter discontinuous mode when load current (I_{LOAD}) and inductor ripple current (ΔI_L) are such that:

$$I_{LOAD} - \frac{\Delta I_L}{2} = I_{LOAD} - \frac{1}{2} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_{SW}} \right) \times \frac{V_{OUT}}{V_{IN}} = 0.21\text{A (typ)}$$

During skip-mode operation, the devices skip switch cycles, switching only as needed to service the load. This reduces the switching frequency and associated losses in the internal switch, the synchronous rectifier, and the inductor. In skip mode, to avoid the occasional switch cycle "bursts" (and reduce power losses), a fixed on-time is forecasted using a skip current-limit flag (0.58A, typ). The on-time, even if controlled by COMP, cannot be lower than the time needed for the inductor current to reach 0.58A.

Starting into a Prebiased Output

The devices are capable of safely soft-starting into a prebiased output without discharging the output capacitor. Starting up into a prebiased condition, both low-side and high-side switches remain off to avoid discharging the prebiased output. PWM operation starts only when the SS voltage crosses the FB voltage. During soft-start, zero crossing is activated to avoid reverse current in the device.

Enable Input and Power-Good Output

The devices feature independent device enable control and power-good signals that allow for flexible power sequencing. The enable input (EN) accepts a digital input with a 1.9V (typ) threshold. Apply a voltage exceeding the threshold on EN to enable the regulator, or connect EN to IN for always-on operations. Power-good (PGOOD) is an open-drain output that deasserts (goes high impedance) when V_{FB} is above 0.56V (typ), and asserts low if V_{FB} is below 0.545V (typ).

When the EN voltage is higher than 0.7V (typ) and lower than 1.9V (typ), most of the internal blocks are disabled; only an internal coarse preregulator, including the EN accurate comparator, is kept on. An external voltage-divider from IN to EN to GND can be used to set the device turn-on threshold.

Programmable Soft-Start (SS)

The devices utilize a soft-start feature to slowly ramp up the regulated output voltage to reduce input inrush current during startup. Connect a capacitor from SS to GND to set the startup time (see the *Setting the Soft-Start Time* section for capacitor selection details).

Internal LDO (V_{DD})

The devices include an internal 5V (typ) LDO. V_{DD} is externally compensated with a minimum 1µF, low-ESR ceramic capacitor. V_{DD} supplies the low-side switch driver, and the internal control logic. The V_{DD} output current limit is 90mA (typ) and a UVLO circuit inhibits switching when V_{DD} falls below 3.75V (typ).

Error Amplifier

A high gain-error amplifier provides accuracy for the voltage feedback loop regulation. Connect the necessary compensation network between COMP and GND (see the *Compensation Design Guidelines* for details). The error-amplifier transconductance is 1.6mS (typ). COMP clamp low is set to 0.68V (typ), just below the slope compensation ramp valley, helping COMP to rapidly return to correct set point during load and line transients.

PWM Comparator

The PWM comparator compares COMP voltage to the current-derived ramp waveform (LX current to COMP voltage transconductance value is 9A/V typ). To avoid instability due to subharmonic oscillations when the duty cycle is around 50% or higher, a slope compensation ramp is added to the current-derived ramp waveform. The compensation ramp (0.667V x 500kHz) for the MAX15066 and (0.667V x 350kHz) for the MAX15166 is equivalent to half of the inductor current down slope in the worst case (load 4A, current ripple 30% and maximum duty-cycle operation of 90%).

Overcurrent Protection and Hiccup Mode

When the converter output is shorted or the device is overloaded, the high-side MOSFET current-limit event (7.7A, typ) turns off the high-side MOSFET and turns on the low-side MOSFET. In addition, the device discharges the SS capacitor (C_{SS}) for a fixed period of time (70ns, typ) through the internal SS low-side switch R_{DS-ON} (R_{SS}). If the overcurrent condition persists, the device continues discharging C_{SS} until V_{SS} drops below 0.606V and a hiccup event is triggered. The regulator softly resets by pulling COMP low, turning off the high-side and turning on the low-side, until the low-side zero-crossing current threshold is reached. The high-side and low-side MOSFETs remain off and COMP is pulled low for a period equal to 21 times the nominal soft-start time (blanking time). This is obtained by charging SS from 0 to 0.606V with a 5µA (typ) current, and then slowly discharging it back to 0V with a 250nA (typ) current. After the blanking time has elapsed, the device attempts to restart. If the overcurrent fault has cleared, the device resumes normal operation. Otherwise, a new hiccup event is triggered (see the Output Short-Circuit Waveform in the *Typical Operating Characteristics*).

Thermal-Shutdown Protection

The devices contain an internal thermal sensor that limits the total power dissipation in the device and protects it in the event of an extended thermal fault condition. When the die temperature exceeds +160°C (typ), the thermal sensor shuts down the device, turning off the DC-DC converter and the LDO regulator to allow the die to cool. The regulator softly resets by pulling COMP low, discharging soft-start, turning off the high-side and turning on the low-side, until the low-side zero-crossing current threshold is reached. After the die temperature falls by 20°C (typ), the device restarts, using the soft-start sequence.

Applications Information

Setting the Output Voltage

Connect a resistive divider (R1 and R2, see Figure 3) from OUT to FB to GND to set the DC-DC converter output voltage. Choose R1 and R2 so that the DC errors due to the FB input bias current do not affect the output-voltage accuracy. With lower value resistors, the DC error is reduced, but the amount of power consumed in the resistive divider increases. A typical trade-off value for R2 is 10kΩ, but values between 5kΩ and 50kΩ are acceptable. Once R2 is chosen, calculate R1 using:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where the feedback threshold voltage V_{FB} = 0.606V (typ). When regulating an output of 0.606V, short FB to OUT and keep R2 connected from FB to GND.

Maximum/Minimum Voltage Conversion Ratio

The maximum voltage conversion ratio is limited by the maximum duty cycle (D_{MAX}):

$$\frac{V_{OUT}}{V_{IN}} < D_{MAX} + \frac{D_{MAX} \times V_{DROP2} + (1 - D_{MAX}) \times V_{DROP1}}{V_{IN}}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances. V_{DROP2} is an absolute value and the sum of the resistances in the charging path, including the high-side switch, inductor, and PCB resistances.

The minimum voltage conversion ratio is limited by the minimum duty cycle (D_{MIN}):

$$\frac{V_{OUT}}{V_{IN}} > D_{MIN} + \left[D_{MIN} \times \frac{V_{DROP2}}{V_{IN}} + (1 - D_{MIN}) \times \frac{V_{DROP1}}{V_{IN}}\right]$$

where $D_{MIN} = f_{OSC} \times t_{ON(min)}$; f_{OSC} is 500kHz/350kHz for the MAX15066/MAX15166, respectively, and $t_{ON(min)}$ is typically 150ns. See the specifications in the *Electrical Characteristics* table.

Inductor Selection

A larger inductor value results in reduced inductor ripple current, leading to a reduced output ripple voltage. However, a larger inductor value results in either a larger physical size or a higher series resistance (DCR) and a lower saturation current rating. Typically, the inductor value is chosen to have current ripple equal to 30% of load current. Choose the inductor with the following formula:

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where f_{SW} is the internally fixed switching frequency of 500kHz (MAX15066) or 350kHz (MAX15166), and ΔI_L is the estimated inductor ripple current (ΔI_L = LIR x I_{LOAD}, where LIR is the inductor current ratio). In addition, the peak inductor current, I_{L_PK}, must always be below both the minimum high-side current-limit value (7.7A, typ), and the inductor saturation current rating, I_{L_SAT}. Ensure that the following relationship is satisfied:

$$I_{L\_PK} = I_{LOAD} + \frac{1}{2} \times \Delta I_L < \min(I_{HSCL}, I_{L\_SAT})$$

Input Capacitor Selection

For a step-down converter, input capacitor C_{IN} helps reduce input ripple voltage, in spite of discontinuous input AC current. Low-ESR capacitors are preferred to minimize the voltage ripple due to ESR.

For low-ESR input capacitors, size C_{IN} using the following formula:

$$C_{IN} = \frac{I_{LOAD}}{f_{SW} \times \Delta V_{IN\_RIPPLE}} \times \frac{V_{OUT}}{V_{IN}}$$

For high-ESR input capacitors, the additional ripple contribution due to ESR ($\Delta V_{IN\_RIPPLE\_ESR}$) is calculated as follows:

$$\Delta V_{IN\_RIPPLE} = R_{ESR\_IN}(I_{LOAD} + \Delta I_L/2)$$

where R_{ESR_IN} is the ESR of the input capacitor. The RMS input ripple current is given by:

$$I_{RIPPLE} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

Output-Capacitor Selection

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and voltage-rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Estimate the output-voltage ripple due to the output capacitance, ESR, and ESL as follows:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = \frac{\Delta I_{P-P}}{8 \times C_{OUT} \times f_{SW}}$$

$$V_{RIPPLE(ESR)} = \Delta I_{P-P} \times ESR$$

and $V_{RIPPLE(ESL)}$ can be approximated as an inductive divider from LX to GND:

$$V_{RIPPLE\,(ESL)} = V_{LX} \times \frac{ESL}{L} = V_{IN} \times \frac{ESL}{L}$$

where V_{LX} swings from V_{IN} to GND.

The peak-to-peak inductor current (ΔI_{P-P}) is:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{V_{IN}}\right)}{L \times f_{SW}}$$

When using ceramic capacitors, which generally have low-ESR, $\Delta V_{RIPPLE(C)}$ dominates. When using electrolytic capacitors, $\Delta V_{RIPPLE(ESR)}$ dominates. Use ceramic capacitors for low ESR and low ESL at the switching frequency of the converter. The ripple voltage due to ESL is negligible when using ceramic capacitors.

As a general rule, a smaller inductor ripple current results in less output ripple voltage. Since inductor ripple current depends on the inductor value and input voltage, the output ripple voltage decreases with larger inductance and increases with higher input voltages. However, the inductor ripple current also impacts transient-response performance, especially at low V_{IN} to V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step.

Load-transient response also depends on the selected output capacitance. During a load transient, the output instantly changes by ESR x ΔI_{LOAD}. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time, the controller responds by regulating the output voltage back to the predetermined value.

Use higher C_{OUT} values for applications that require light-load operation or transition between heavy load and light load, triggering skip mode, causing output undershooting or overshooting. When applying the load, limit the output undershooting by sizing C_{OUT} according to the following formula:

$$C_{OUT} = \frac{\Delta I_{LOAD}}{3 f_{CO} \times \Delta V_{OUT}}$$

where ΔI_{LOAD} is the total load change, f_{CO} is the unity-gain bandwidth (or zero-crossing frequency), and ΔV_{OUT} is the desired output undershooting. When removing the load and entering skip mode, the device cannot control output overshooting, since it has no sink current capability; see the *Skip Mode Frequency and Output Ripple* section to properly size C_{OUT} under this circumstance.

A worst-case analysis in sizing the minimum output capacitance takes the total energy stored in the inductor into account, as well as the allowable sag/soar (undershoot/overshoot) voltage as follows:

$$C_{OUT\,(MIN)} = \frac{L \times \left(I^2_{OUT(MAX)} - I^2_{OUT(MIN)}\right)}{(V_{FIN} + V_{SOAR})^2 - V^2_{INIT}}, \text{voltage soar (overshoot)}$$

$$C_{OUT(MIN)} = \frac{L \times \left(I^2_{OUT(MAX)} - I^2_{OUT(MIN)}\right)}{V^2_{INIT} - (V_{FIN} - V_{SAG})^2}, \text{voltage sag (undershoot)}$$

where $I_{OUT(MAX)}$ and $I_{OUT(MIN)}$ are the initial and final values of the load current during the worst-case load dump, V_{INIT} is the initial voltage prior to the transient, V_{FIN} is the steady-state voltage after the transient, V_{SOAR} is the allowed voltage soar (overshoot) above V_{FIN}, and V_{SAG} is the allowable voltage sag below V_{FIN}. The terms (V_{FIN} + V_{SOAR}) and (V_{FIN} - V_{SAG}) represent the maximum/minimum transient output voltage reached during the transient, respectively.

Use these equations for initial output-capacitor selection. Determine final values by testing a prototype or an evaluation circuit under the worst-case conditions.

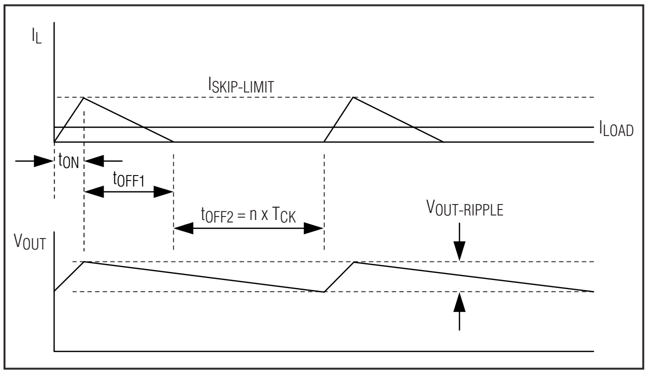


Figure 2. Skip Mode Waveform

Skip Mode Frequency and Output Ripple

In skip mode, the switching frequency (f_{SKIP}) and output ripple voltage (V_{OUT_RIPPLE}) shown in Figure 2 are calculated as follows:

t_{ON} is the time needed for inductor current to reach SKIP current limit (0.58A, typ):

$$t_{ON} = \frac{L \times I_{SKIP-LIMIT}}{V_{IN} - V_{OUT}} \quad [1]$$

t_{OFF1} is the time needed for inductor current to reach the zero current limit (~0A):

$$t_{OFF1} = \frac{L \times I_{SKIP-LIMIT}}{V_{OUT}} \quad [2]$$

During t_{ON} and t_{OFF1} the output capacitor stores a charge equal to (see Figure 2):

$$\Delta Q_{OUT} = \left[\frac{1}{2} I_{SKIP-LIMIT} \times (t_{ON} + t_{OFF1})\right] - \left[I_{LOAD} \times (t_{ON} + t_{OFF1})\right] \quad [3]$$

Combining [1], [2] and [3], and solving for ΔQ_{OUT}:

$$\Delta Q_{OUT} = \frac{L \times I_{SKIP-LIMIT} \times \left(\frac{I_{SKIP-LIMIT}}{2} - I_{LOAD}\right) \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)}{2}$$

During t_{OFF2} (= n x t_{CK}, number of clock cycles skipped), the output capacitor loses this charge or can approximate as:

$$t_{OFF2} = \frac{\Delta Q_{OUT}}{I_{LOAD}}$$

or approximately as:

$$t_{OFF2} = \frac{L \times I_{SKIP-LIMIT} \times \left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right) \times \left(\frac{I_{SKIP-LIMIT}}{2} - I_{LOAD}\right)}{I_{LOAD}}$$

Finally, frequency in skip mode is:

$$f_{SKIP} = \frac{1}{t_{ON} + t_{OFF1} + t_{OFF2}}$$

Output ripple in skip mode is:

$$V_{OUT-RIPPLE} = V_{COUT-RIPPLE} + V_{ESR-RIPPLE} = \frac{(I_{SKIP-LIMIT} - I_{LOAD}) \times t_{ON}}{C_{OUT}} + R_{ESR,COUT} \times (I_{SKIP-LIMIT} - I_{LOAD})$$

To limit output ripple in skip mode, size C_{OUT} based on the above formula accordingly. All formulas above are valid for $I_{LOAD} < I_{SKIP-LIMIT}$.

Compensation Design Guidelines

The devices use a fixed-frequency, peak current-mode control scheme to provide easy compensation and fast transient response. The inductor peak current is monitored on a cycle-by-cycle basis and compared to the COMP voltage (output of the voltage error amplifier). The regulator's duty cycle is modulated based on the inductor's peak current value. This cycle-by-cycle control of the inductor current emulates a controlled current source. As a result, the inductor's pole frequency is shifted beyond the gain bandwidth of the regulator.

System stability is provided with the addition of a simple series capacitor-resistor from COMP to GND. This pole-zero combination serves to tailor the desired response of the closed-loop system.

The basic regulator loop consists of a power modulator (comprising the regulator's pulse-width modulator, slope compensation ramp, control circuitry, MOSFETs, and inductor), the capacitive output filter and load, an output feedback divider, and a voltage-loop error amplifier with its associated compensation circuitry (see Figure 3).

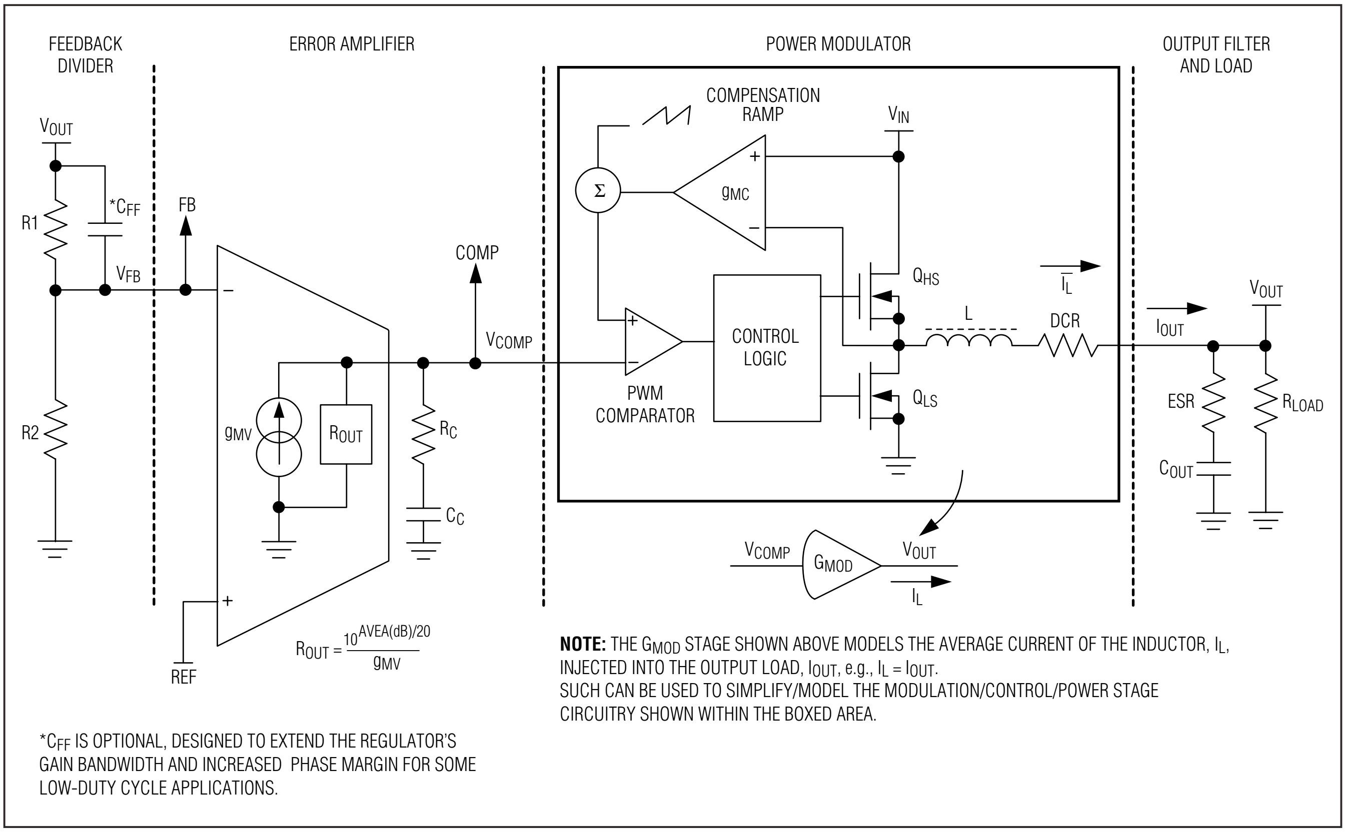


Figure 3. Peak Current-Mode Regulator Transfer Model

The average current through the inductor is expressed as:

$$\overline{I_L} = G_{MOD} \times \overline{V_{COMP}}$$

where $\overline{I_L}$ is the average inductor current and G_{MOD} is the power modulator's transconductance. For a buck converter:

$$\overline{V_{OUT}} = R_{LOAD} \times \overline{I_L}$$

where R_{LOAD} is the equivalent load resistor value. Combining the above two relationships, the power modulator's transfer function in terms of V_{OUT} with respect to V_{COMP} is:

$$\frac{\overline{V_{OUT}}}{\overline{V_{COMP}}} = \frac{R_{LOAD} \times \overline{I_L}}{\left(\frac{\overline{I_L}}{G_{MOD}}\right)} = R_{LOAD} \times G_{MOD}$$

The peak current-mode controller's modulator gain is attenuated by the equivalent divider ratio of the load resistance and the current-loop gain. G_{MOD} becomes:

$$G_{MOD}(DC) = g_{MC} \times \frac{1}{\left\{1 + \frac{R_{LOAD}}{f_{SW} \times L} \times \left[K_S \times (1 - D) - 0.5\right]\right\}}$$

where $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$, f_{SW} is the switching frequency, L is the output inductance, D is the duty cycle (V_{OUT}/V_{IN}), and K_S is the slope compensation factor calculated from the following equation:

$$K_S = 1 + \frac{S_{SLOPE}}{S_N} = 1 + \frac{V_{SLOPE} \times f_{SW} \times L \times g_{MC}}{(V_{IN} - V_{OUT})}$$

where:

$$S_{SLOPE} = \frac{V_{SLOPE}}{t_{SW}} = V_{SLOPE} \times f_{SW}$$

$$S_N = \frac{(V_{IN} - V_{OUT})}{L \times g_{MC}}$$

As previously mentioned, the power modulator's dominate pole is a function of the parallel effects of the load resistance and the current-loop gain's equivalent impedance:

$$f_{PMOD} = \frac{1}{2\pi \times C_{OUT} \times \left[ESR + \left(\frac{1}{R_{LOAD}} + \frac{\left[K_S \times (1-D) - 0.5\right]}{f_{SW} \times L}\right)^{-1}\right]}$$

Knowing that the ESR is typically much smaller than the parallel combination of the load and the current loop, e.g.,:

$$ESR << \left(\frac{1}{R_{LOAD}} + \frac{\left[K_S \times (1-D) - 0.5\right]}{f_{SW} \times L}\right)^{-1}$$

$$f_{PMOD} \approx \frac{1}{2\pi \times C_{OUT} \times \left(\frac{1}{R_{LOAD}} + \frac{\left[K_S \times (1-D) - 0.5\right]}{f_{SW} \times L}\right)^{-1}}$$

This can be expressed as:

$$f_{PMOD} \approx \frac{1}{2\pi \times C_{OUT} \times R_{LOAD}} + \frac{\left[K_S \times (1-D) - 0.5\right]}{2\pi \times f_{SW} \times L \times C_{OUT}}$$

Note: Depending on the application's specifics, the amplitude of the slope compensation ramp could have a significant impact on the modulator's dominate pole. For low duty-cycle applications, it provides additional damping (phase lag) at/near the crossover frequency. See the *Closing the Loop: Designing the Compensation Circuitry* section. There is no equivalent effect on the power modulator zero:

$$f_{ZMOD} = f_{ZESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

The effect of the inner current loop at higher frequencies is modeled as a double-pole (complex conjugate) frequency term, $G_{SAMPLING}(s)$, as shown:

$$G_{SAMPLING}(s) = \frac{1}{\frac{s^2}{(\pi \times f_{SW})^2} + \frac{s}{\pi \times f_{SW} \times Q_C} + 1}$$

where the sampling effect quality factor, Q_C, is:

$$Q_C = \frac{1}{\pi \times \left[K_S \times (1-D) - 0.5\right]}$$

and the resonant frequency is:

$$\omega_{SAMPLING}(s) = \pi \times f_{SW}$$

or:

$$f_{SAMPLING} = \frac{f_{SW}}{2}$$

Having defined the power modulator's transfer function, the total system transfer can be written as follows (Figure 3):

$$Gain(s) = G_{FF}(s) \times G_{EA}(s) \times G_{MOD}(DC) \times G_{FILTER}(s) \times G_{SAMPLING}(s)$$

where:

$$G_{FF}(s) = \frac{R2}{R1 + R2} \times \frac{(sC_{FF}R1 + 1)}{\left[sC_{FF}(R1 || R2) + 1\right]}$$

Leaving C_{FF} empty, $G_{FF}(s)$ becomes:

$$G_{FF}(s) = \frac{R2}{R1 + R2}$$

Also:

$$G_{EA}(s) = 10^{AVEA(dB)/20} \times \frac{(sC_C R_C + 1)}{\left[sC_C\left(R_C + \frac{10^{AVEA(dB)/20}}{g_{MV}}\right) + 1\right]}$$

If $R_C << \frac{10^{AVEA(dB)/20}}{g_{MV}}$, the equation simplifies to:

$$G_{EA}(s) = 10^{AVEA(dB)/20} \times \frac{(sC_C R_C + 1)}{\left[sC_C\left(\frac{10^{AVEA(dB)/20}}{g_{MV}}\right) + 1\right]}$$

$$G_{FILTER}(s) = R_{LOAD} \times \frac{(sC_{OUT}ESR + 1)}{\left(sC_{OUT}\left\{\frac{1}{2\pi \times R_{LOAD}} + \frac{\left[K_S \times (1-D) - 0.5\right]}{2\pi \times f_{SW} \times L}\right\}^{-1} + 1\right)}$$

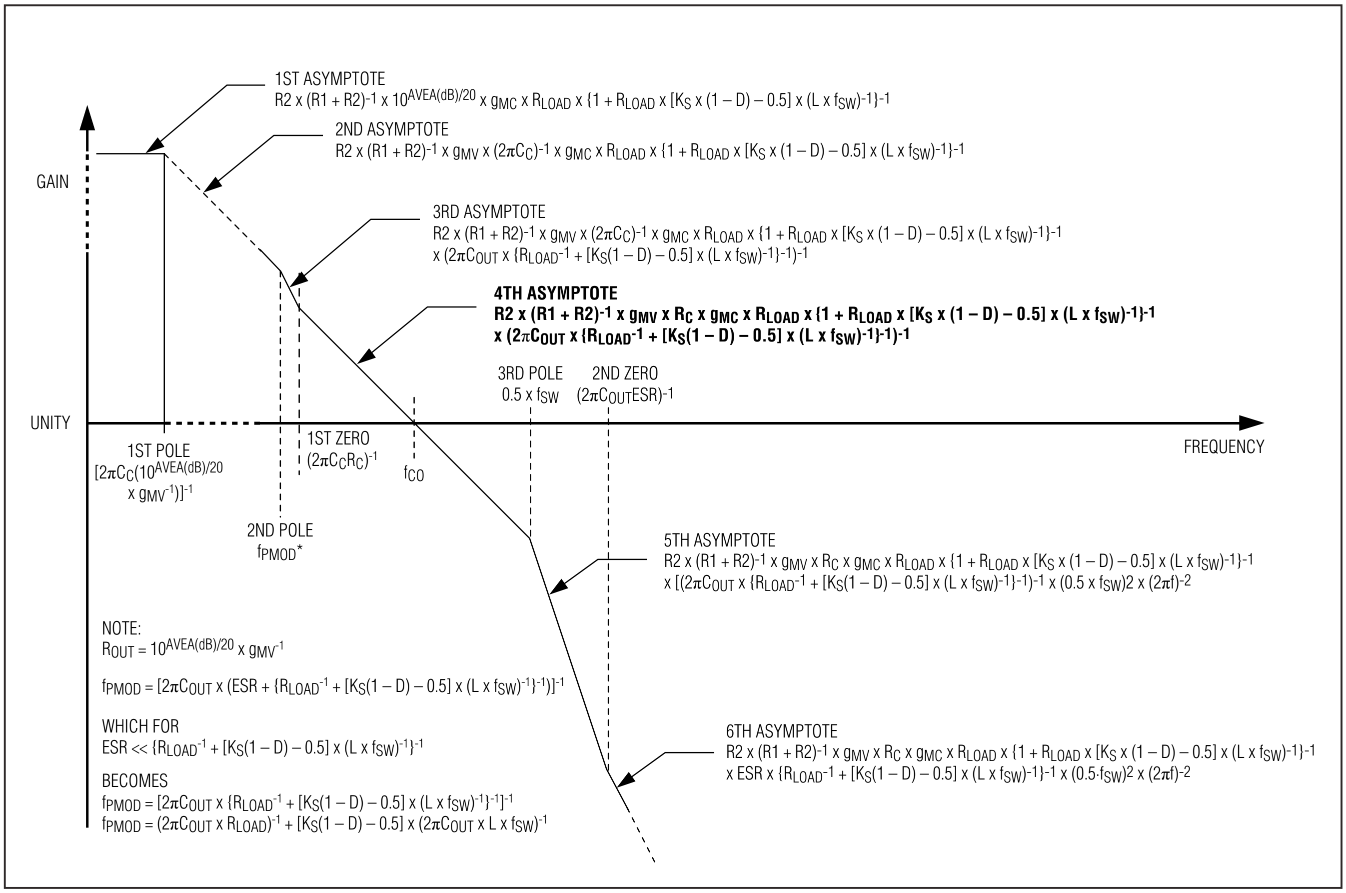


Figure 4. Asymptotic Loop Response of Peak Current-Mode Regulator

The dominant poles and zeros of the transfer loop gain are shown below:

$$f_{P1} << \frac{g_{MV}}{2\pi \times C_C \times 10^{AVEA(dB)/20}}$$

$$f_{P2} = \frac{1}{2\pi \times C_{OUT}\left(\frac{1}{R_{LOAD}} + \frac{[K_S \times (1 - D) - 0.5]}{f_{SW} \times L}\right)^{-1}}$$

$$f_{P3} = \frac{f_{SW}}{2}$$

$$f_{Z1} = \frac{1}{2\pi \times C_C R_C} \quad f_{Z2} = \frac{1}{2\pi \times C_{OUT} ESR}$$

The order of pole-zero occurrences is:

$$f_{P1} < f_{P2} \leq f_{Z1} < f_{CO} < f_{P3} < f_{Z2}$$

Note: Under heavy load, f_{P2} can approach f_{Z1}.

Figure 4 shows a graphical representation of the asymptotic system closed-loop response, including dominant pole and zero locations.

The loop response's fourth asymptote (in bold, Figure 4) is the one of interest in establishing the desired crossover frequency (and determining the compensation component values). A lower crossover frequency provides for stable closed-loop operation at the expense of a slower load and line transient response. Increasing the crossover frequency improves the transient response at the (potential) cost of system instability. A standard rule of thumb sets the crossover frequency ≤ 1/5 to 1/10 of the switching frequency.

First, select the passive power components that meet the application's requirements. Then, choose the small-signal compensation components to achieve the desired closed-loop frequency response and phase margin as outlined in the *Closing the Loop: Designing the Compensation Circuitry* section.

Closing the Loop: Designing the Compensation Circuitry

1) Select the desired crossover frequency. Choose f_{CO} between 1/5 to 1/10 of f_{SW}.
2) Select R_C by setting the system transfer's fourth asymptote gain equal to unity (assuming $f_{CO} > f_{Z1}$, f_{P2}, and f_{P1}). R_C becomes:

$$R_C = \frac{R1+R2}{R2} \times \frac{\left(1+\frac{R_{LOAD}K_S\left[(1-D)-0.5\right]}{L \times f_{SW}}\right)}{g_{MV} \times g_{MC} \times R_{LOAD}} \times 2\pi f_{CO} C_{OUT} \times \left[ESR + \frac{1}{\left(\frac{1}{R_{LOAD}} + \frac{K_S\left[(1-D)-0.5\right]}{L \times f_{SW}}\right)}\right]$$

and where the ESR is much smaller than the parallel combination of the equivalent load resistance and the current-loop impedance, e.g.,:

$$ESR << \frac{1}{\left(\frac{1}{R_{LOAD}} + \frac{K_S\left[(1-D)-0.5\right]}{L \times f_{SW}}\right)}$$

R_C becomes:

$$R_C = \frac{R1+R2}{R2} \times \frac{2\pi f_{CO} \times C_{OUT}}{g_{MV} \times g_{MC}}$$

3) Select C_C. C_C is determined by selecting the desired first system zero, f_{Z1}, based on the desired phase margin. Typically, setting f_{Z1} below 1/5 of f_{CO} provides sufficient phase margin.

$$f_{Z1} = \frac{1}{2\pi \times C_C R_C} \le \frac{f_{CO}}{5}$$

therefore:

$$C_C \ge \frac{5}{2\pi \times f_{CO} \times R_C}$$

Optional: For low duty-cycle applications, the addition of a phase-leading capacitor (C_{FF} in Figure 3) helps mitigate the phase lag of the damped half-frequency double pole. Adding a second zero near to but below the desired crossover frequency increases both the closed-loop phase margin and the regulator's unity-gain bandwidth (crossover frequency). Select the capacitor as follows:

$$C_{FF} = \frac{1}{2\pi \times f_{CO} \times (R1 \| R2)}$$

This guarantees the additional phase-leading zero occurs at a frequency lower than f_{CO} from:

$$f_{PHASE\_LEAD} = \frac{1}{2\pi \times C_{FF} \times R1}$$

Using C_{FF}, the zero-pole order is adjusted as follows:

$$f_{P1} < f_{P2} \le f_{Z1} < \frac{1}{2\pi C_{FF} R1} < \frac{1}{2\pi C_{FF}(R1 \| R2)} \approx f_{CO} < f_{P3} < f_{Z2}$$

Confirm the desired operation of C_{FF} empirically. The phase lead of C_{FF} diminishes as the output voltage is a smaller multiple of the reference voltage, e.g., below about 1V. Do not use C_{FF} when $V_{OUT} = V_{FB}$.

Setting the Soft-Start Time

The soft-start feature ramps up the output voltage slowly, reducing input inrush current during startup. Size the C_{SS} capacitor to achieve the desired soft-start time (t_{SS}) using:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{FB}}$$

I_{SS}, the soft-start current, is 5μA (typ) and V_{FB}, the output feedback voltage threshold, is 0.606V (typ). When using large C_{OUT} capacitance values, the high-side current limit can trigger during soft-start period. To ensure the correct soft-start time t_{SS}, choose C_{SS} large enough to satisfy:

$$C_{SS} >> C_{OUT} \times \frac{V_{OUT} \times I_{SS}}{(I_{HSCL} - I_{OUT}) \times V_{FB}}$$

I_{HSCL} is the typical high-side switch current-limit value.

Layout Procedure

Careful PCB layout is critical to achieve clean and stable operation. It is highly recommended to duplicate the MAX15066/MAX15166 evaluation kit layout for optimum performance. If deviation is necessary, follow these guidelines for good PCB layout:

1) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane. Connect the signal ground plane to the power ground plane at a single point adjacent to the ground bump of the IC.
2) Place capacitors on V_{DD}, IN, and SS as close as possible to the device and the corresponding pin using direct traces. Keep the power ground plane and signal ground plane separate. Connect all GND bumps at only one common point near the input bypass capacitor return terminal.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current short and minimize the loop area formed by LX, the output capacitors, and the input capacitors.
4) Connect IN, LX, and GND separately to large copper areas to help cool the device to further improve efficiency and long-term reliability.
5) For better thermal performance, maximize the copper trace widths for consecutive bumps (LX, IN, GND) using solder mask (SMD) lands.
6) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the device.
7) Route high-speed switching nodes (such as LX and BST) away from sensitive analog areas (such as SS, FB, and COMP).

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	FREQUENCY
MAX15066EWE+	-40°C to +85°C	16 WLP	500kHz
MAX15166EWE+	-40°C to +85°C	16 WLP	350kHz

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W162B2+1	21-0200	—

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/10	Initial release	—
1	4/10	Revised the *General Description*, *Absolute Maximum Ratings*, *Typical Operating Characteristics*, and the *PWM Comparator*, *Output-Capacitor Selection*, *Compensation Design Guidelines*, and the *Closing the Loop: Designing the Compensation Circuitry* sections. Updated Figures 3 and 4.	1, 2, 4, 10, 13, 15–18
2	5/10	Revised the *Electrical Characteristics*, *PWM Comparator*, *Output Capacitor Selection*, *Skip Mode Frequency and Output Ripple*, *Compensation Design Guidelines*, *Closing the Loop: Designing the Compensation Circuitry,* and the *Layout Procedure* sections and Figures 3 and 4.	3, 11, 13–19
3	9/10	Revised the *Electrical Characteristics* and *PWM Comparator* sections.	3, 11
4	5/13	Added MAX15166	1–20
5	1/15	Updated *Benefits and Features* section	1

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