

**Benefits**

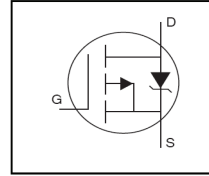
- Advanced Process Technology
- Surface Mount (IRF9530NS)
- Low-profile through-hole (IRF9530NL)
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated
- Lead-Free

**Description**

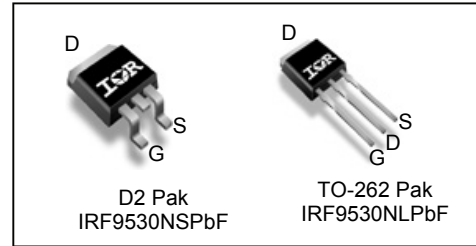
Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D2Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D2Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF9530NL) is available for low-profile applications.

**HEXFET® Power MOSFET**


<b>V<sub>DSS</sub></b>	<b>-100V</b>
<b>R<sub>DS(on)</sub></b>	<b>0.20Ω</b>
<b>I<sub>D</sub></b>	<b>-14A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF9530NLPbF	TO-262	Tube	50	IRF9530NLPbF (Obsolete)
IRF9530NSPbF	D2-Pak	Tape and Reel Left	800	IRF9530NSTRLPbF

**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ -10V ⑤	-14	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ -10V ⑤	-10	
I <sub>DM</sub>	Pulsed Drain Current ①⑤	-56	
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Maximum Power Dissipation	3.8	W
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	79	W
	Linear Derating Factor	0.53	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②⑤	250	mJ
I <sub>AR</sub>	Avalanche Current ①	-8.4	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	7.9	mJ
dv/dt	Peak Diode Recovery dv/dt③⑤	-5.0	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	


**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	1.9	°C/W
R <sub>θJA</sub>	Junction-to-Ambient ( PCB Mount, steady state) ⑥	—	40	

**Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

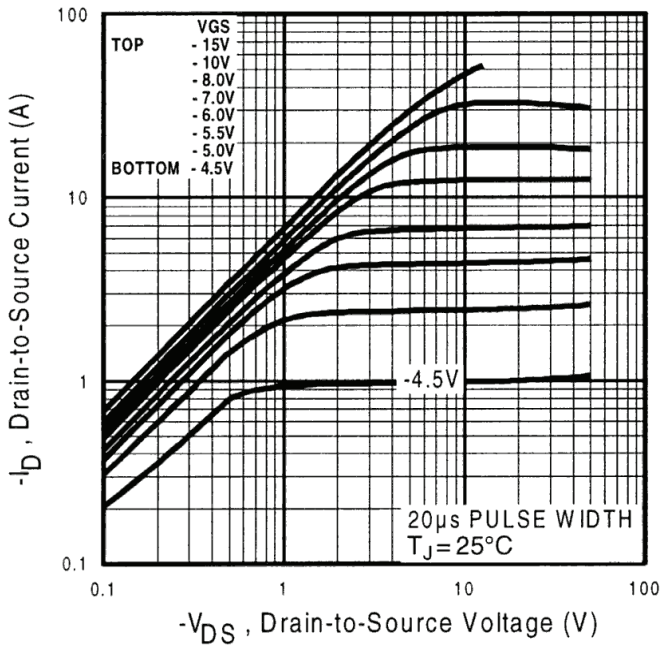
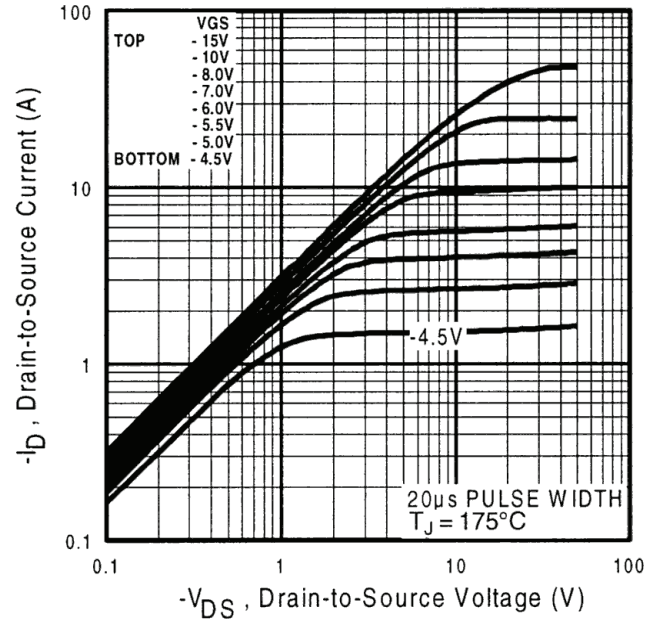
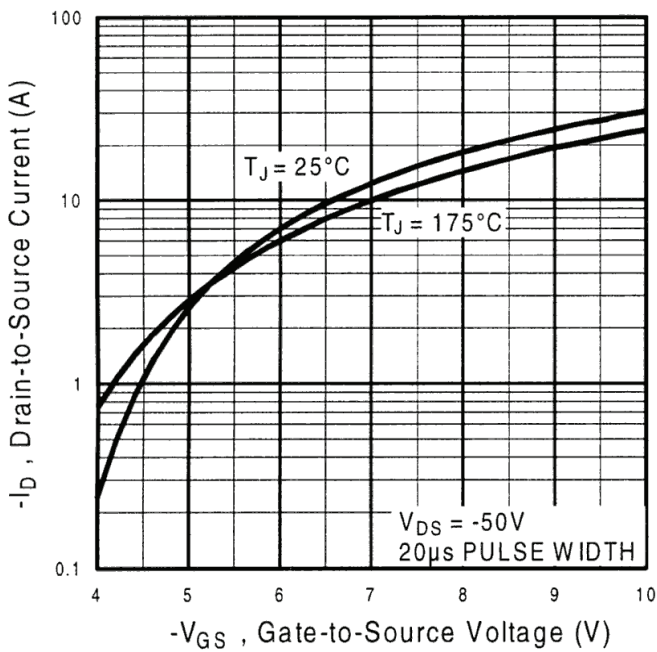
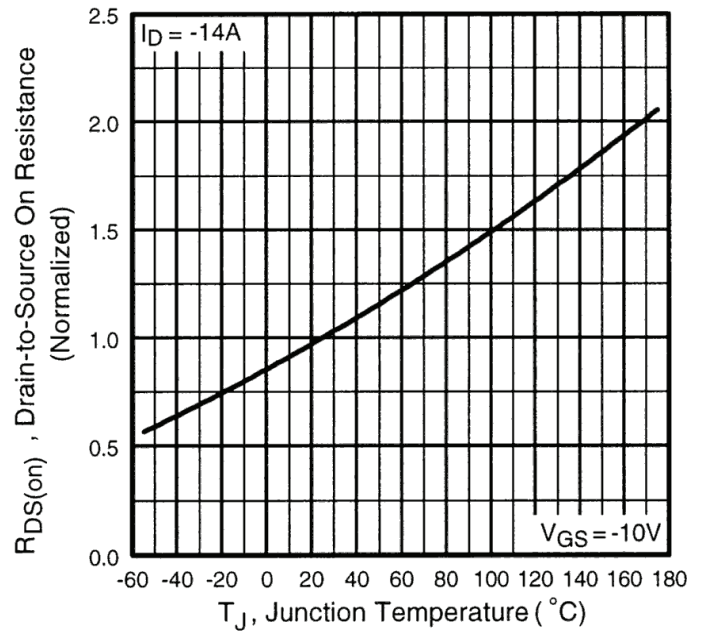
	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	-100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1mA ⑤
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.20	Ω	V <sub>GS</sub> = -10V, I <sub>D</sub> = -8.4A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-2.0	—	-4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
g <sub>fs</sub>	Forward Trans conductance	3.2	—	—	S	V <sub>DS</sub> = -50V, I <sub>D</sub> = -8.4A ⑤
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	-25	μA	V <sub>DS</sub> = -100V, V <sub>GS</sub> = 0V
		—	—	-250		V <sub>DS</sub> = -80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	-100	nA	V <sub>GS</sub> = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V <sub>GS</sub> = 20V
Q <sub>g</sub>	Total Gate Charge	—	—	58	nC	I <sub>D</sub> = -8.4A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	8.3		V <sub>DS</sub> = -80V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	—	32		V <sub>GS</sub> = -10V See Fig.6 and 13 ④⑤
t <sub>d(on)</sub>	Turn-On Delay Time	—	15	—	ns	V <sub>DD</sub> = -50V
t <sub>r</sub>	Rise Time	—	58	—		I <sub>D</sub> = -8.4A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	45	—		R <sub>G</sub> = 9.1Ω
t <sub>f</sub>	Fall Time	—	46	—		R <sub>D</sub> = 6.2Ω See Fig.6 ④⑤
L <sub>S</sub>	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C <sub>iss</sub>	Input Capacitance	—	760	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	260	—		V <sub>DS</sub> = -25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	170	—		f = 1.0MHz, See Fig. 5 ⑤

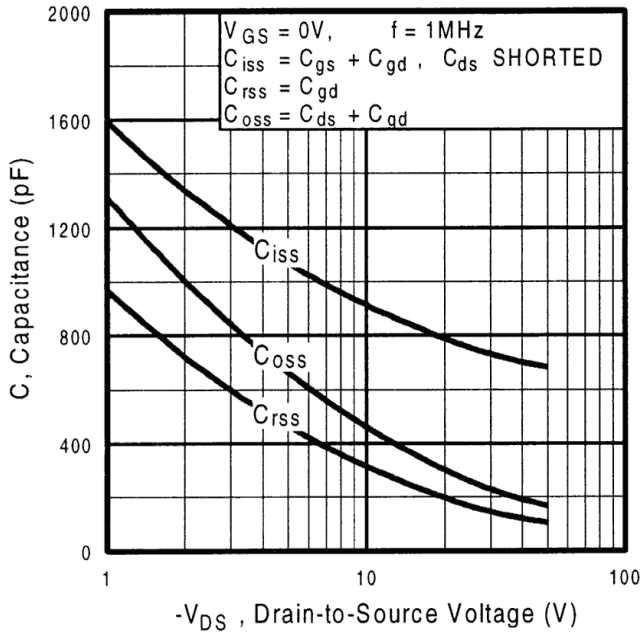
**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-14	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	-56		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-1.6	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = -8.4A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	130	190	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = -8.4A
Q <sub>rr</sub>	Reverse Recovery Charge	—	650	970	nC	di/dt = -100A/μs ④⑤
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

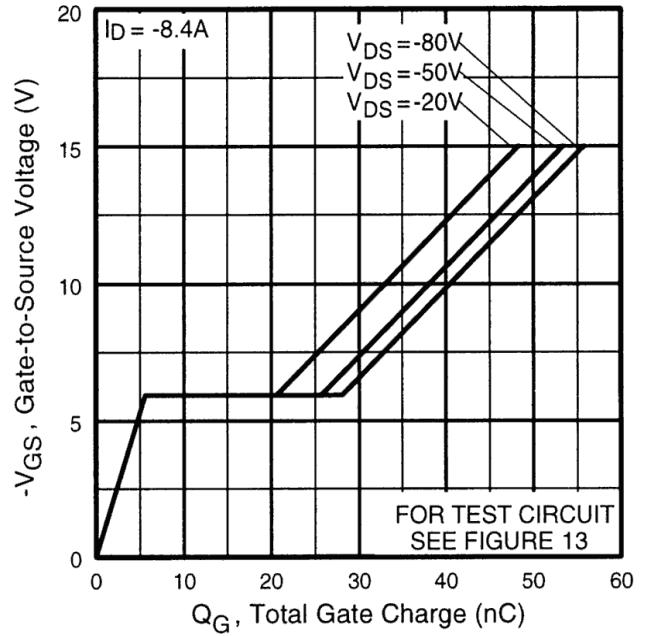
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② starting T<sub>J</sub> = 25°C, L = 7.0mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = -8.4A. (See fig. 12)
- ③ I<sub>SD</sub> ≤ -8.4A, di/dt ≤ -490A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Uses IRF9530N data and test conditions.
- ⑥ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994

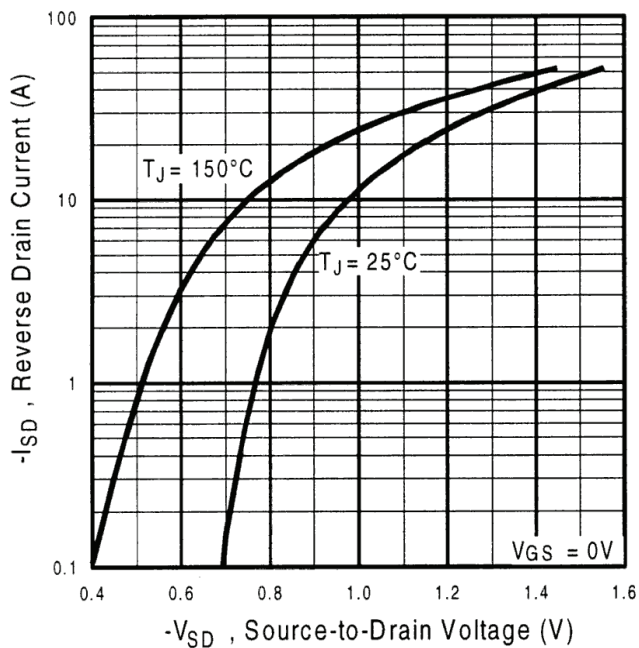

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Normalized On-Resistance vs. Temperature



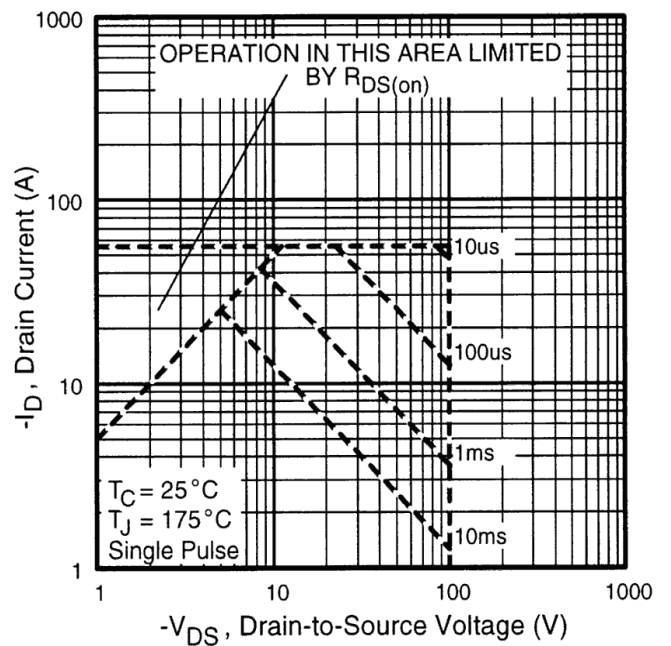
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



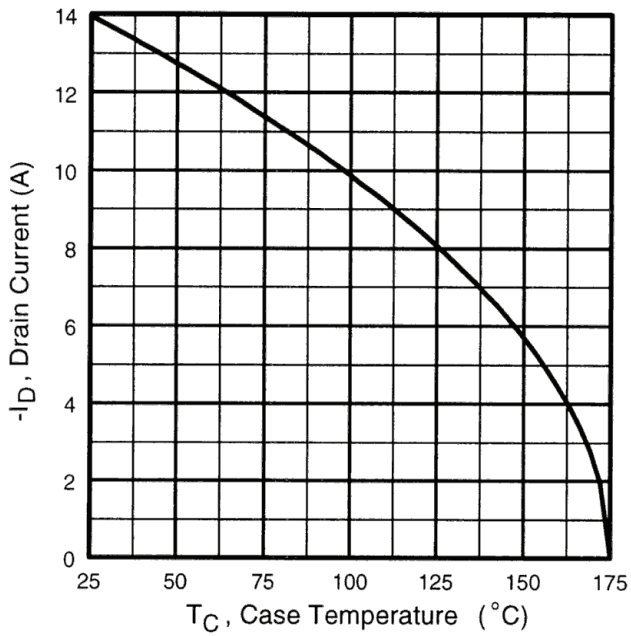
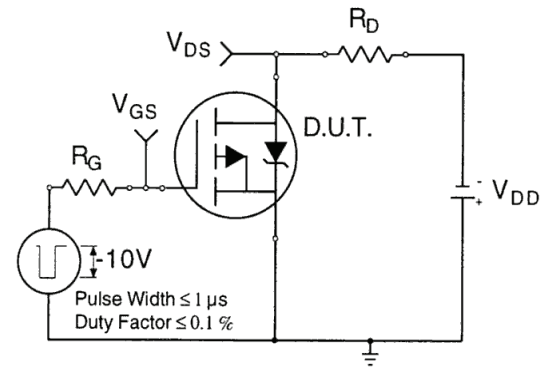
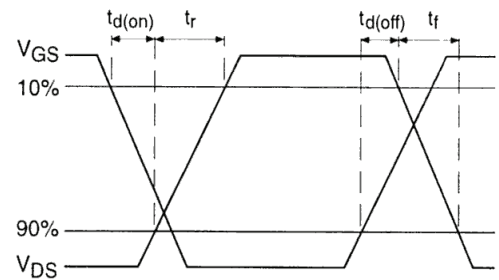
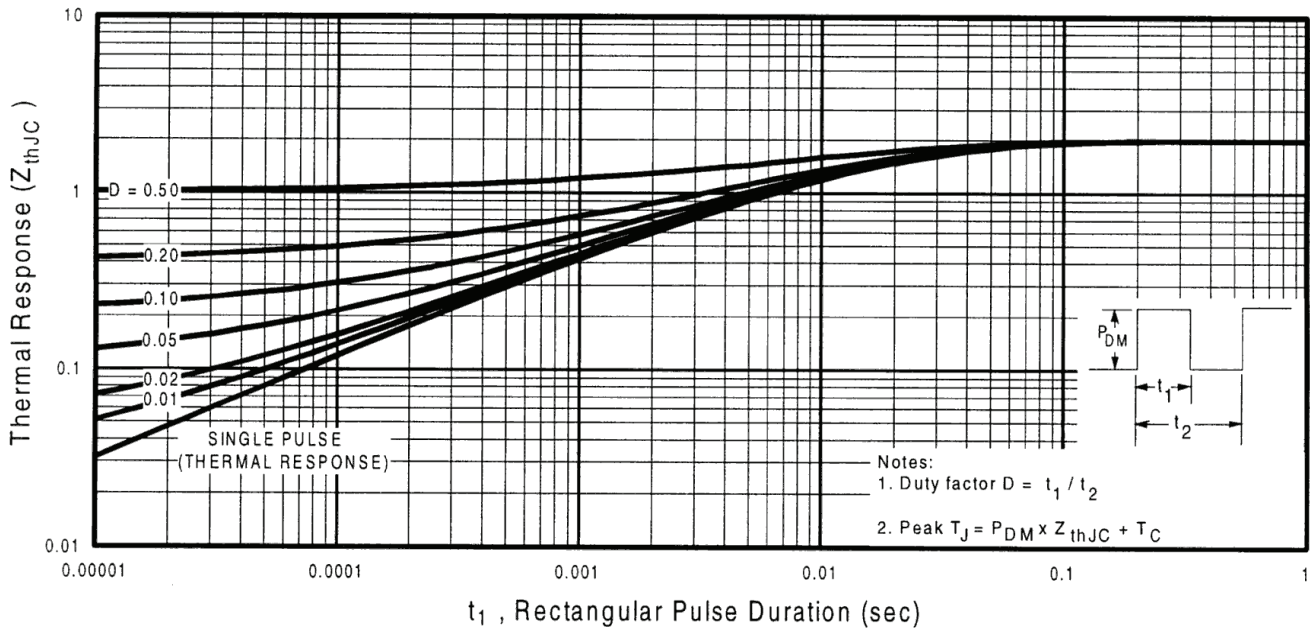
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

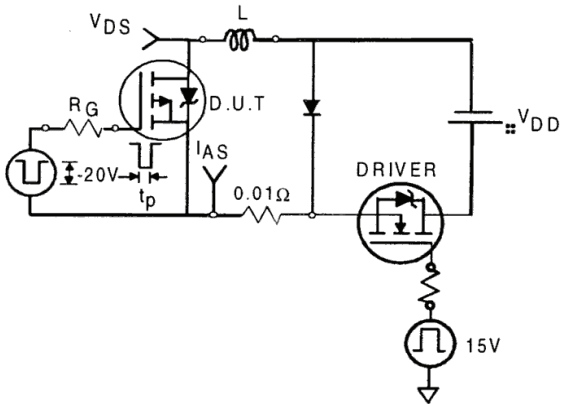
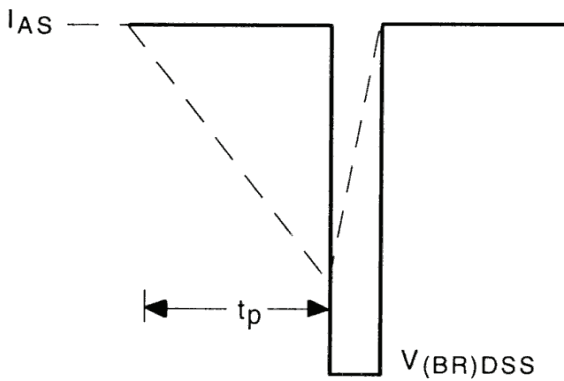
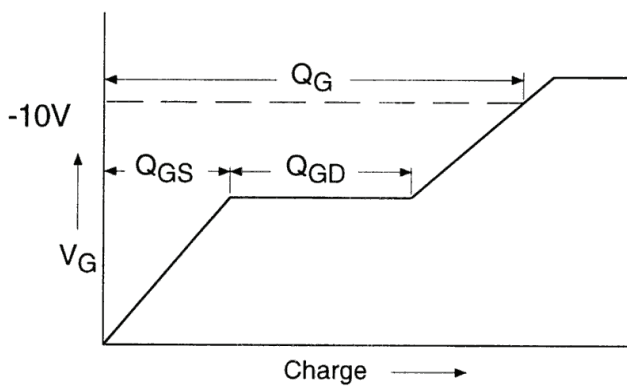
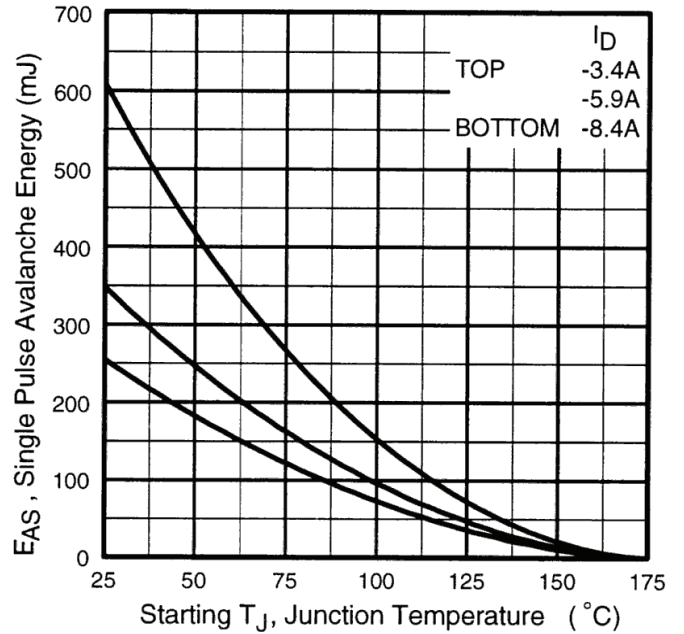
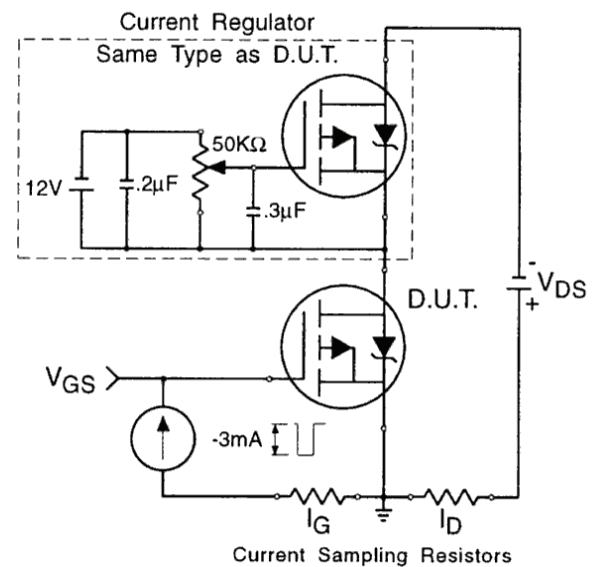


**Fig 7** Typical Source-to-Drain Diode Forward Voltage

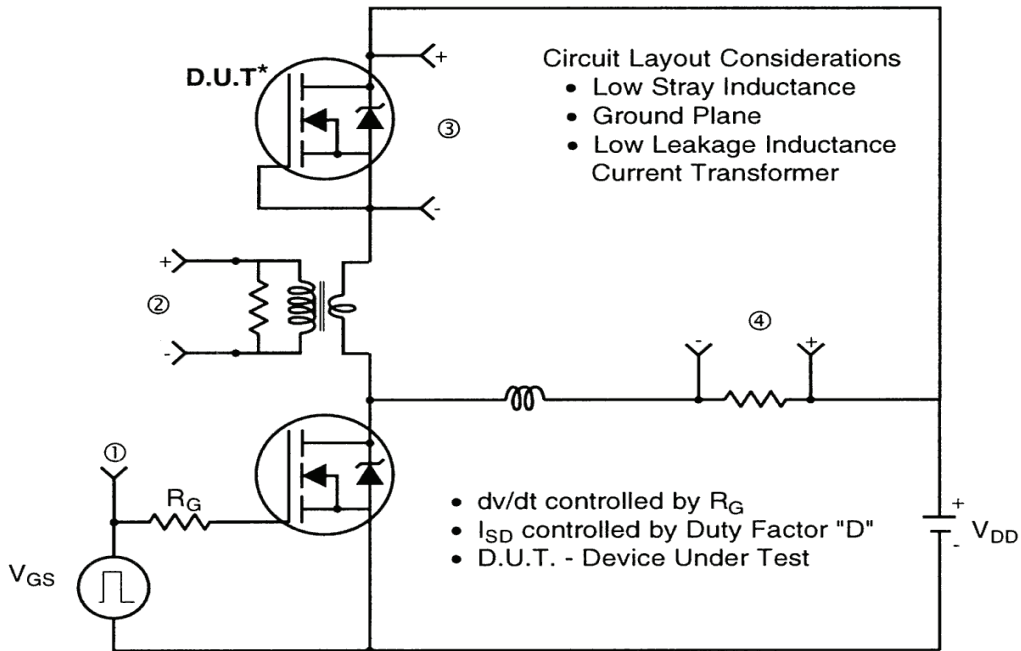


**Fig 8.** Maximum Safe Operating Area

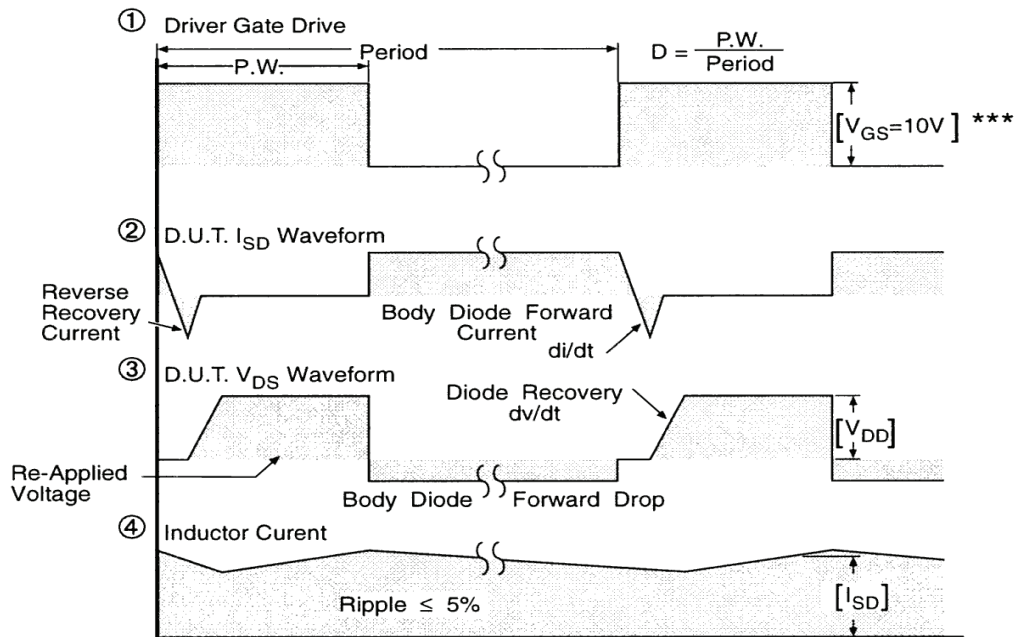

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10a.** Switching Time Test Circuit

**Fig 10b.** Switching Time Waveforms

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case


**Fig 12a.** Unclamped Inductive Test Circuit

**Fig 12b.** Unclamped Inductive Waveforms

**Fig 13a.** Gate Charge Waveform

**Fig 12c.** Maximum Avalanche Energy vs. Drain Current

**Fig 13b.** Gate Charge Test Circuit

### Peak Diode Recovery dv/dt Test Circuit



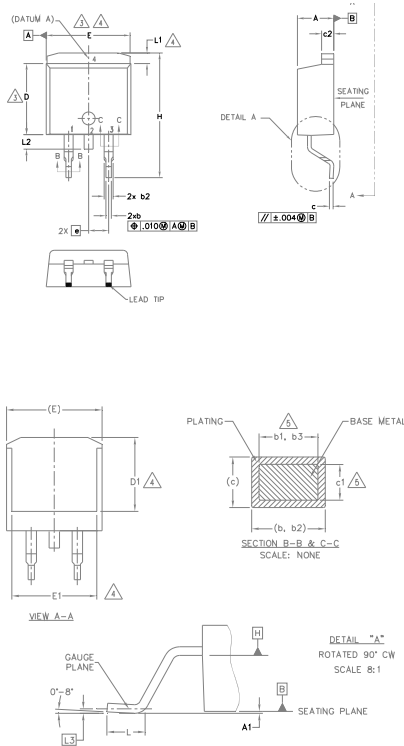
\* Reverse Polarity of D.U.T for P-Channel



\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 14.** Peak Diode Recovery  $dv/dt$  Test Circuit for PChannel HEXFET® Power MOSFETs



**D2-Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [".005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	—	.270	—	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	4
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

**LEAD ASSIGNMENTS**
**DIODES**

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

**HEXFET**

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

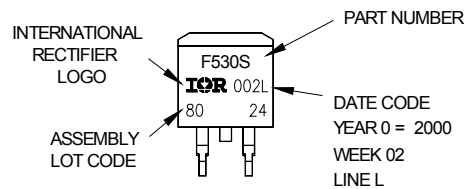
**IGBTs, CoPACK**

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

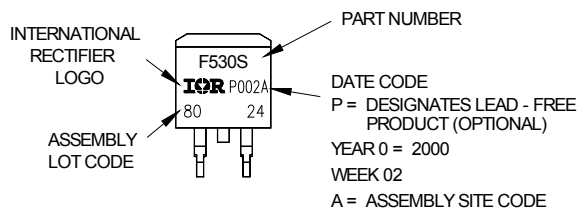
**D2-Pak (TO-263AB) Part Marking Information**

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position  
indicates "Lead - Free"

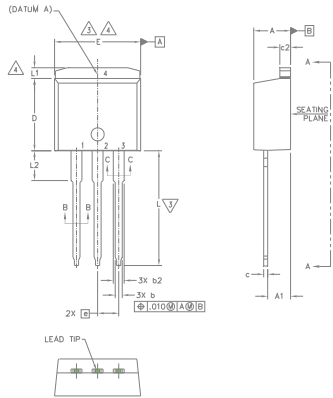


OR



Note: For the most current drawing please refer to Infineon's web site [www.infineon.com](http://www.infineon.com)



**TO-262 Package Outline (Dimensions are shown in millimeters (inches))**


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
  5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  6. CONTROLLING DIMENSION: INCH.
  7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

**LEAD ASSIGNMENTS**
**IGBTs, CoPACK**

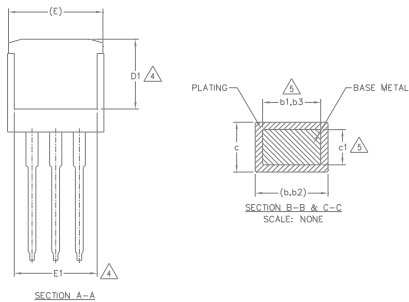
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**DIODES**

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

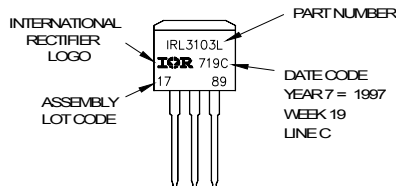


SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

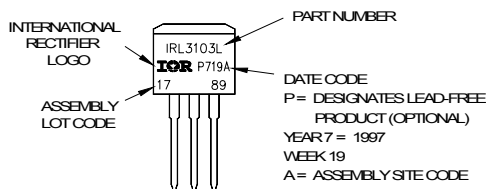
**TO-262 Part Marking Information**

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW19, 1997  
 IN THE ASSEMBLY LINE "C"

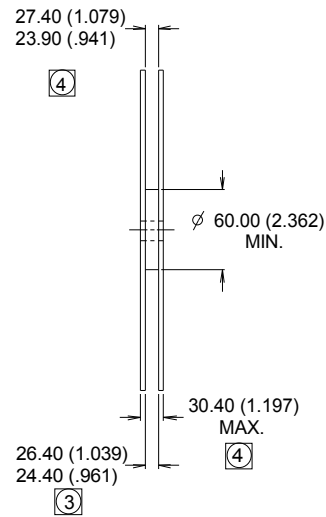
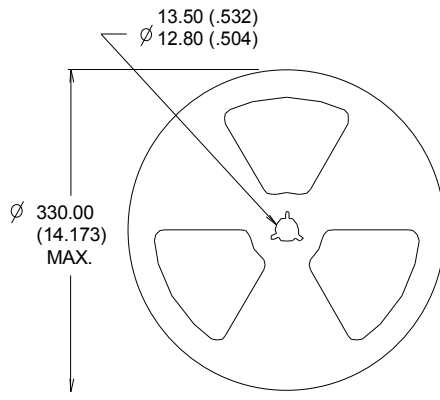
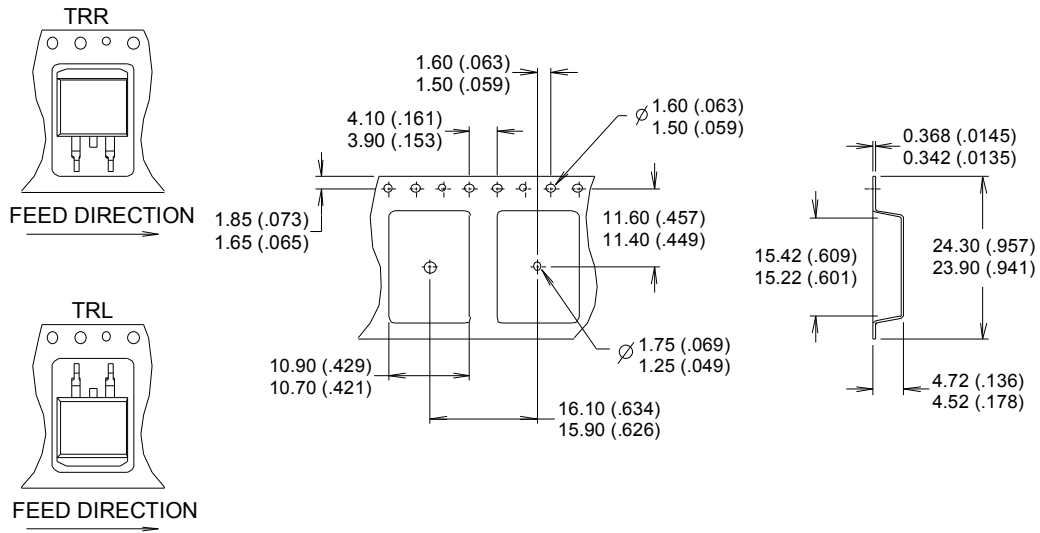
Note: "P" in assembly line position indicates "Lead - Free"



OR



Note: For the most current drawing please refer to Infineon's web site [www.infineon.com](http://www.infineon.com)

**D2-Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))**

**NOTES :**

1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION MEASURED @ HUB.
4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to Infineon's web site [www.infineon.com](http://www.infineon.com)

**Qualification Information†**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) ††	
<b>Moisture Sensitivity Level</b>	D2-Pak	MSL1 (per JEDEC J-STD-020D) ††
	TO-262	N/A
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at Infineon’s web site [www.infineon.com](http://www.infineon.com)

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
5/27/2016	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template.</li> <li>Added disclaimer on last page.</li> <li>TO-262 package was removed from ordering information since it is EOL on page 1.</li> </ul>

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Trademarks updated November 2015

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