

OptiMOS®-T2 Power-Transistor

Product Summary

| | | |
|--------------------------------|-----|------------|
| V_{DS} | 40 | V |
| $R_{DS(on),max}$ (SMD version) | 4.2 | m Ω |
| I_D | 80 | A |

Features

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

PG-TO263-3-2 PG-TO262-3-1 PG-TO220-3-1



| Type | Package | Marking |
|---------------|--------------|---------|
| IPB80N04S4-04 | PG-TO263-3-2 | 4N0404 |
| IPI80N04S4-04 | PG-TO262-3-1 | 4N0404 |
| IPP80N04S4-04 | PG-TO220-3-1 | 4N0404 |


Maximum ratings, at $T_j=25^\circ\text{C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|----------------|--|--------------|------------------|
| Continuous drain current ¹⁾ | I_D | $T_C=25^\circ\text{C}$, $V_{GS}=10\text{V}$ | 80 | A |
| | | $T_C=100^\circ\text{C}$, $V_{GS}=10\text{V}^{2)}$ | 80 | |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | $T_C=25^\circ\text{C}$ | 320 | |
| Avalanche energy, single pulse ²⁾ | E_{AS} | $I_D=40\text{A}$ | 100 | mJ |
| Avalanche current, single pulse | I_{AS} | - | 80 | A |
| Gate source voltage | V_{GS} | - | ± 20 | V |
| Power dissipation | P_{tot} | $T_C=25^\circ\text{C}$ | 71 | W |
| Operating and storage temperature | T_j, T_{stg} | - | -55 ... +175 | $^\circ\text{C}$ |
| IEC climatic category; DIN IEC 68-1 | - | - | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|--|------------|--|--------|------|------|------|
| | | | min. | typ. | max. | |
| Thermal characteristics²⁾ | | | | | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | - | 2.1 | K/W |
| Thermal resistance, junction - ambient, leaded | R_{thJA} | - | - | - | 62 | |
| SMD version, device on PCB | R_{thJA} | minimal footprint | - | - | 62 | |
| | | 6 cm ² cooling area ³⁾ | - | - | 40 | |

Electrical characteristics, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified
Static characteristics

| | | | | | | |
|----------------------------------|---------------|--|-----|------|-----|------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=1mA$ | 40 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=35\mu A$ | 2.0 | 3.0 | 4.0 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=40V, V_{GS}=0V$ | - | 0.02 | 1 | μA |
| | | $V_{DS}=18V, V_{GS}=0V, T_j=85^\circ C^{2)}$ | - | 1 | 20 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=20V, V_{DS}=0V$ | - | - | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=10V, I_D=80A$ | - | 4.3 | 4.6 | m Ω |
| | | $V_{GS}=10V, I_D=80A, \text{SMD version}$ | - | 3.9 | 4.2 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics²⁾

| | | | | | | |
|------------------------------|--------------|---|---|------|------|----|
| Input capacitance | C_{iss} | $V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$ | - | 2650 | 3440 | pF |
| Output capacitance | C_{oss} | | - | 650 | 840 | |
| Reverse transfer capacitance | C_{rss} | | - | 20 | 46 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=20V, V_{GS}=10V,$ $I_D=80A, R_G=3.5\Omega$ | - | 10 | - | ns |
| Rise time | t_r | | - | 12 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 9 | - | |
| Fall time | t_f | | - | 12 | - | |

Gate Charge Characteristics²⁾

| | | | | | | |
|-----------------------|---------------|---|---|-----|----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=32V, I_D=80A,$ $V_{GS}=0$ to 10V | - | 16 | 20 | nC |
| Gate to drain charge | Q_{gd} | | - | 5 | 12 | |
| Gate charge total | Q_g | | - | 33 | 43 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 5.8 | - | V |

Reverse Diode

| | | | | | | |
|--|---------------|---|---|-----|-----|----|
| Diode continuous forward current ²⁾ | I_S | $T_C=25^\circ C$ | - | - | 80 | A |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | | - | - | 320 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0V, I_F=80A,$ $T_j=25^\circ C$ | - | 0.9 | 1.3 | V |
| Reverse recovery time ²⁾ | t_{rr} | $V_R=20V, I_F=50A,$ $di_F/dt=100A/\mu s$ | - | 39 | - | ns |
| Reverse recovery charge ²⁾ | Q_{rr} | | - | 35 | - | nC |

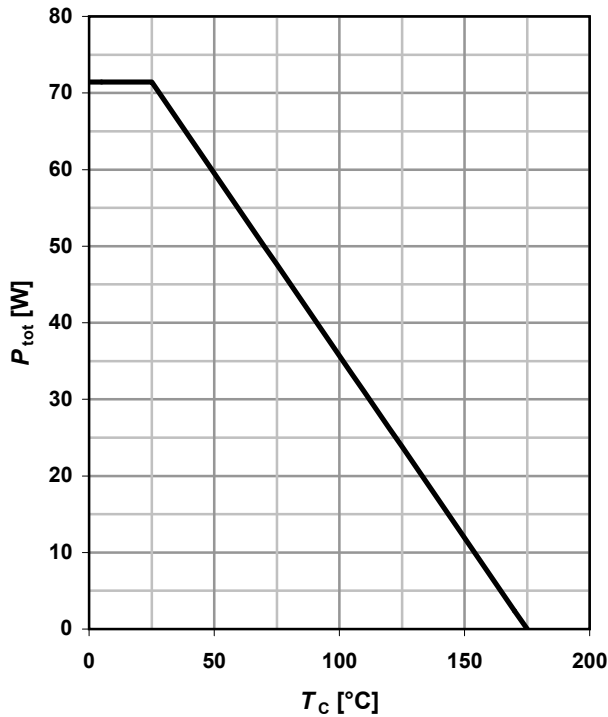
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 2.1K/W$ the chip is able to carry 98A at 25°C.

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

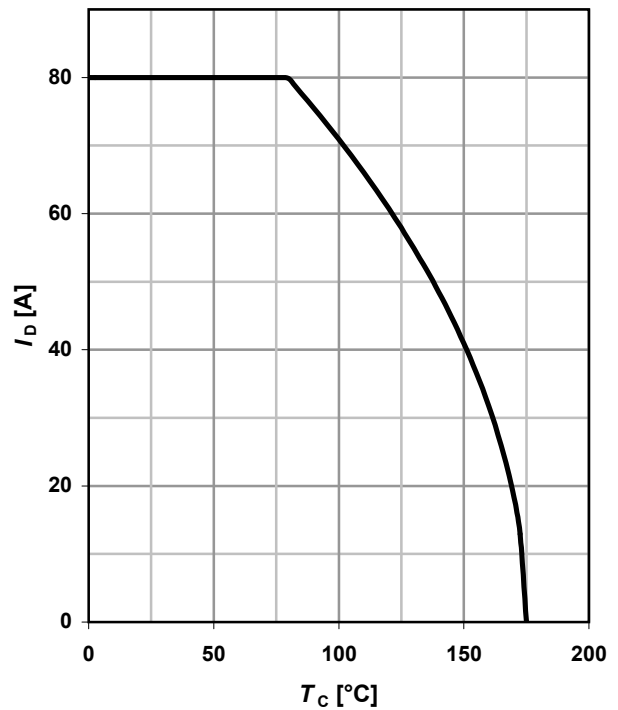
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6\text{ V}$



2 Drain current

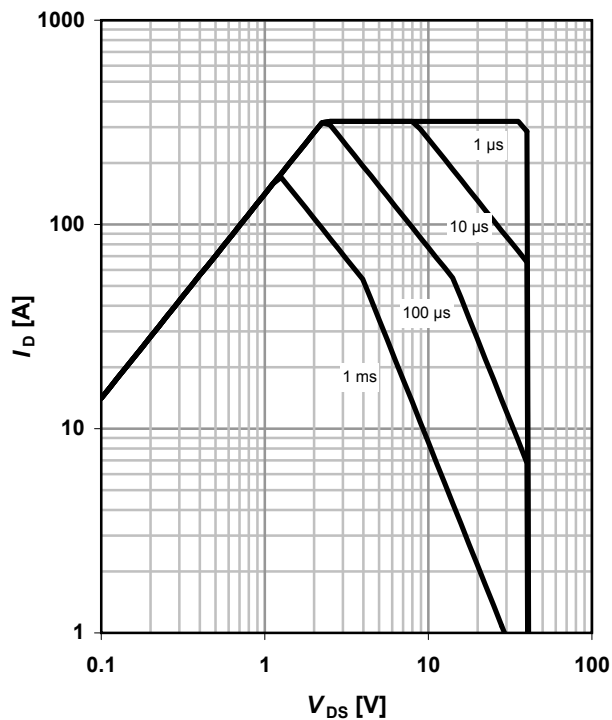
$I_D = f(T_C); V_{GS} \geq 6\text{ V}; \text{SMD}$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0; \text{SMD}$

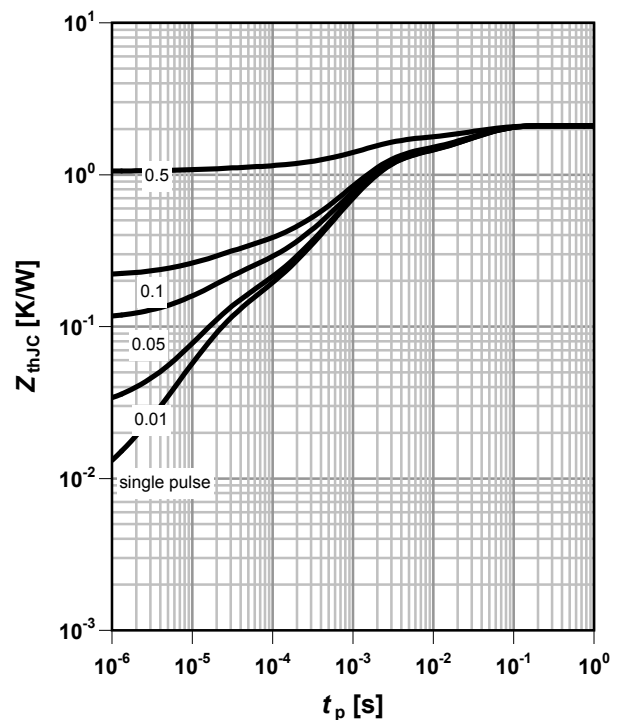
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

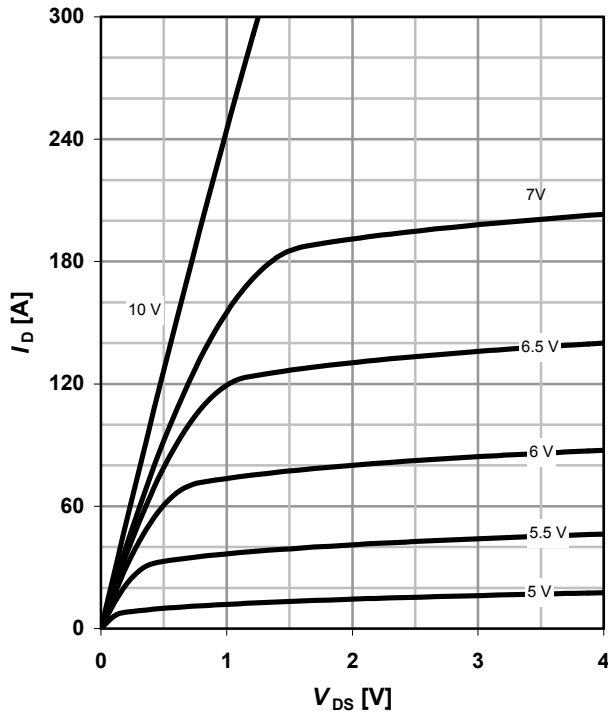
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}; \text{SMD}$

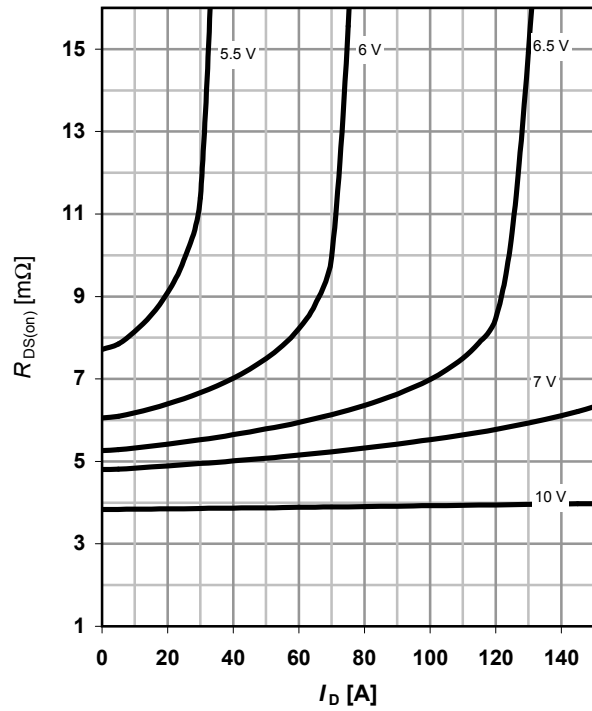
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}; \text{SMD}$

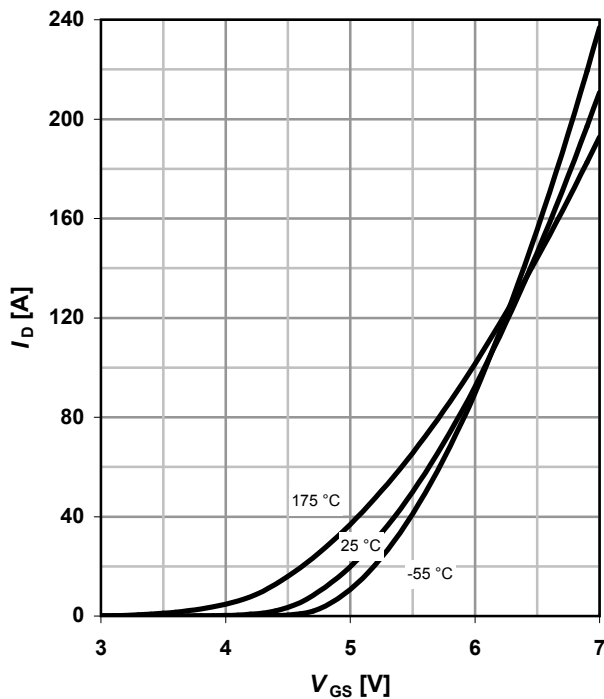
parameter: V_{GS}



7 Typ. transfer characteristics

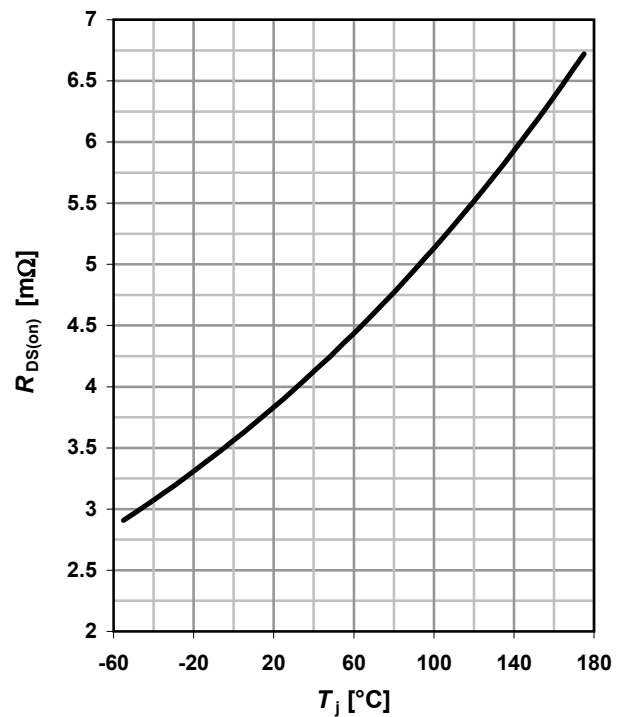
$I_D = f(V_{GS}); V_{DS} = 6\text{V}$

parameter: T_j



8 Typ. drain-source on-state resistance

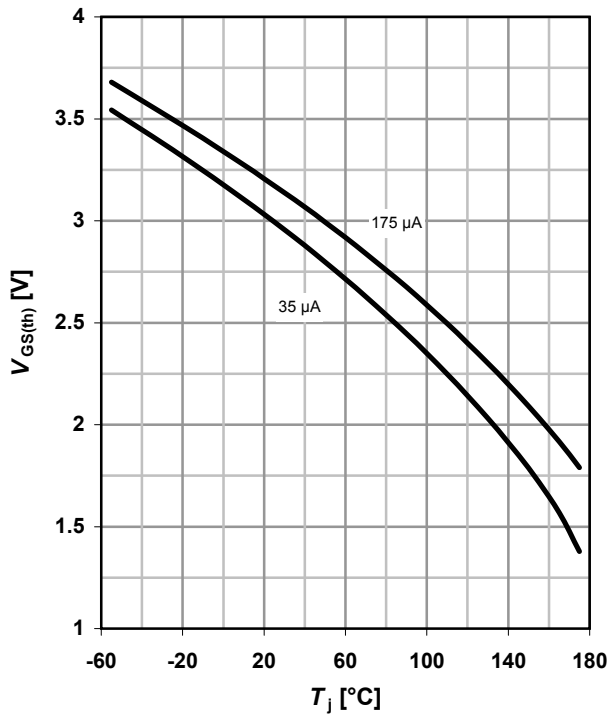
$R_{DS(on)} = f(T_j); I_D = 80\text{ A}; V_{GS} = 10\text{ V}; \text{SMD}$



9 Typ. gate threshold voltage

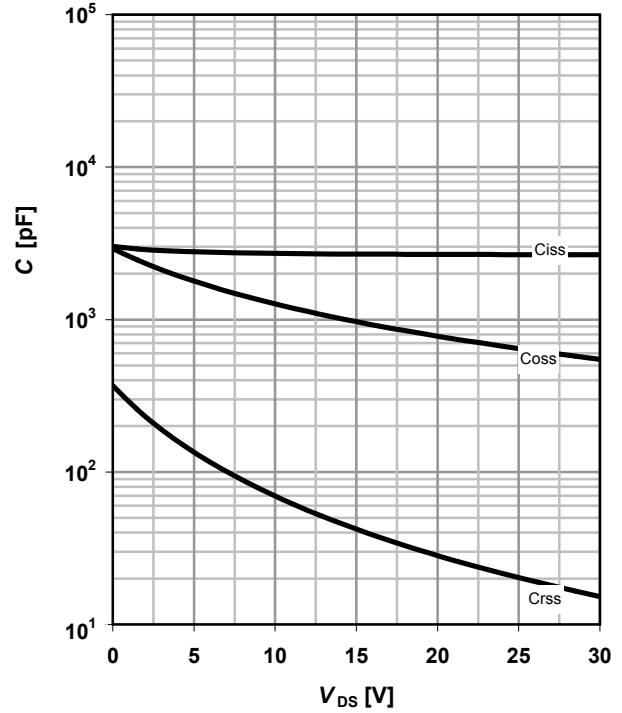
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

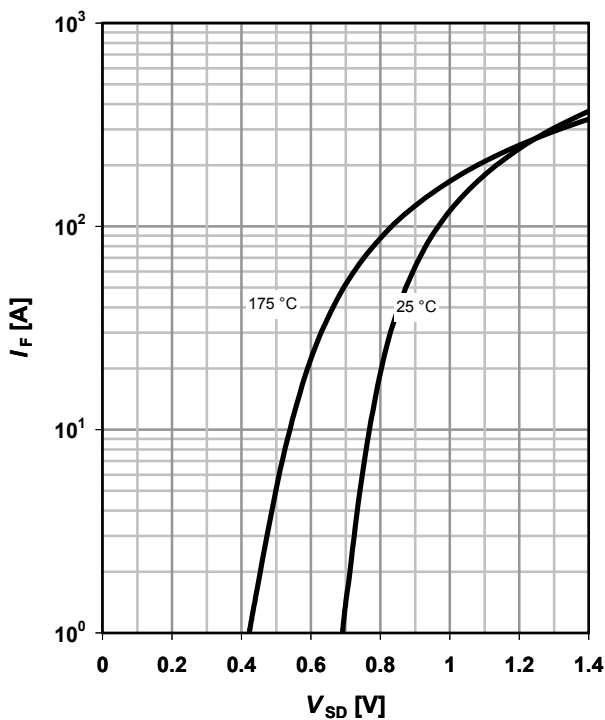
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

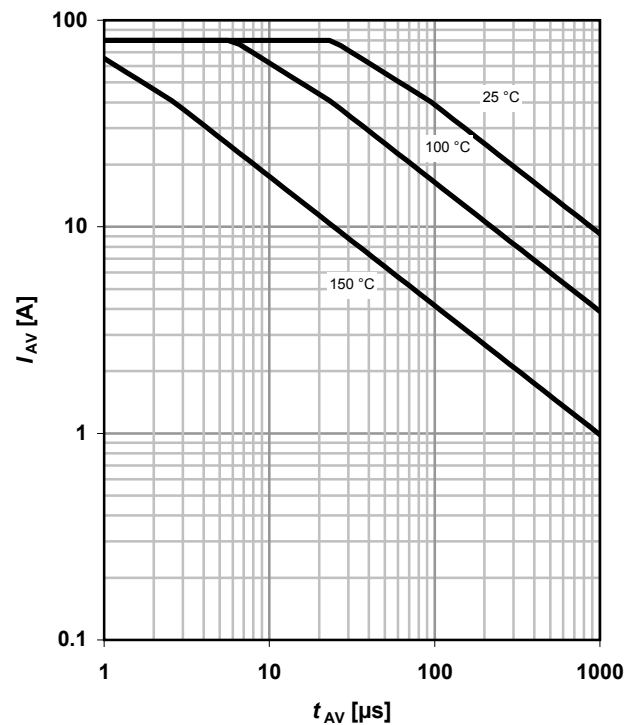
parameter: T_j



12 Avalanche characteristics

$I_{AS} = f(t_{AV})$

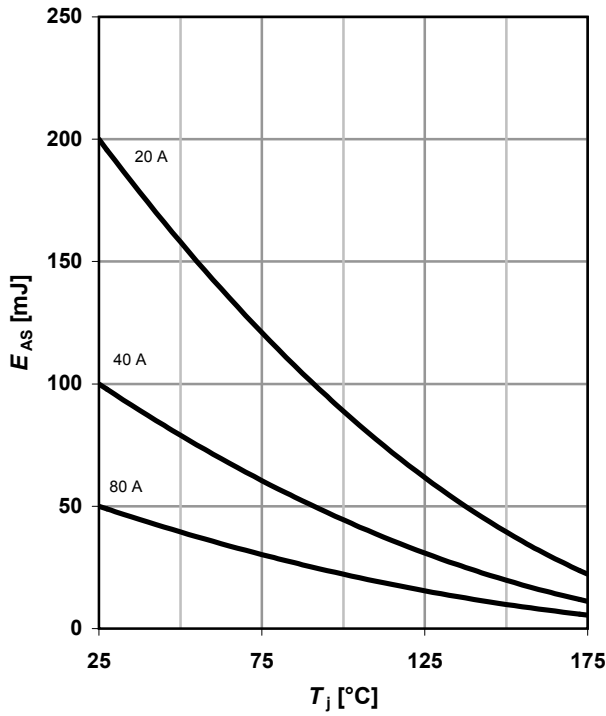
parameter: $T_{j(start)}$



13 Avalanche energy

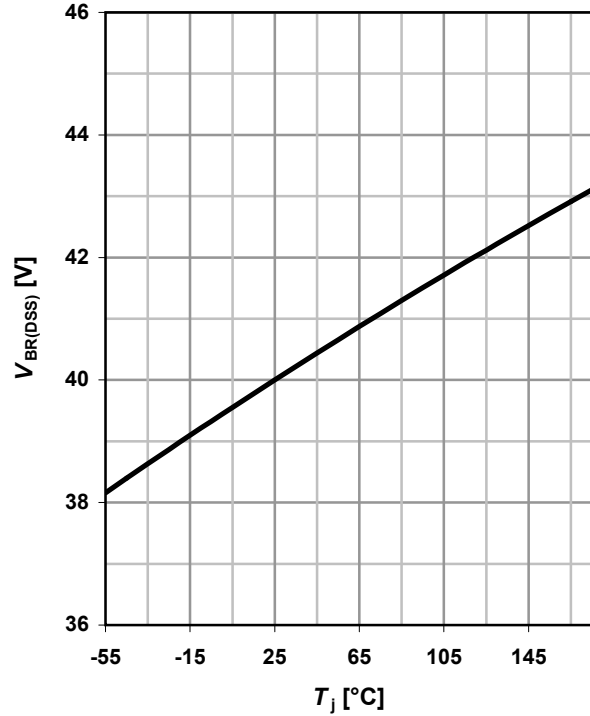
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

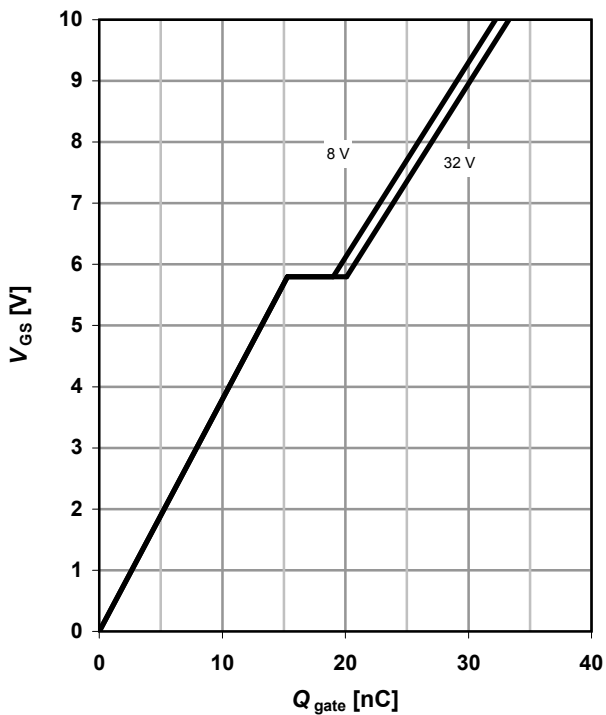
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 80 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

| Version | Date | Changes |
|--------------|------------|------------------|
| Revision 1.0 | 06.04.2010 | Final Data Sheet |
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