

# IRFR2307ZPbF IRFU2307ZPbF

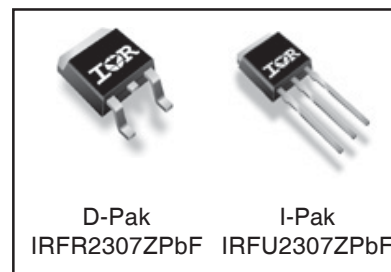
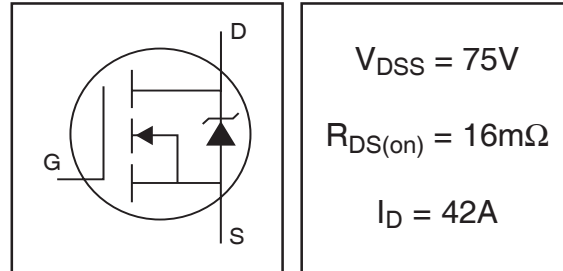
## Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

## Description

This HEXFET<sup>®</sup> Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

## HEXFET<sup>®</sup> Power MOSFET



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	53	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	38	
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Package Limited)	42	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	210	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	110	W
	Linear Derating Factor	0.70	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>②</sup>	100	mJ
$E_{AS}$ (Tested)	Single Pulse Avalanche Energy Tested Value <sup>③</sup>	140	
$I_{AR}$	Avalanche Current <sup>①</sup>	See Fig.12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy <sup>③</sup>		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

## Thermal Resistance

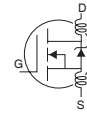
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case <sup>④</sup>	—	1.42	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount) <sup>⑤</sup>	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

HEXFET<sup>®</sup> is a registered trademark of International Rectifier.

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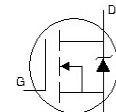
## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	75	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.072	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	12.8	16	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 32A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
g <sub>fs</sub>	Forward Transconductance	30	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 32A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge	—	50	75		I <sub>D</sub> = 32A
Q <sub>gs</sub>	Gate-to-Source Charge	—	14	—	nC	V <sub>DS</sub> = 60V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	19	—		V <sub>GS</sub> = 10V ③
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—		V <sub>DD</sub> = 38V
t <sub>r</sub>	Rise Time	—	65	—		I <sub>D</sub> = 32A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	44	—	ns	R <sub>G</sub> = 10 Ω
t <sub>f</sub>	Fall Time	—	29	—		V <sub>GS</sub> = 10V ③
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	2190	—		V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	280	—	pF	V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	150	—		f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	1070	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	190	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 60V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance	—	400	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V ④



## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	42	A	MOSFET symbol showing the integral reverse
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	210		p-n junction diode.
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 32A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	31	47	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 32A, V <sub>DD</sub> = 38V
Q <sub>rr</sub>	Reverse Recovery Charge	—	31	47	nC	di/dt = 100A/μs ③
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



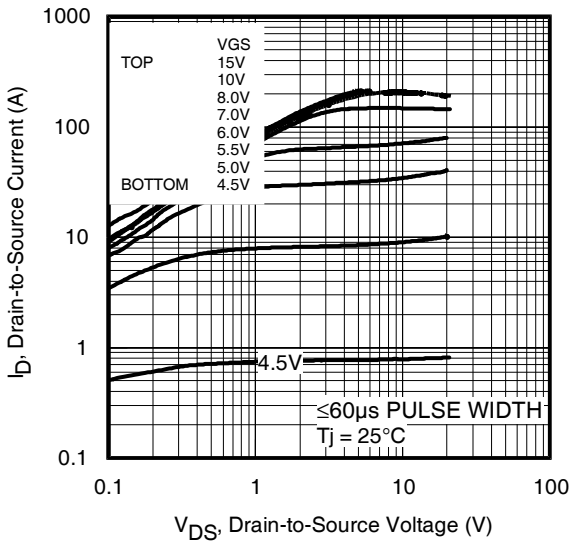


Fig 1. Typical Output Characteristics

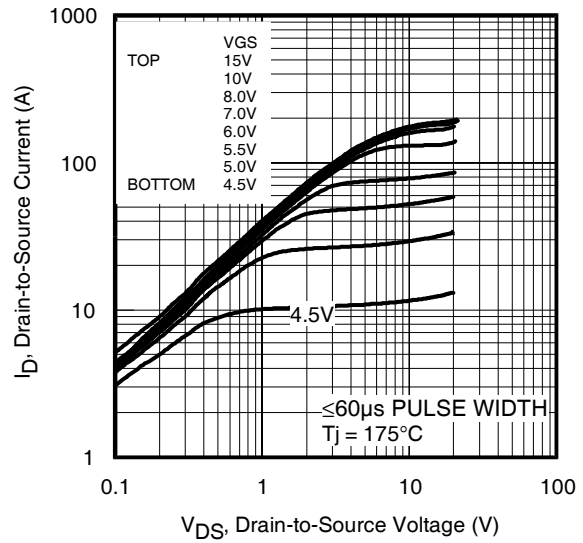


Fig 2. Typical Output Characteristics

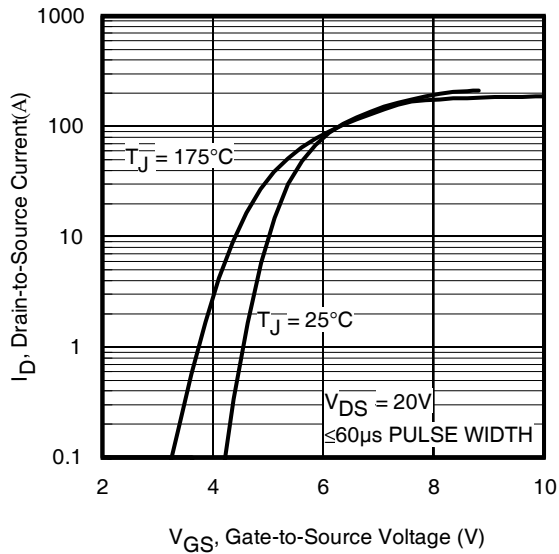


Fig 3. Typical Transfer Characteristics

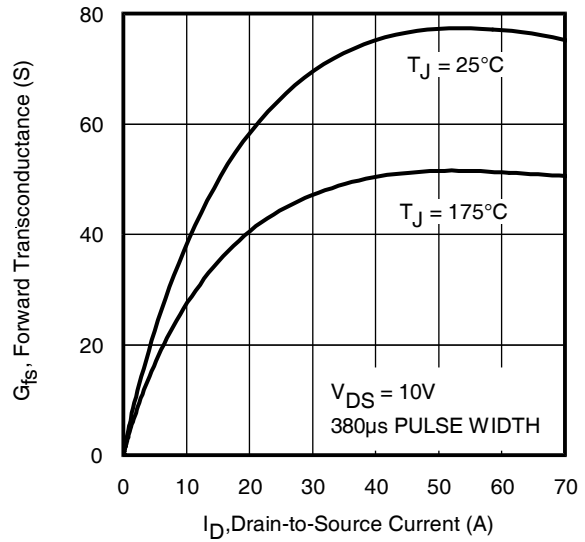
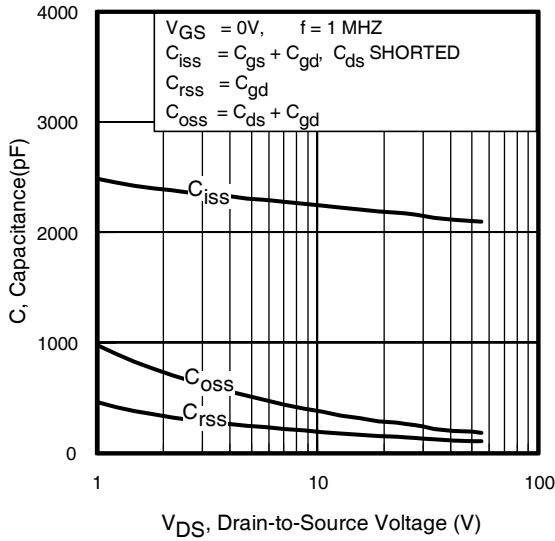
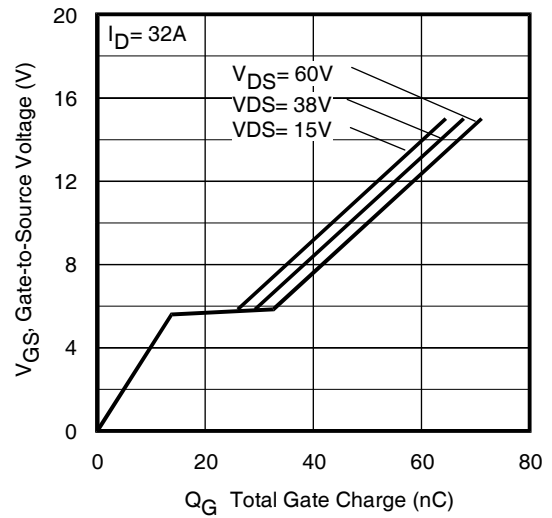


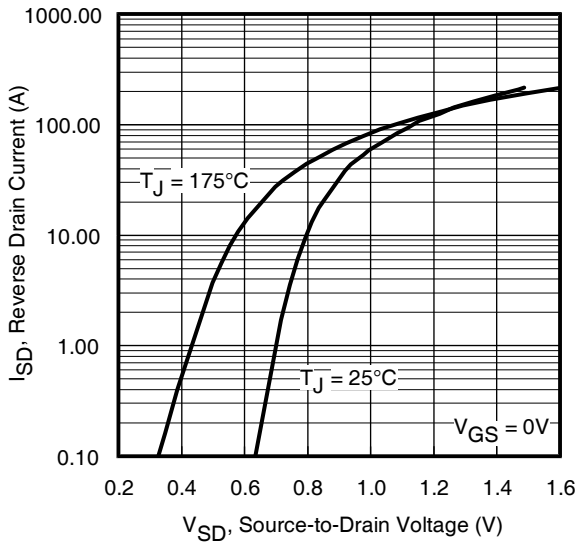
Fig 4. Typical Forward Transconductance vs. Drain Current



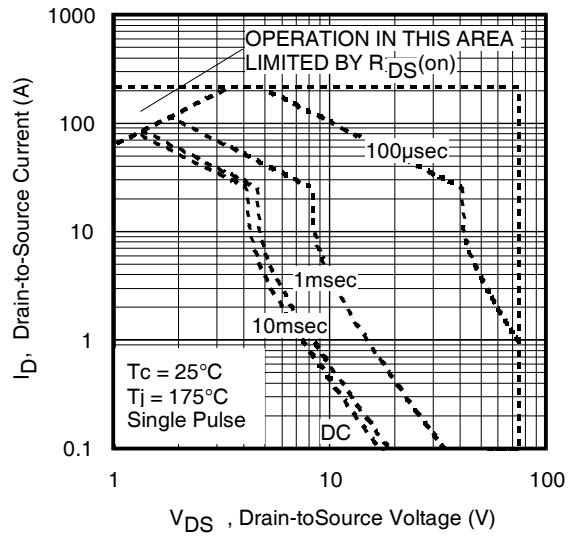
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



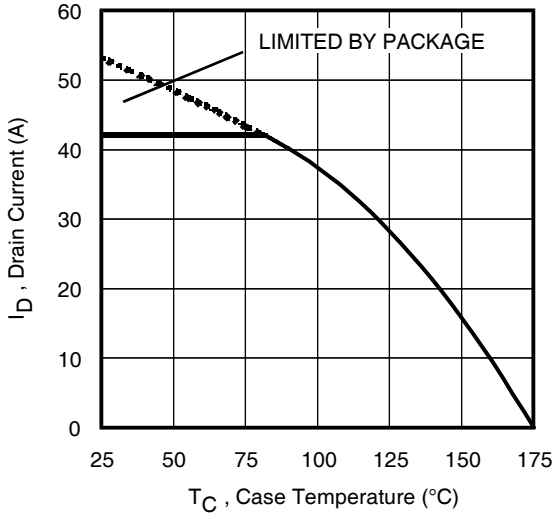
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage



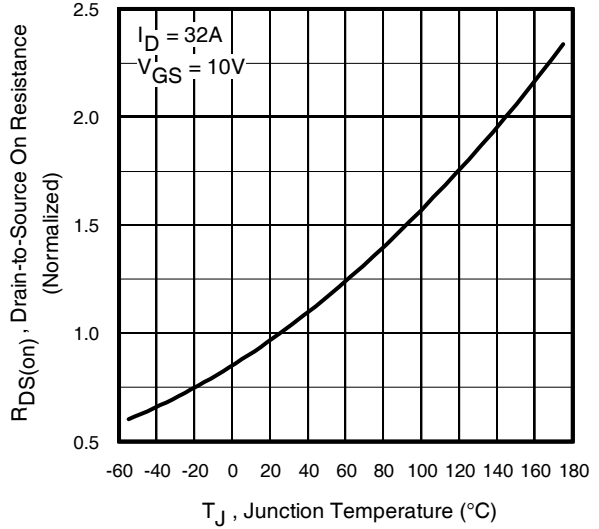
**Fig 7.** Typical Source-Drain Diode Forward Voltage



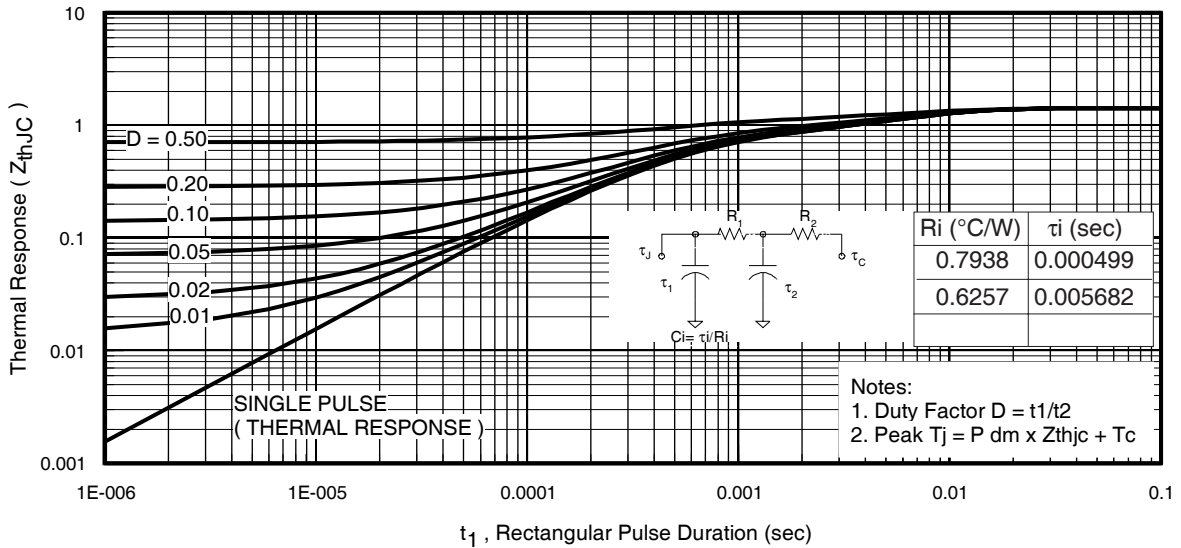
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Normalized On-Resistance vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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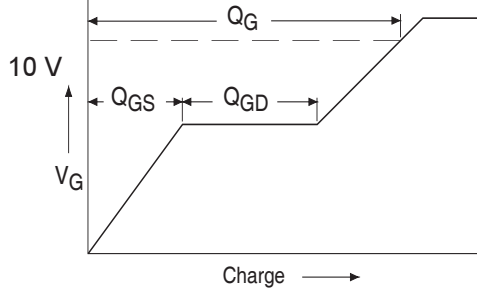
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**Fig 12a.** Unclamped Inductive Test Circuit



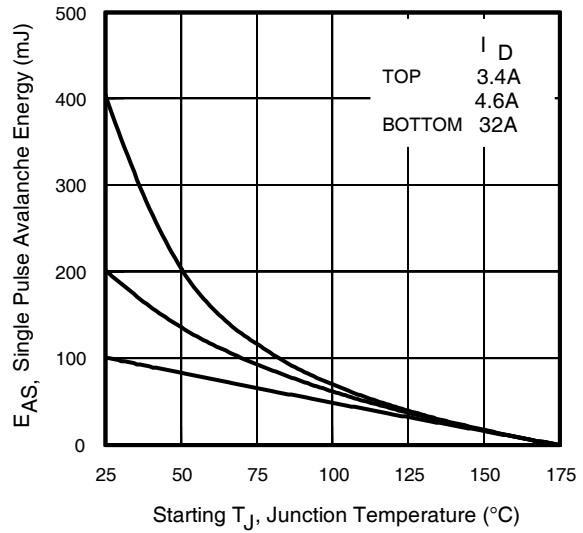
**Fig 12b.** Unclamped Inductive Waveforms



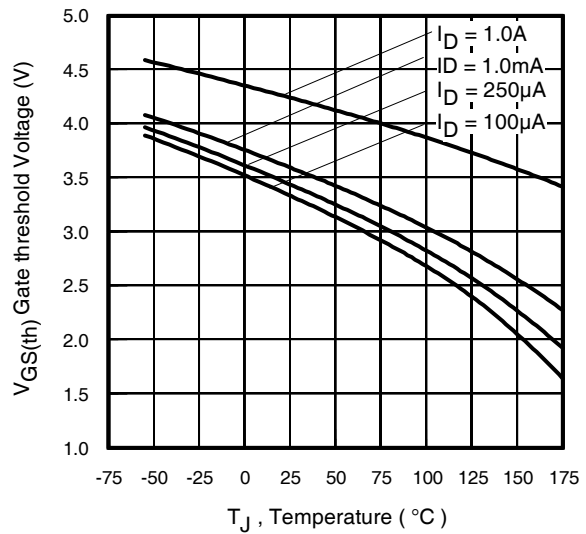
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



**Fig 14.** Threshold Voltage vs. Temperature

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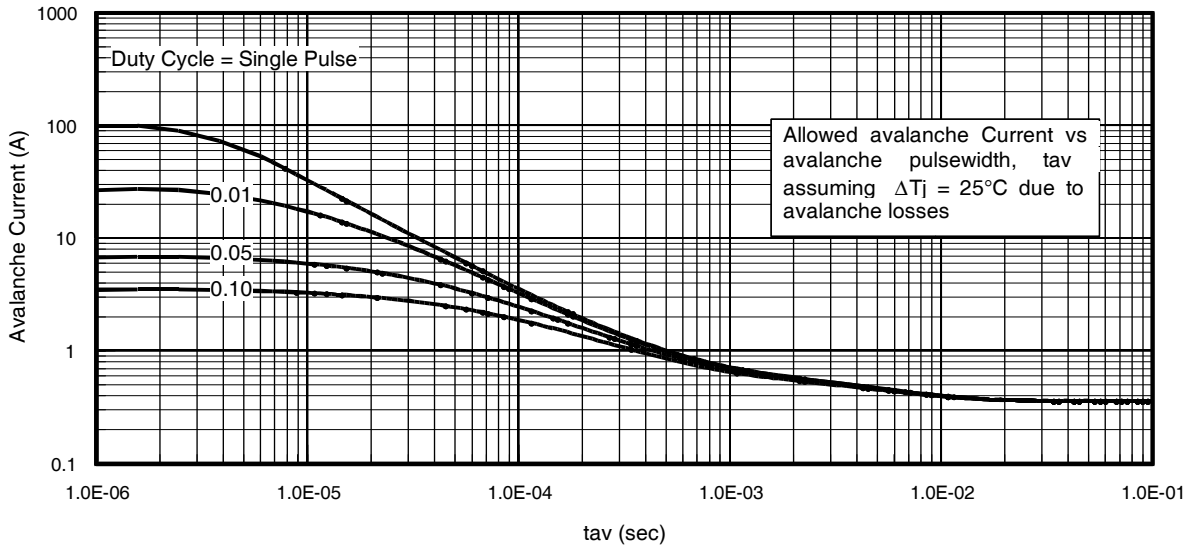


Fig 15. Typical Avalanche Current vs.Pulsewidth

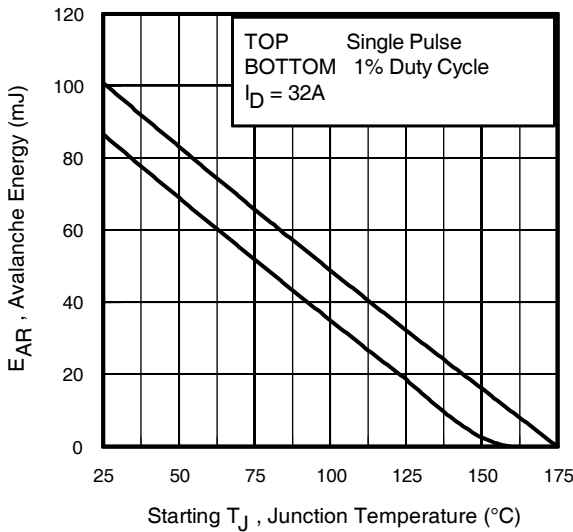


Fig 16. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



**Fig 18a. Switching Time Test Circuit**

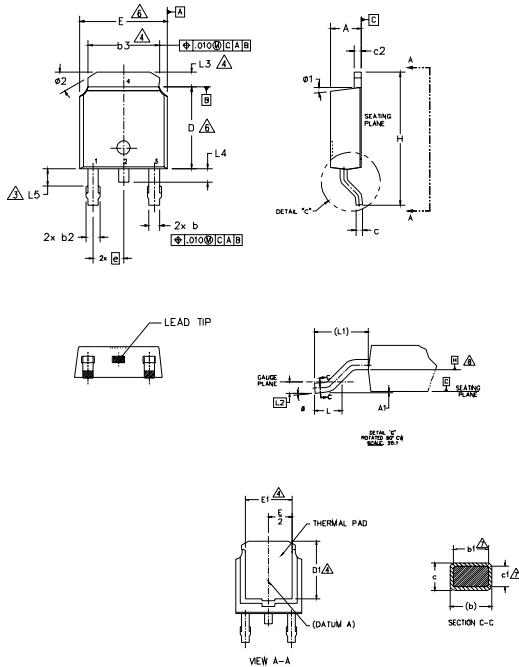


**Fig 18b. Switching Time Waveforms**



## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
  - 3.- LEAD DIMENSION UNCONTROLLED IN L5.
  - 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
  - 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
  - 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  - 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	1.02		.040		
L5	1.14	1.52	.045	.060	3
phi	0°	10°	0°	10°	
phi1	0°	15°	0°	15°	
phi2	25°	35°	25°	35°	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBT & CoPAK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

## D-Pak (TO-252AA) Part Marking Information

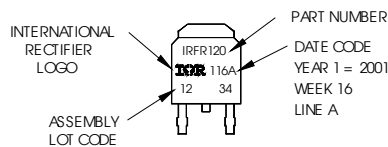
EXAMPLE: THIS IS AN IRFR120 WITH ASSEMBLY LOT CODE 1234 ASSEMBLED ON WW 16, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"  
"P" in assembly line position indicates "Lead-Free" qualification to the consumer-level



INTERNATIONAL RECTIFIER LOGO

ASSEMBLY LOT CODE



PART NUMBER

DATE CODE  
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)

P̄ = DESIGNATES LEAD-FREE PRODUCT QUALIFIED TO THE CONSUMER LEVEL (OPTIONAL)

YEAR 1 = 2001  
WEEK 16

A = ASSEMBLY SITE CODE

**Notes:**

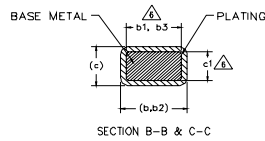
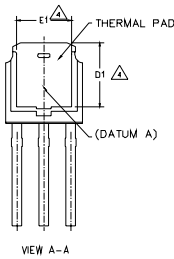
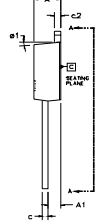
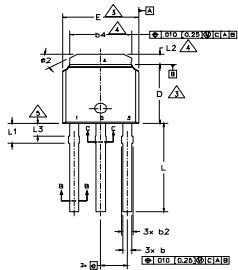
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# IRFR/U2307ZPbF



## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
  - △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - △- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
  - △- LEAD DIMENSION UNCONTROLLED IN L3.
  - △- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
  - 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
  - 8.- CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	0.89	1.14	.035	.045	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	6
b2	0.76	1.14	.030	.045	
b3	0.76	1.04	.030	.041	6
b4	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	6
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	3
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	3
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
L	8.89	9.65	.350	.380	
L1	1.91	2.29	.045	.090	
L2	0.89	1.27	.035	.050	4
L3	1.14	1.52	.045	.060	5
ø1	0"	15"	0"	15"	
ø2	25"	35"	25"	35"	

### LEAD ASSIGNMENTS

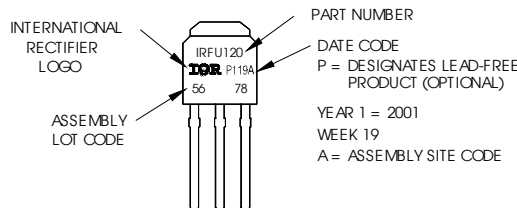
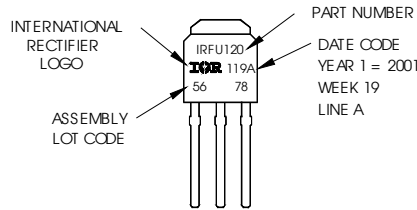
- HEXFET
- 1.- GATE
  - 2.- DRAIN
  - 3.- SOURCE
  - 4.- DRAIN

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates Lead-Free\*

OR

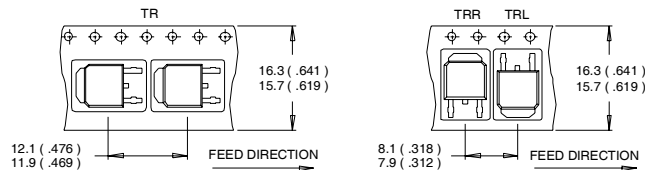


### Notes:

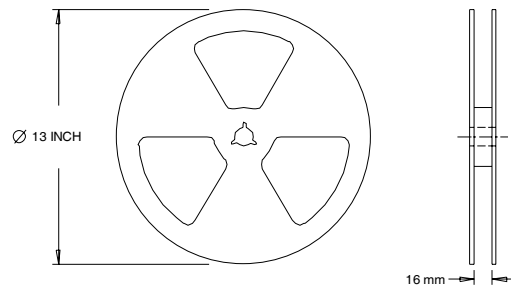
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/autol>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters



- NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
  2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
  3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. OUTLINE CONFORMS TO EIA-481.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.197\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 32\text{A}$ ,  $V_{GS} = 10\text{V}$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0\text{ms}$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑤ Limited by  $T_{Jmax}$ , see Fig. 12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$

Data and specifications subject to change without notice.  
 This product has been designed for the Industrial market.  
 Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
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