

## FDS6875

### Dual P-Channel 2.5V Specified PowerTrench™ MOSFET

#### General Description

These P-Channel 2.5V specified MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for portable electronics applications: load switching and power management, battery charging and protection circuits.

#### Features

- -6 A, -20 V.  $R_{DS(ON)} = 0.030 \Omega @ V_{GS} = -4.5 \text{ V}$ ,  
 $R_{DS(ON)} = 0.040 \Omega @ V_{GS} = -2.5 \text{ V}$ .
- Low gate charge (23nC typical).
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.



SOT-23



SuperSOT™-6



SuperSOT™-8



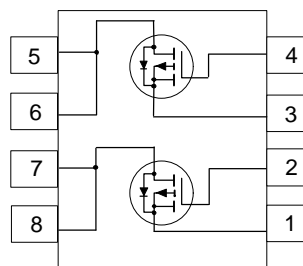
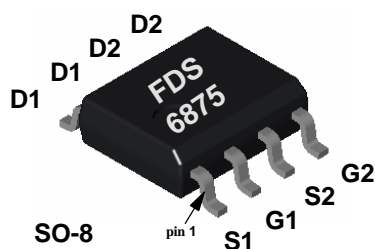
SO-8



SOT-223



SOIC-16



#### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDS6875	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 8$	V
$I_D$	Drain Current - Continuous (Note 1a)	-6	A
	- Pulsed	-20	
$P_D$	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

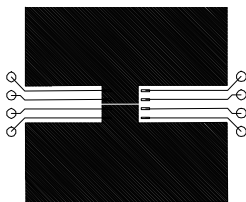
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	$^\circ\text{C}/\text{W}$

**Electrical Characteristics** ( $T_A = 25\text{ }^\circ\text{C}$  unless otherwise noted)

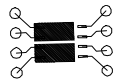
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		-21		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
					-10	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4	-0.8	-1.5	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = 250\text{ }\mu\text{A}$ , Referenced to $25\text{ }^\circ\text{C}$		2.8		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -6\text{ A}$		0.024	0.03	$\Omega$
			$T_J = 125\text{ }^\circ\text{C}$	0.033	0.048	
		$V_{GS} = -2.5\text{ V}, I_D = -5.3\text{ A}$		0.032	0.04	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-20			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -4.5\text{ V}, I_D = -6\text{ A}$		22		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2250		pF
$C_{oss}$	Output Capacitance			500		pF
$C_{rss}$	Reverse Transfer Capacitance			200		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DS} = -10\text{ V}, I_D = -1\text{ A}$ $V_{GEN} = -4.5\text{ V}, R_{GEN} = 6\text{ }\Omega$		8	16	ns
$t_r$	Turn - On Rise Time			15	27	ns
$t_{D(off)}$	Turn - Off Delay Time			98	135	ns
$t_f$	Turn - Off Fall Time			35	55	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -6\text{ A},$ $V_{GS} = -5\text{ V}$		23	31	nC
$Q_{gs}$	Gate-Source Charge			3.9		nC
$Q_{gd}$	Gate-Drain Charge			5.5		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)		-0.7	-1.2	V

Notes:

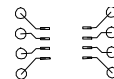
- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $78\text{ }^\circ\text{C/W}$  on a  $0.5\text{ in}^2$  pad of 2oz copper.



b.  $125\text{ }^\circ\text{C/W}$  on a  $0.02\text{ in}^2$  pad of 2oz copper.



c.  $135\text{ }^\circ\text{C/W}$  on a  $0.003\text{ in}^2$  pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

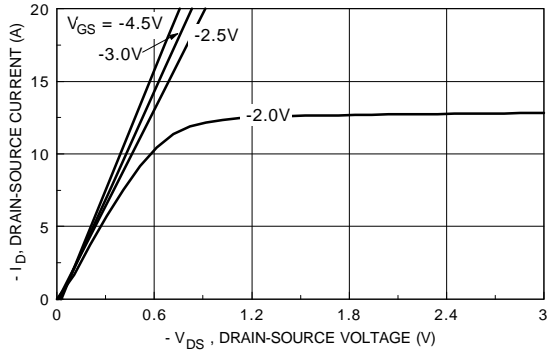


Figure 1. On-Region Characteristics.

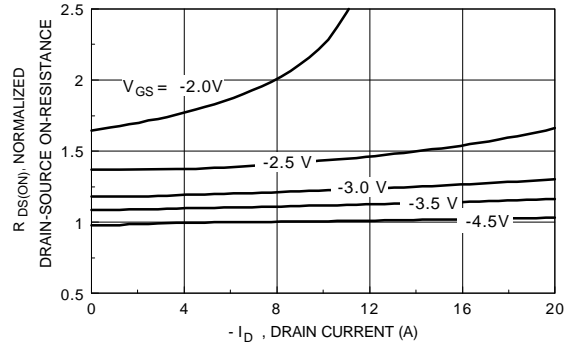


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

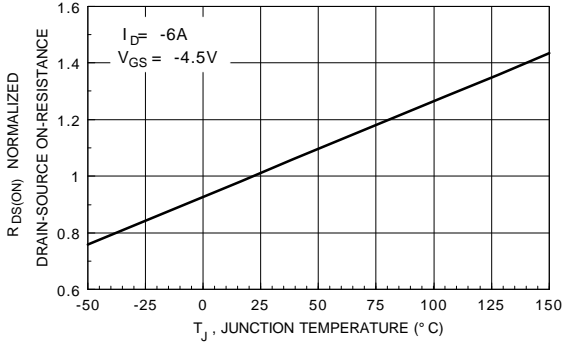


Figure 3. On-Resistance Variation with Temperature.

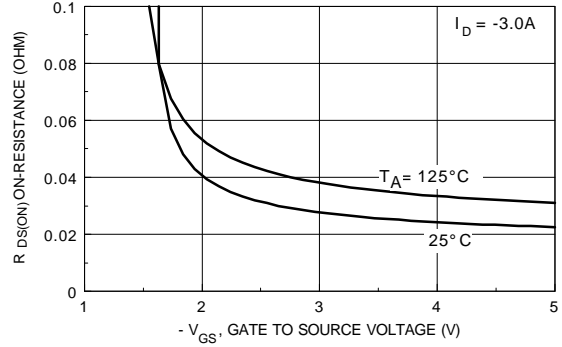


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

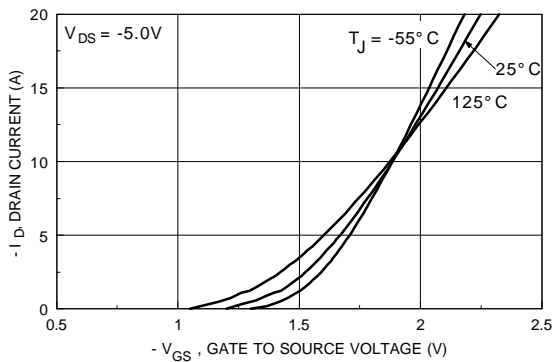


Figure 5. Transfer Characteristics.

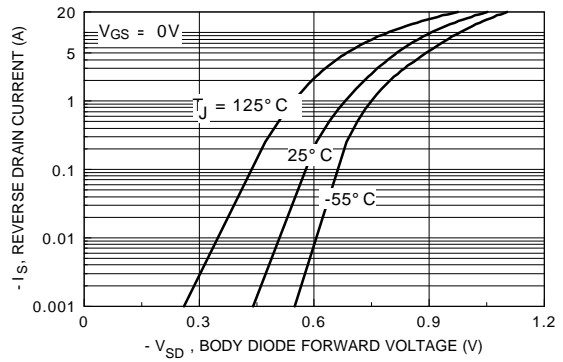
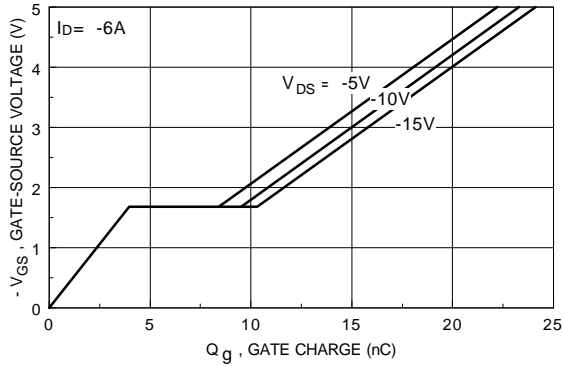
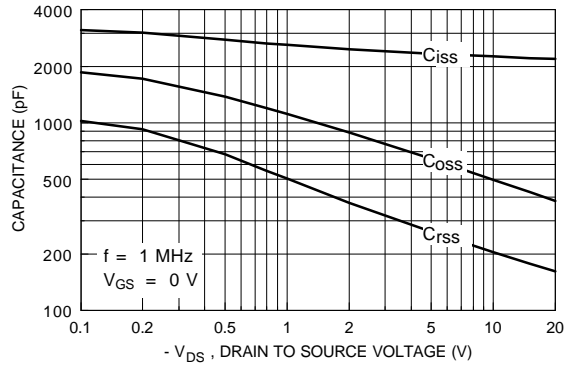


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

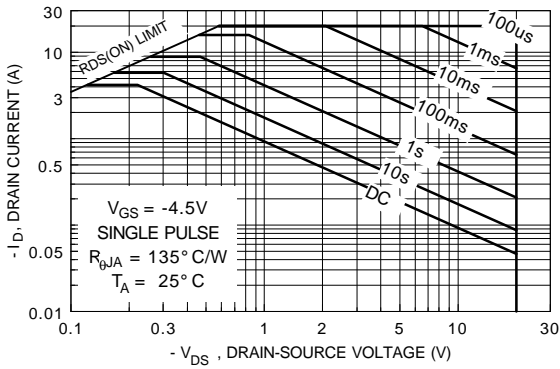
**Typical Electrical Characteristics** (continued)



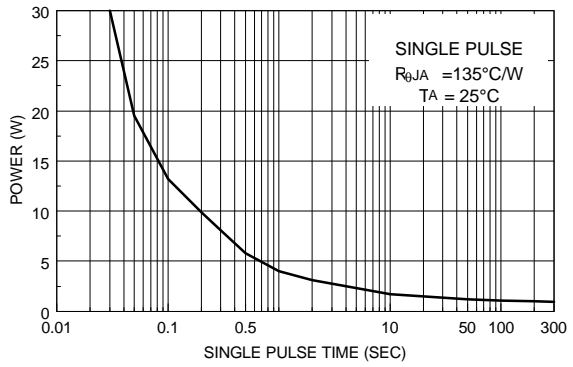
**Figure 7. Gate Charge Characteristics.**



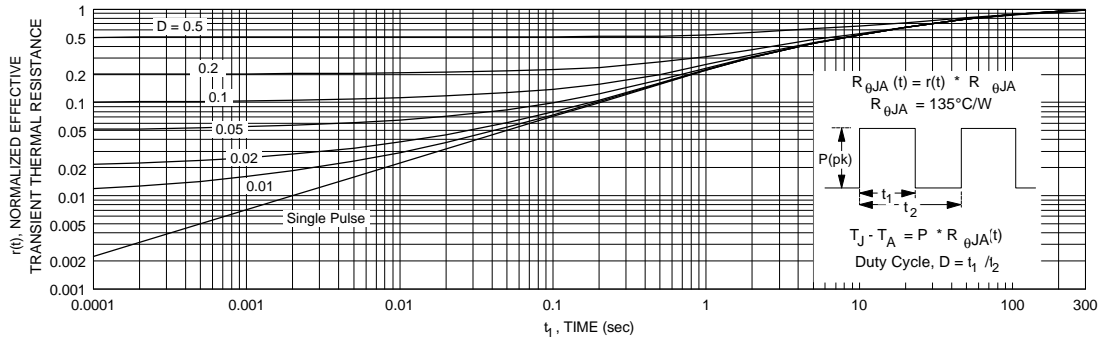
**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

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