



October 2015

FDMA86251

Single N-Channel PowerTrench[®] MOSFET

150 V, 2.4 A, 175 mΩ

Features

- Max $r_{DS(on)}$ = 175 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 2.4\text{ A}$
- Max $r_{DS(on)}$ = 237 mΩ at $V_{GS} = 6\text{ V}$, $I_D = 2.0\text{ A}$
- Low Profile - 0.8 mm maximum in the new package MicroFET 2x2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

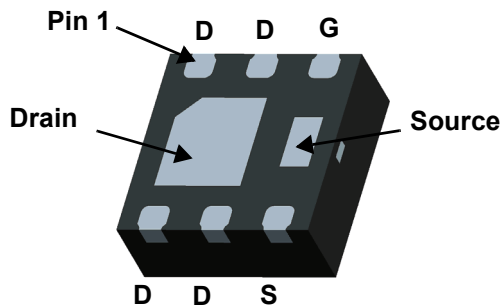


General Description

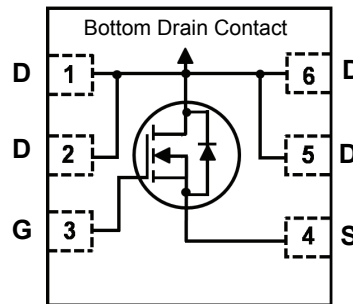
This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $r_{DS(on)}$ and gate charge provide excellent switching performance.

Applications

- DC – DC Primary Switch
- Load Switch



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Rated	Units
V_{DS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous $T_A = 25\text{ °C}$ (Note 1a)	2.4	A
	-Pulsed (Note 4)	12	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	13	mJ
P_D	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.4	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	145	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
251	FDMA86251	MicroFET 2X2	7"	8 mm	3000 units

FDMA86251 Single N-Channel PowerTrench[®] MOSFET

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		108		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.0	2.8	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 2.4\text{ A}$		148	175	m Ω
		$V_{GS} = 6\text{ V}, I_D = 2.0\text{ A}$		175	237	
		$V_{GS} = 10\text{ V}, I_D = 2.4\text{ A}, T_J = 125\text{ }^\circ\text{C}$		272	333	
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{ V}, I_D = 2.4\text{ A}$		4.7		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		259	363	pF
C_{oss}	Output Capacitance			24	34	pF
C_{rss}	Reverse Transfer Capacitance			1.5	2.4	pF
R_g	Gate Resistance		0.1	1.5	3.0	Ω

Switching Characteristics

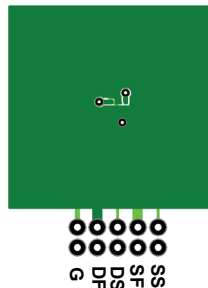
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\text{ V}, I_D = 2.4\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		5.9	12	ns
t_r	Rise Time			1.7	10	ns
$t_{d(off)}$	Turn-Off Delay Time			10	20	ns
t_f	Fall Time			2.3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$	$V_{DD} = 75\text{ V}, I_D = 2.4\text{ A}$	4.1	5.8	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }6\text{ V}$		2.7	3.8	nC
Q_{gs}	Gate to Source Charge			1.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.0		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.4\text{ A}$ (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 2.4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		49	79	ns
Q_{rr}	Reverse Recovery Charge			38	61	nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 52 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. 145 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2: Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3: E_{AS} of 13 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 3\text{ A}$, $V_{DD} = 150\text{ V}$, $V_{GS} = 10\text{ V}$. 100% tested at $L = 0.3\text{ mH}$, $I_{AS} = 8\text{ A}$.

4: Pulsed I_D please refer to Fig 9 SOA graph for more details.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

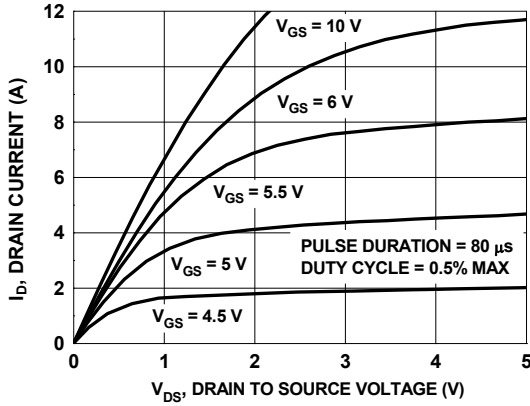


Figure 1. On Region Characteristics

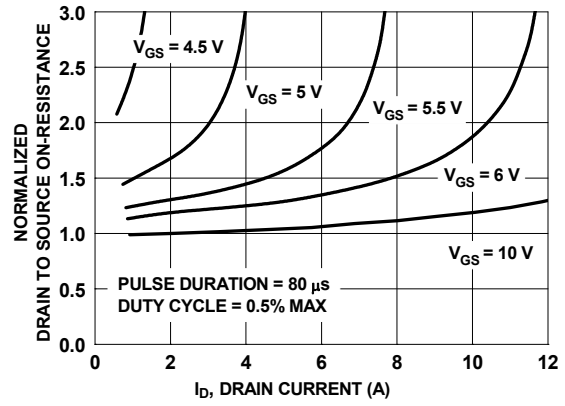


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

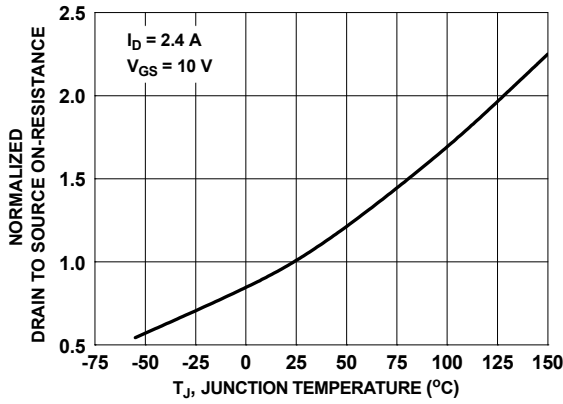


Figure 3. Normalized On Resistance vs. Junction Temperature

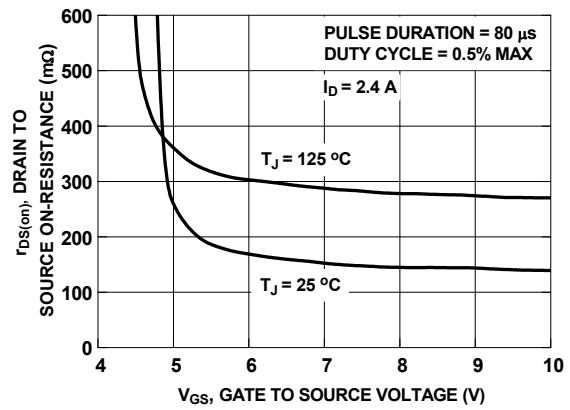


Figure 4. On-Resistance vs. Gate to Source Voltage

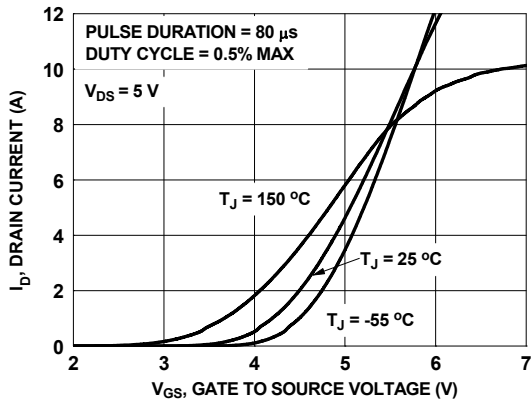


Figure 5. Transfer Characteristics

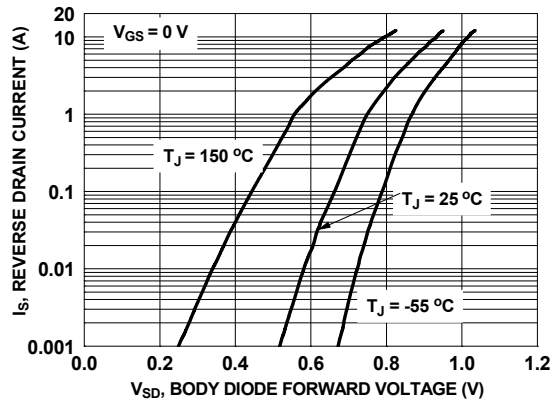


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

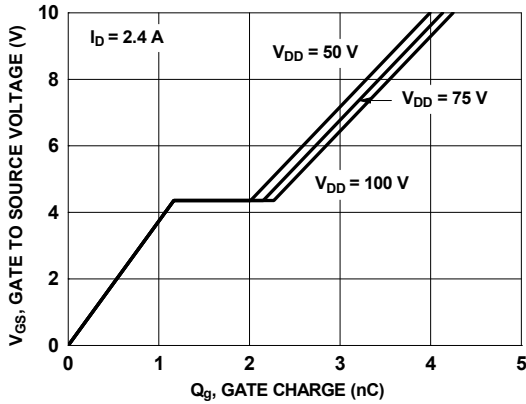


Figure 7. Gate Charge Characteristics

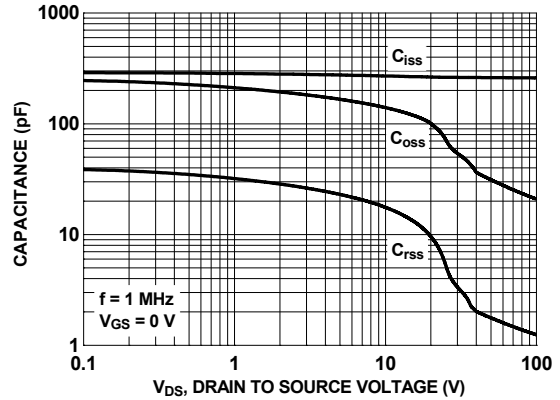


Figure 8. Capacitance vs. Drain to Source Voltage

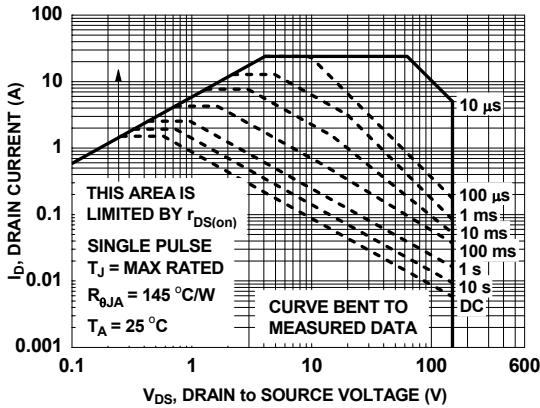


Figure 9. Forward Bias Safe Operating Area

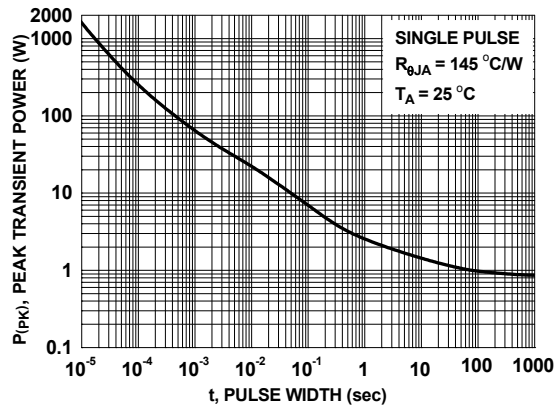


Figure 10. Single Pulse Maximum Power Dissipation

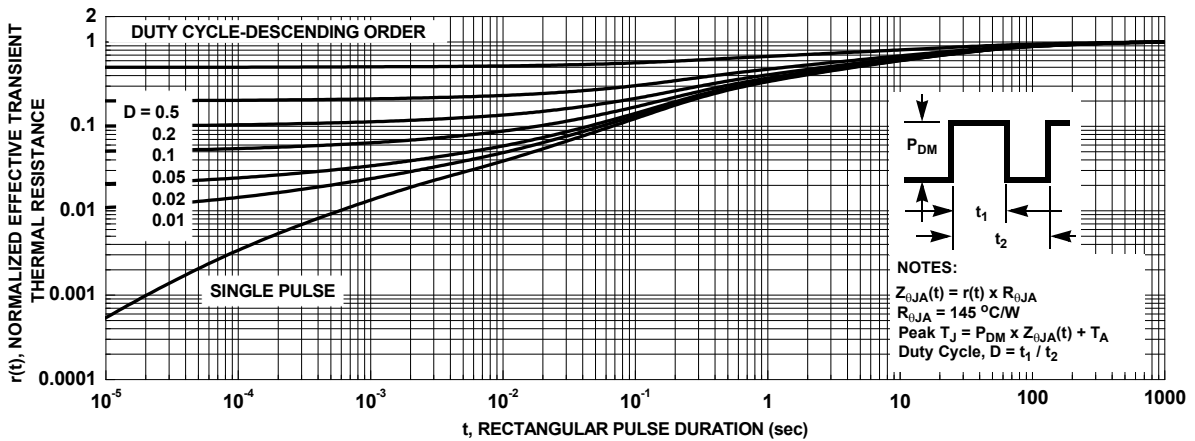
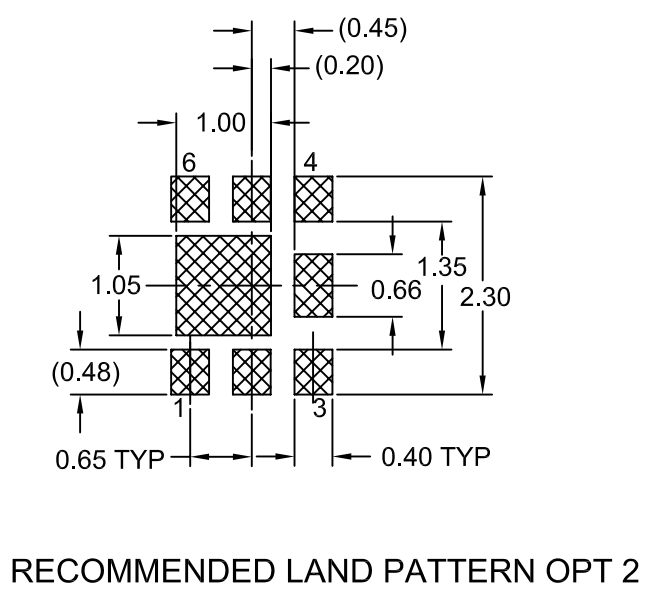
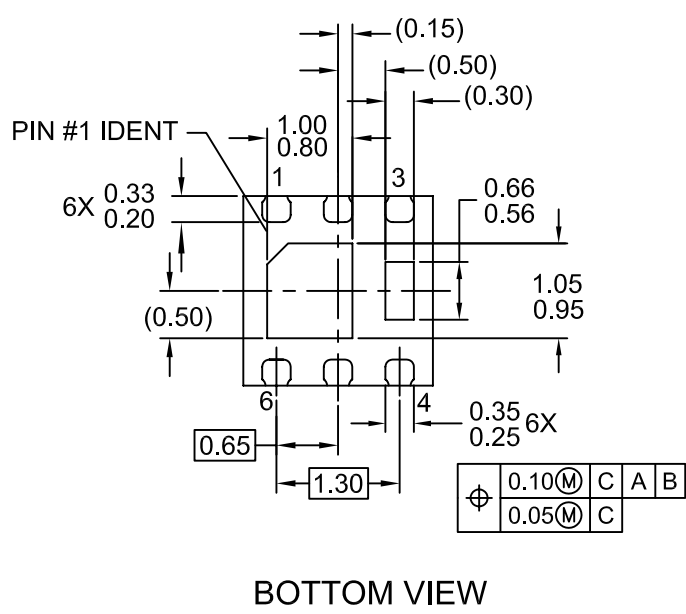
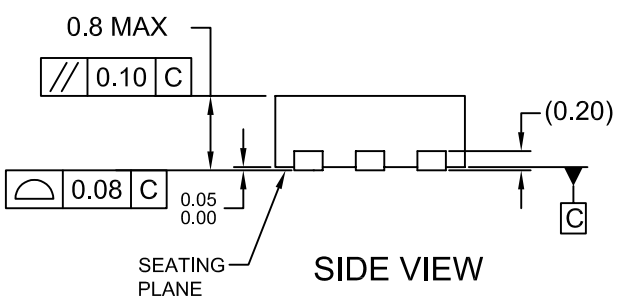
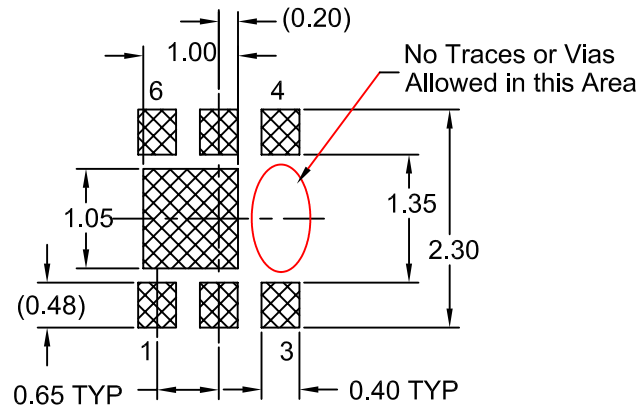
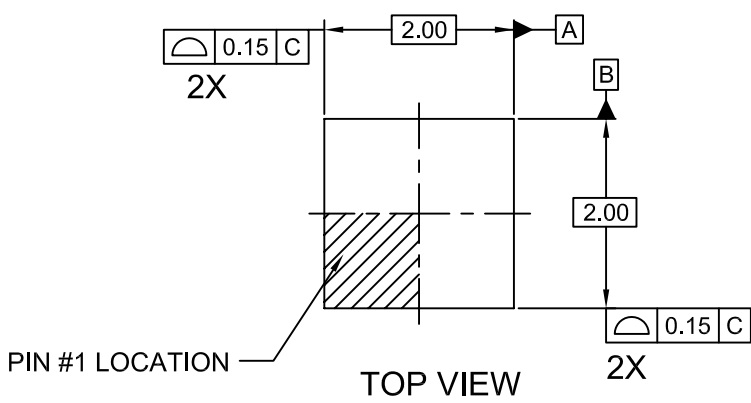


Figure 11. Junction-to-Ambient Transient Thermal Response Curve



NOTES:

- A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-229 DATED AUG/2003
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
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