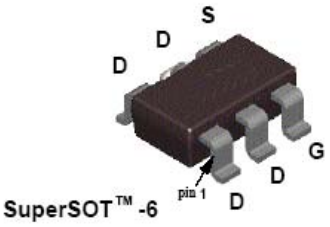
April 2016

FDC642P_F085

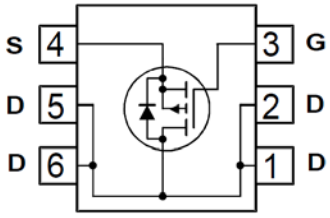
P-Channel PowerTrench® MOSFET
-20V, -4A, 100mΩ

Features

- Typ $R_{DS(on)}$ = 52.5mΩ at V_{GS} = -4.5V, I_D = -4A
- Typ $R_{DS(on)}$ = 75.3mΩ at V_{GS} = -2.5V, I_D = -3.2A
- Fast switching speed
- Low gate charge(6.9nC typical)
- High performance trench technology for extremely low $R_{DS(on)}$
- SuperSOT™-6 package:small foot-print(72% smaller than standard SO-8);low profile(1mm thick).
- RoHS Compliant
- Qualified to AEC Q101



SuperSOT™ -6



Applications

- Load switch
- Battery protection
- Power management

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current Continuous (V_{GS} = 4.5V)	-4	A
	Pulsed	-20	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	72	mJ
P_D	Power Dissipation	1.2	W
T_J, T_{STG}	Operating and Storage Temperature	-55 to +150	°C
$R_{\theta JC}$	Thermal Resistance Junction to Case	30	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, 1in² copper pad area	103	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDC642P	FDC642P_F085	SSOT-6	7”	8mm	3000 units

Notes:
1: Starting T_J = 25°C, L = 14.1mH, I_{AS} = -3.2A
2: A suffix as “…F085P” has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
B_{VDSS}	Drain to Source Breakdown Voltage	I_D = -250μA, V_{GS} = 0V	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16V, V_{GS} = 0V	-	-	-1	μA
		V_{DS} = -16V, V_{GS} = 0V, T_A = 150°C	-	-	-250	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	-0.4	-0.7	-1.5	V
$r_{DS(on)}$	Drain to Source On Resistance	I_D = -4A, V_{GS}= -4.5V	-	52.5	65	mΩ
		I_D = -3.2A, V_{GS}= -2.5V	-	75.3	100	mΩ
		I_D = -4A, V_{GS}= -4.5V, T_J = 125°C	-	72.7	105	mΩ
g_{FS}	Forward Transconductance	I_D = -4A, V_{DD}= -5V	-	10	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -10V, V_{GS} = 0V, f = 1MHz	-	630	-	pF
C_{oss}	Output Capacitance		-	160	-	pF
C_{rss}	Reverse Transfer Capacitance		-	65	-	pF
R_G	Gate Resistance	f = 1MHz	-	4.4	-	Ω
$Q_{g(TOT)}$	Total Gate Charge at -4.5V	V_{GS} = 0 to -4.5V, V_{DD} = -10V, I_D = -4A	-	6.9	9.0	nC
Q_{gs}	Gate to Source Gate Charge		-	1.2	-	nC
Q_{gd}	Gate to Drain “Miller“ Charge		-	1.8	-	nC

Switching Characteristics

t_{on}	Turn-On Time	V_{DD} = -10V, I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6Ω	-	-	23	ns
$t_{d(on)}$	Turn-On Delay Time		-	7.3	-	ns
t_r	Rise Time		-	5.5	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	23.2	-	ns
t_f	Fall Time		-	9.6	-	ns
t_{off}	Turn-Off Time		-	-	53	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	I_{SD} = -1.3A	-	-	-1.25	V
		I_{SD} = -0.65A	-	-	-1.0	V
t_{rr}	Reverse Recovery Time	I_{SD} = -1.3A, dI_{SD}/dt = 100A/μs	-	17	22	ns
Q_{rr}	Reverse Recovery Charge		-	5.6	7.3	nC

Typical Characteristics

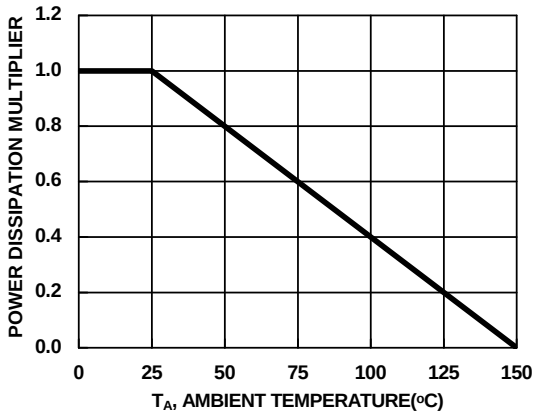


Figure 1. Normalized Power Dissipation vs Ambient Temperature

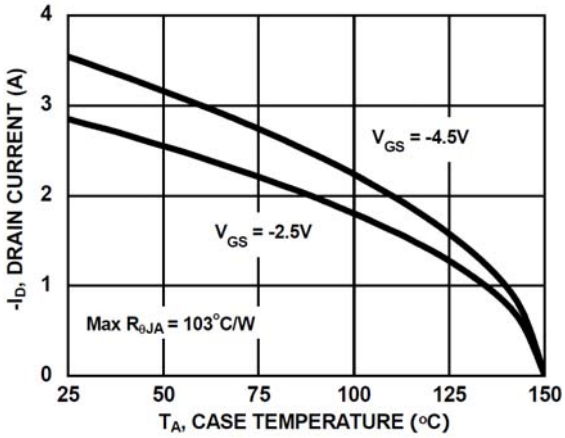


Figure 2. Maximum Continuous Drain Current vs Ambient Temperature

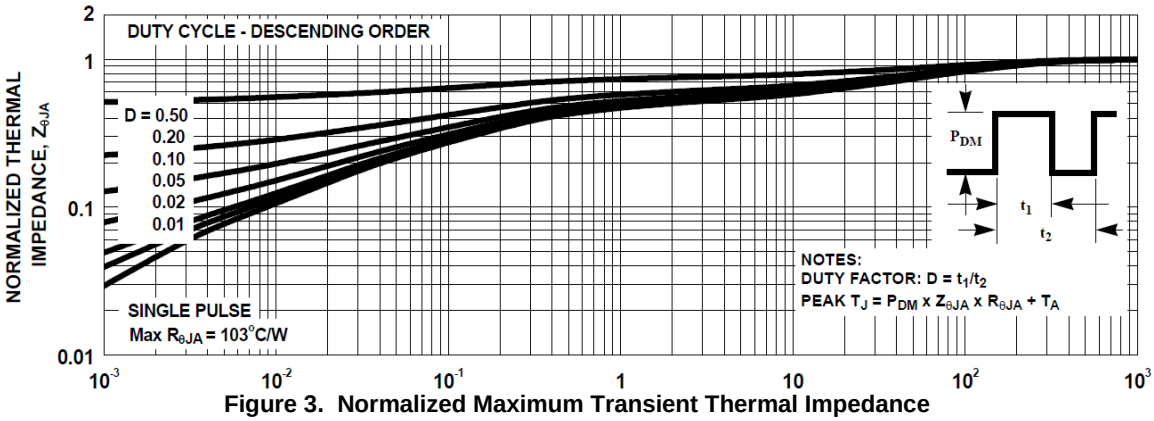


Figure 3. Normalized Maximum Transient Thermal Impedance

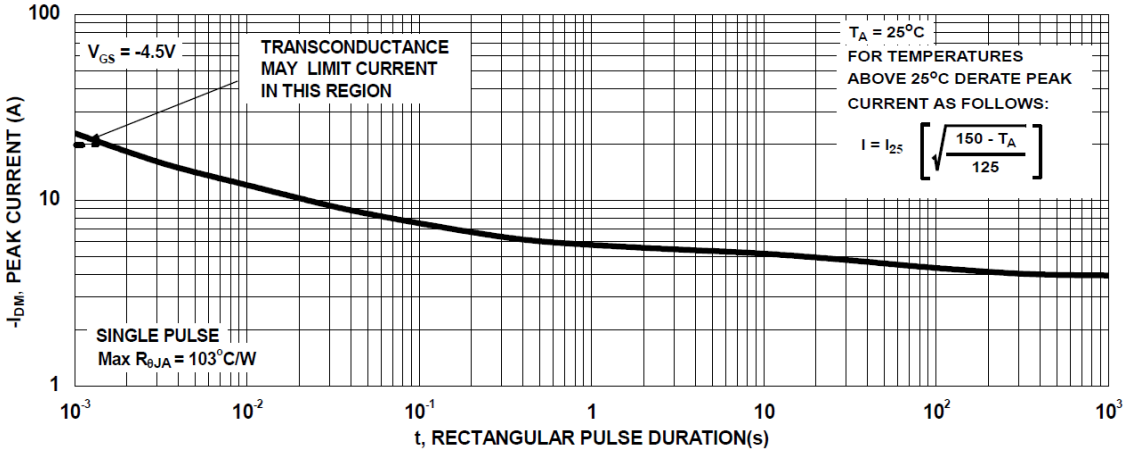


Figure 4. Peak Current Capability

Typical Characteristics

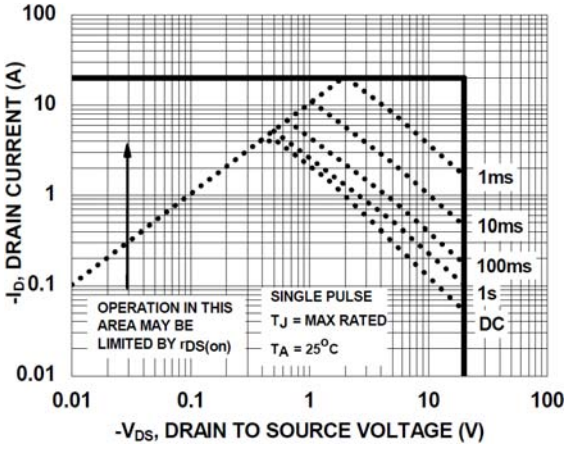
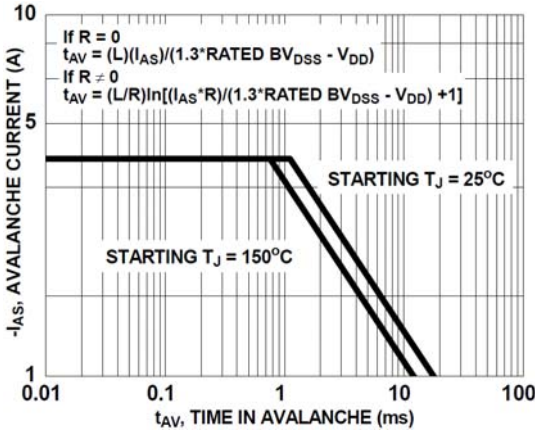


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

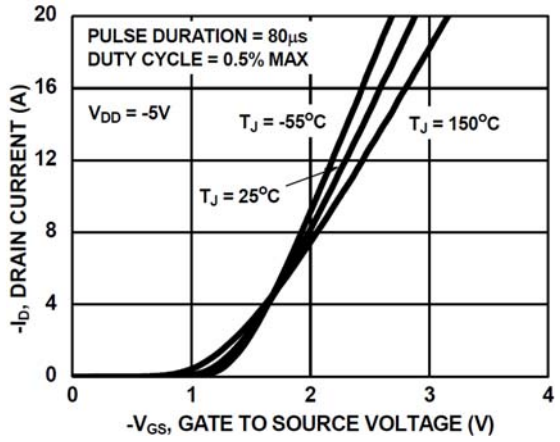


Figure 7. Transfer Characteristics

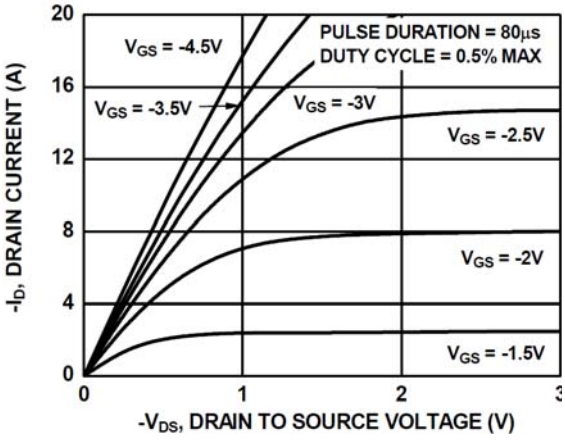


Figure 8. Saturation Characteristics

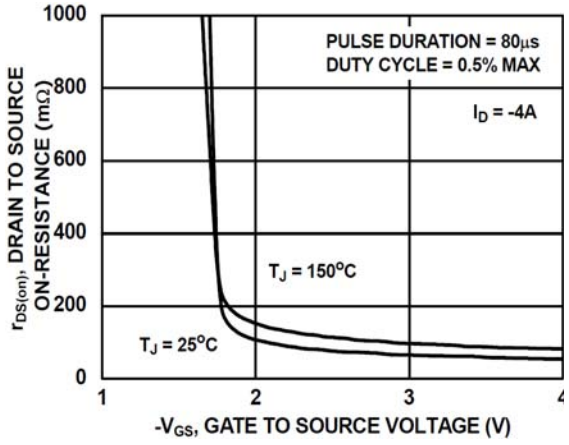


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

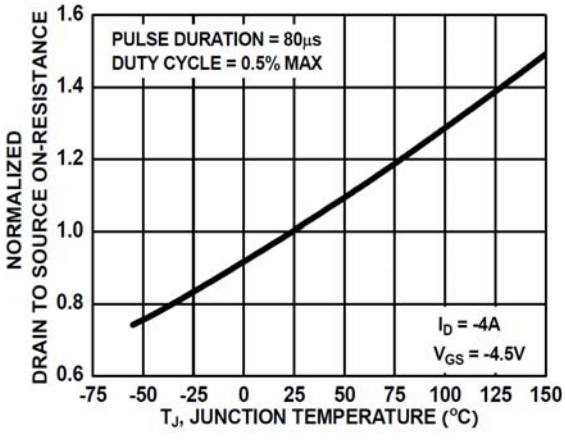


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics

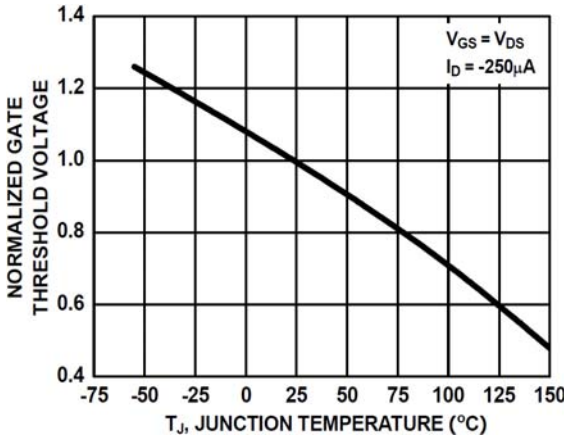


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

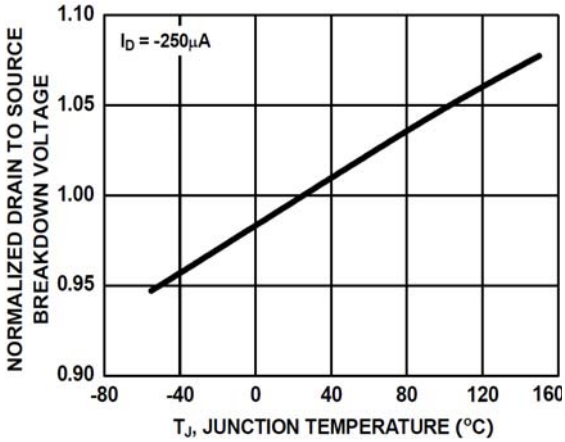


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

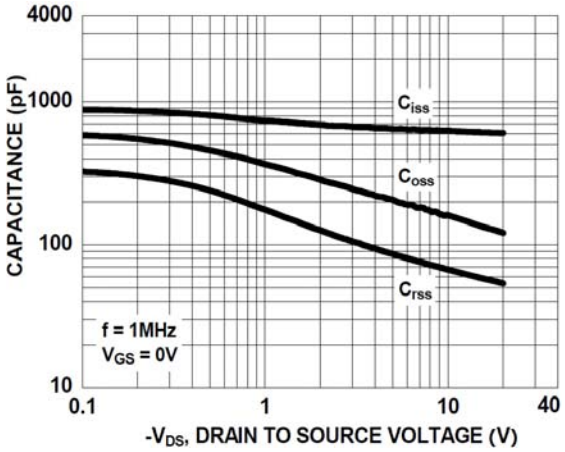


Figure 13. Capacitance vs Drain to Source Voltage

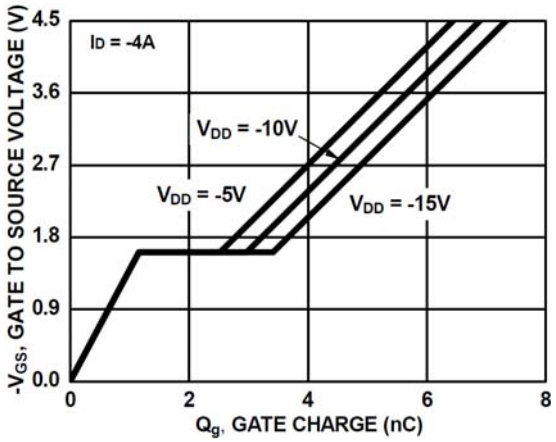
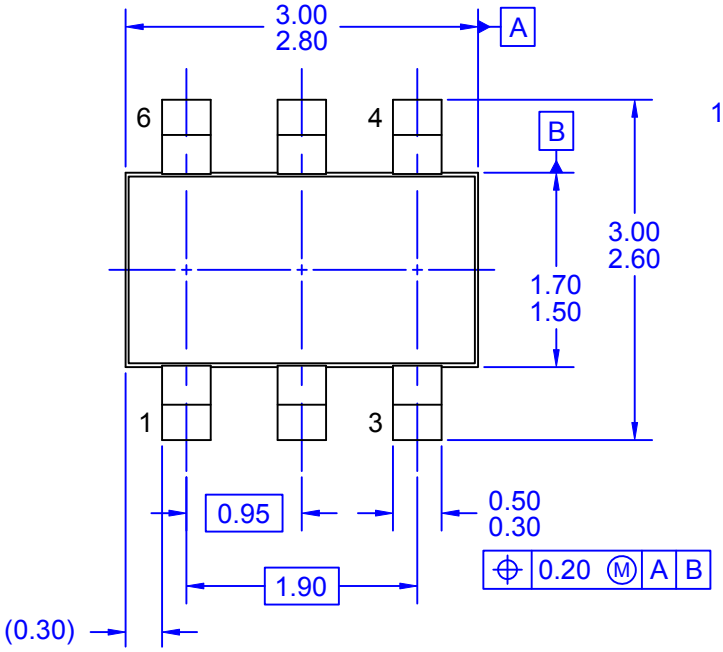
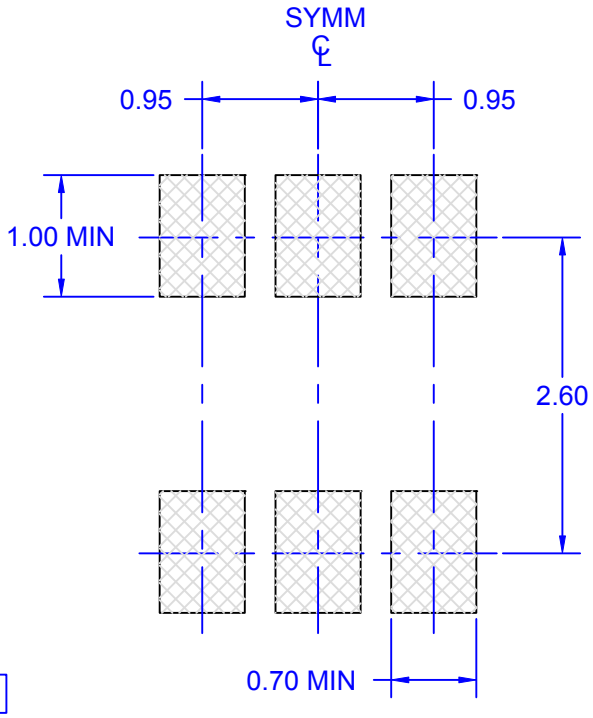
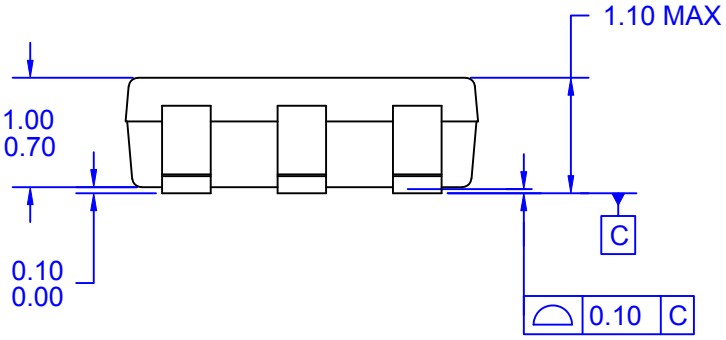


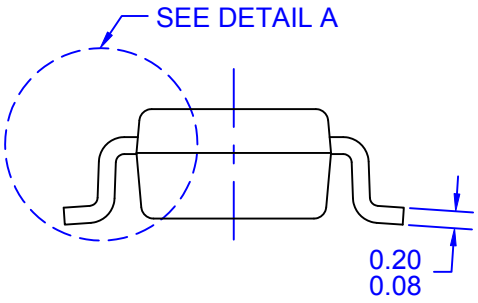
Figure 14. Gate Charge vs Gate to Source Voltage

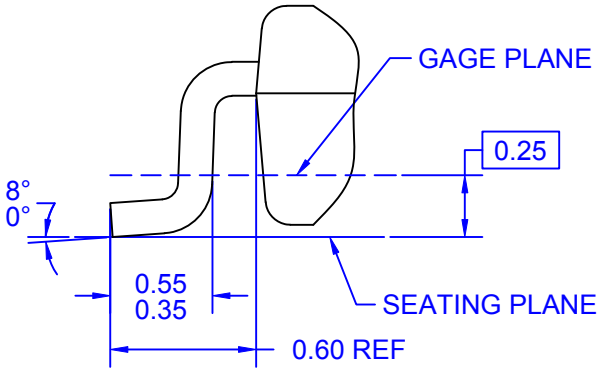




LAND PATTERN RECOMMENDATION







DETAIL A
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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