FDB12N50F

N-Channel UniFET^{TM} FRFET$^®$ MOSFET

500 V, 11.5 A, 700 mΩ

Features

- $R_{DS(on)}$ = 590 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 6 A
- Low Gate Charge (Typ. 21 nC)
- Low C_{rss} (Typ. 11 pF)
- 100% Avalanche Tested
- Improve dv/dt Capability
- RoHS Compliant

Applications

- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET^{TM} MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET$^®$ MOSFET has been enhanced by lifetime control. Its t_{rr} is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

D

G
S
D^2-PAK

D

G

S
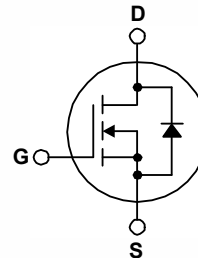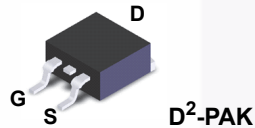
MOSFET Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter			FDB12N50FTM_WS	Unit
V_{DSS}	Drain to Source Voltage			500	V
V_{GSS}	Gate to Source Voltage			±30	V
I_D	Drain Current	- Continuous (T_C = 25°C)		11.5	A
		- Continuous (T_C = 100°C)		6.9	
I_{DM}	Drain Current	- Pulsed	(Note 1)	46	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	456	mJ
I_{AR}	Avalanche Current		(Note 1)	11.5	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	16.5	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	20	V/ns
P_D	Power Dissipation	(T_C = 25°C)		165	W
		- Derate above 25°C		1.33	W/^{o}C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	^{o}C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	^{o}C

Thermal Characteristics

Symbol	Parameter	FQB12N50FTM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.75	^{o}C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in^2 pad of 2 oz copper), Max.	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB12N50F	FDB12N50FTM_WS	D2-PAK	330mm	24mm	800 units

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$, $T_J = 25^oC$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$, Referenced to 25^oC	-	0.5	-	V/^oC
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500V$, $V_{GS} = 0V$	-	-	10	μA
		$V_{DS} = 400V$, $T_C = 125^oC$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30V$, $V_{DS} = 0V$	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10V$, $I_D = 6A$	-	0.59	0.7	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40V$, $I_D = 6A$	-	12	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz	-	1050	1395	pF
C_{oss}	Output Capacitance		-	135	180	pF
C_{rss}	Reverse Transfer Capacitance		-	11	17	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400V$, $I_D = 11.5A$ $V_{GS} = 10V$	-	21	30	nC
Q_{gs}	Gate to Source Gate Charge		-	6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	9	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250V$, $I_D = 11.5A$ $R_G = 25\Omega$	-	21	50	ns
t_r	Turn-On Rise Time		-	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		-	50	110	ns
t_f	Turn-Off Fall Time	(Note 4)	-	35	80	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	11.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	46	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V$, $I_{SD} = 11.5A$	-	-	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0V$, $I_{SD} = 11.5A$ $dI_F/dt = 100A/\mu s$	-	134	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.37	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. L = 6.9mH, $I_{AS} = 11.5A$, $V_{DD} = 50V$, $R_G = 25\Omega$, Starting $T_J = 25°C$

3. $I_{SD} \le 11.5A$, di/dt $\le 200A/\mu s$, $V_{DD} \le BV_{DSS}$, Starting $T_J = 25°C$

4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Characteristics

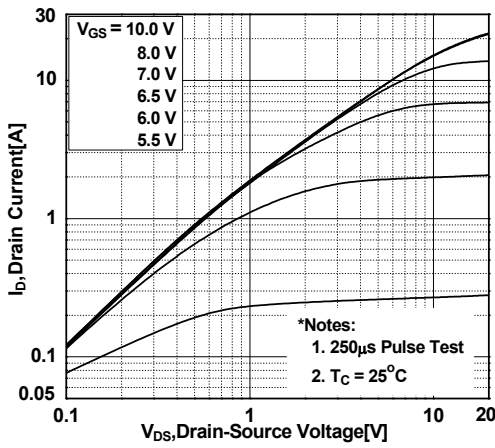### Figure 1. On-Region Characteristics
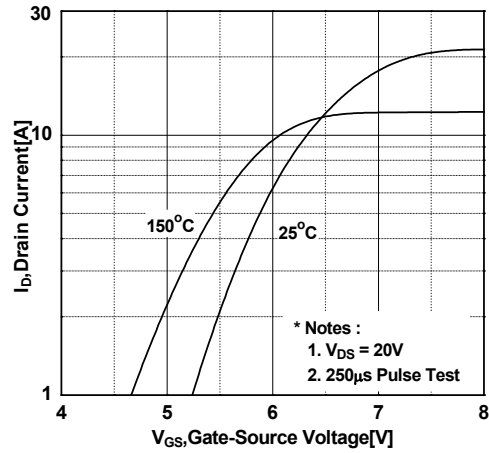

Figure 2. Transfer Characteristics

Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage
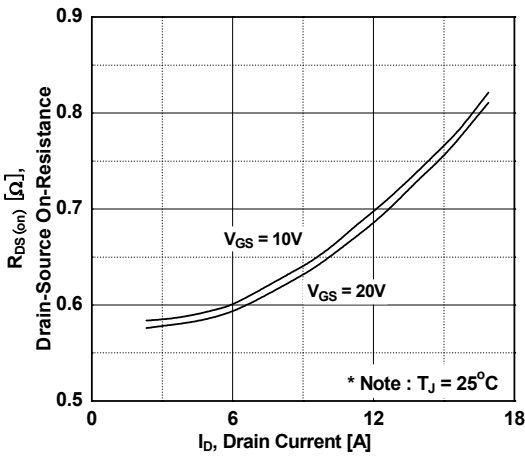

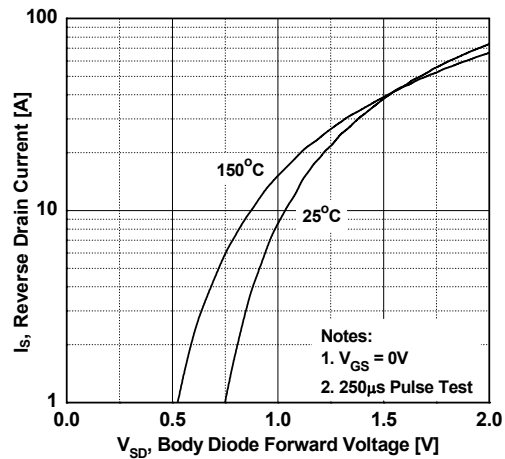### Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature
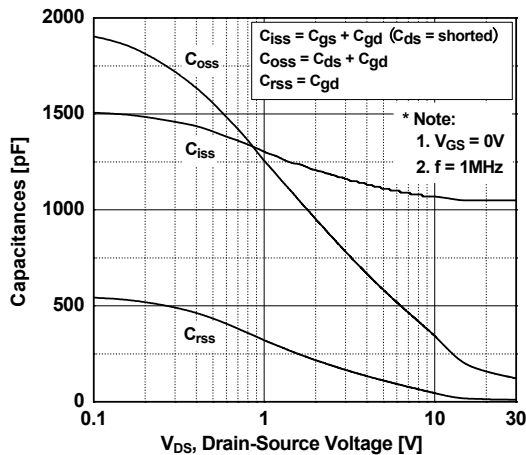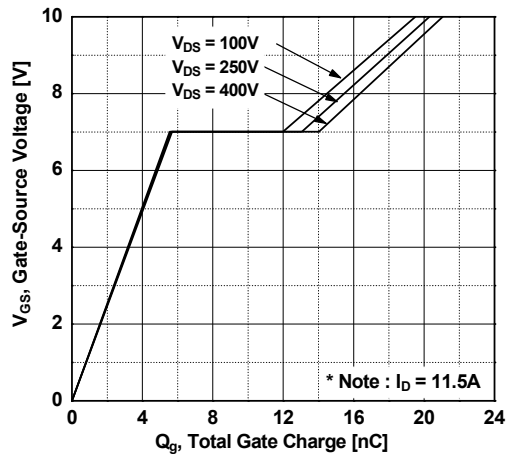

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

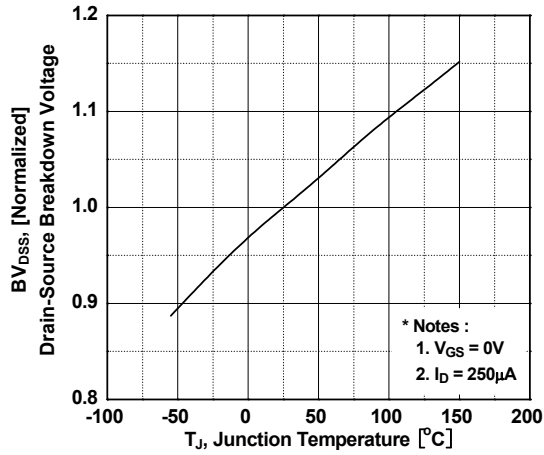### Figure 7. Breakdown Voltage Variation vs. Temperature

* Notes :
1. V_{GS} = 0V
2. I_D = 250µA

Figure 8. Maximum Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

*Notes:
1. T_C = 25°C
2. T_J = 150°C
3. Single Pulse
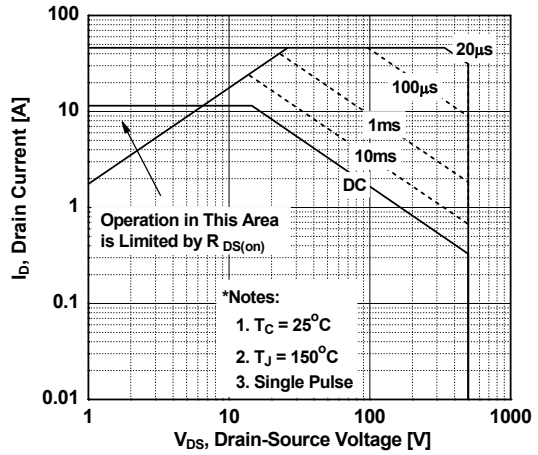
Figure 9. Maximum Drain Current vs. Case Temperature
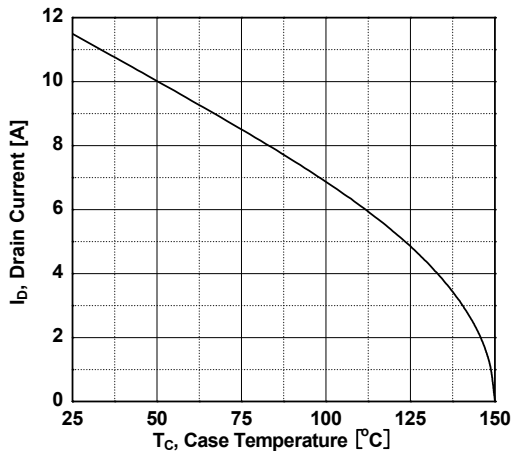
Figure 10. Transient Thermal Response Curve

*Notes:
1. $Z_{\theta JC}(t)$ = 0.75°C/W Max.
2. Duty Factor, D= t_1/t_2
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$
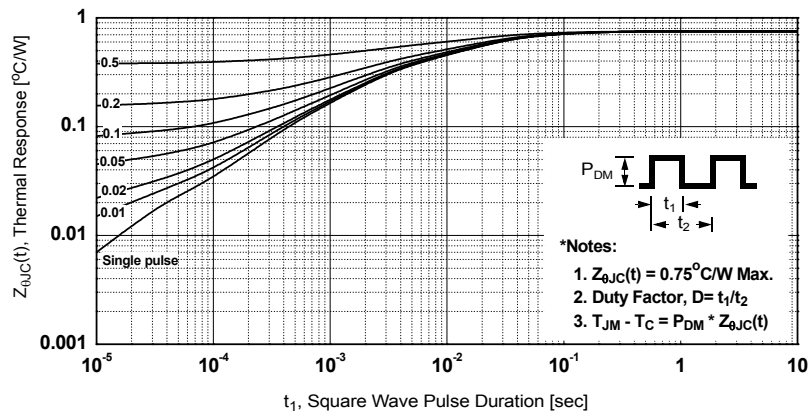
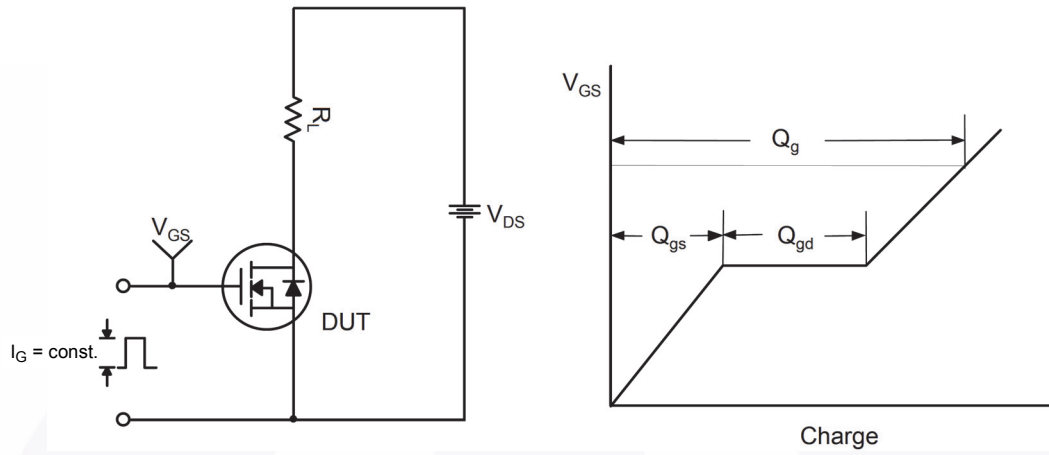## Figure 11. Gate Charge Test Circuit & Waveform

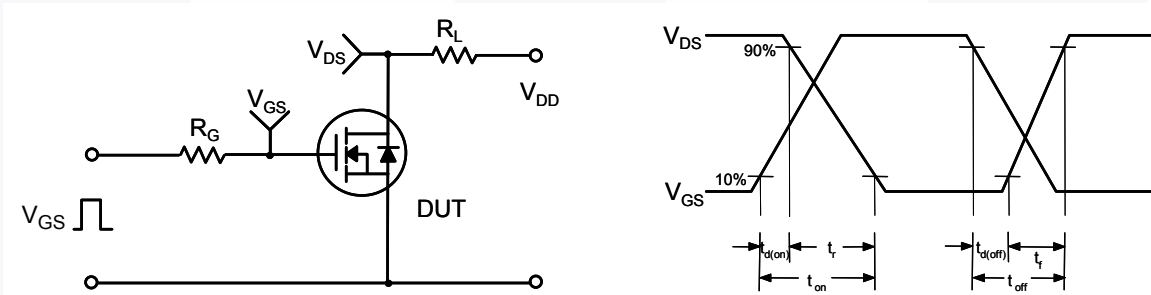## Figure 12. Resistive Switching Test Circuit & Waveforms

Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$
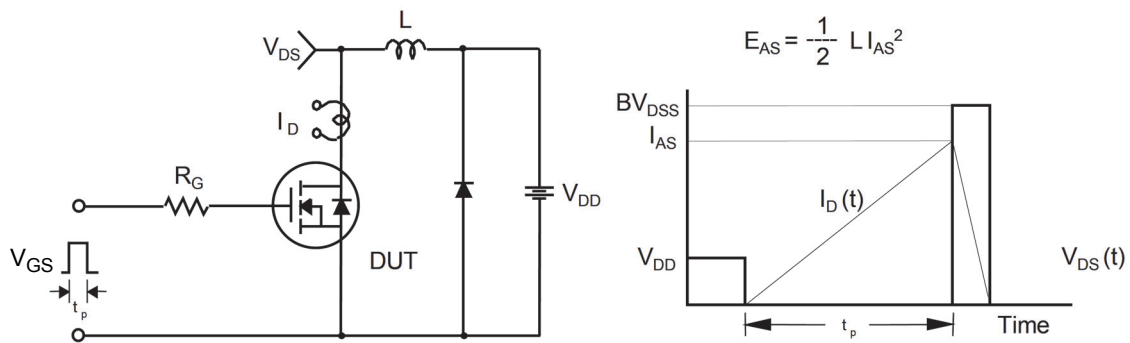
Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop
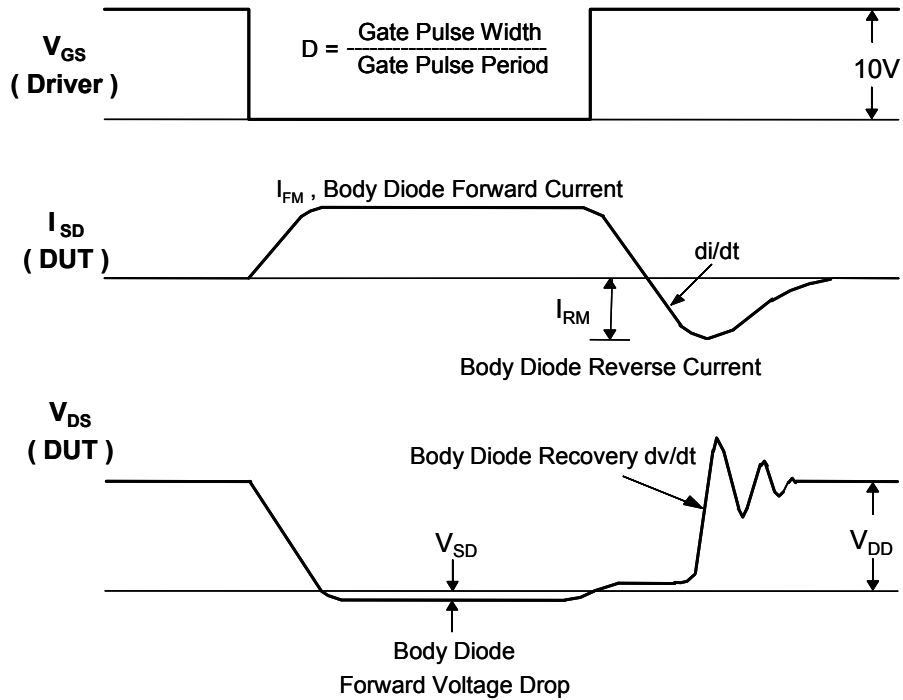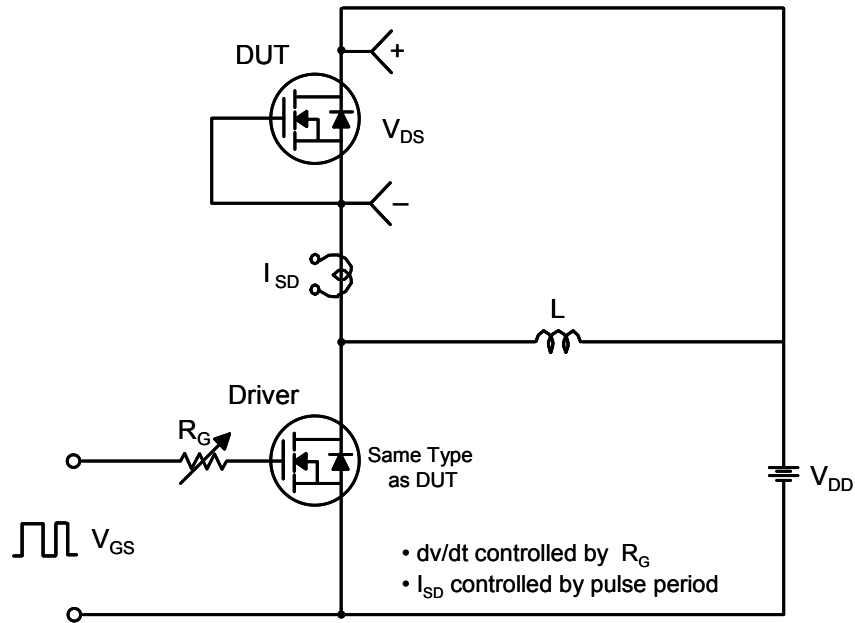
Mechanical Dimensions

TO-263 2L (D^{2}PAK)

Figure 15. 2LD,TO263, Surface Mount

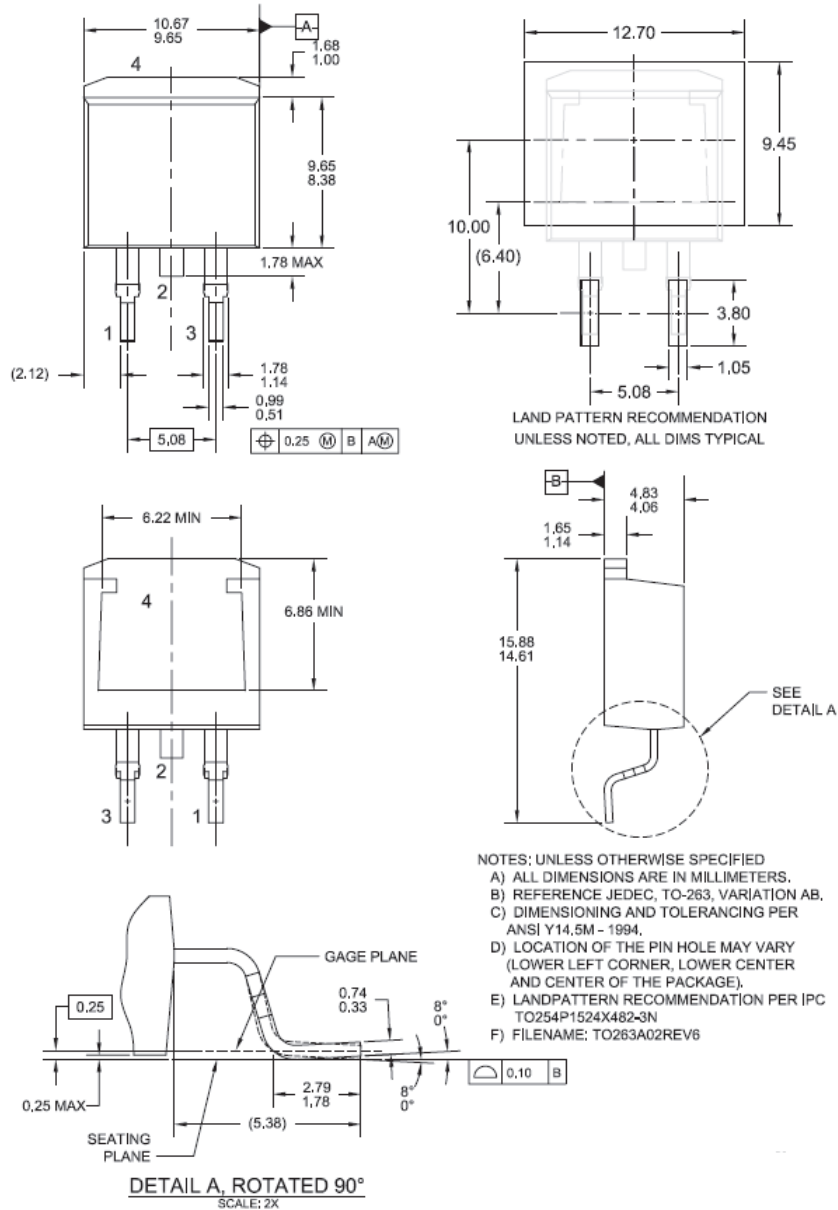Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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Dimension in Millimeters

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