FAIRCHILD™

June 2014

FCA47N60 / FCA47N60_F109

N-Channel SuperFET® MOSFET

600 V, 47 A, 70 mΩ

Features

- 650 V @ T_J = 150°C
- Typ. $R_{DS(on)}$ = 58 mΩ
- Ultra Low Gate Charge (Typ. Q_g= 210 nC)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 420 pF)
- 100% Avalanche Tested

Application

- Solar Invertor
- AC-DC Power Supply

Description

SuperFET® MOSFET is Fairchild Semiconductor's first genera-tion of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switch-ing performance, dv/dt rate and higher avalanche energy. Con-sequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

TO-3PN

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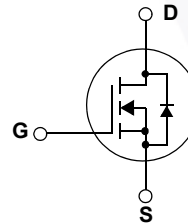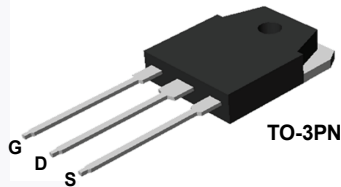
Absolute Maximum Ratings

Symbol	Parameter		FCA47N60	FCA47N60_F109	Unit
V_{DSS}	Drain-Source Voltage		600		V
I_D	Drain Current	- Continuous (T_C = 25°C) - Continuous (T_C = 100°C)	47 29.7		A A
I_{DM}	Drain Current	- Pulsed (Note 1)	141		A
V_{GSS}	Gate-Source voltage		± 30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1800		mJ
I_{AR}	Avalanche Current (Note 1)		47		A
E_{AR}	Repetitive Avalanche Energy (Note 1)		41.7		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
P_D	Power Dissipation	(T_C = 25°C) - Derate above 25°C	417 3.33		W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300		°C

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	--	0.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	--	41.7	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCA47N60	FCA47N60	TO-3PN	-	-	30
FCA47N60	FCA47N60_F109	TO-3PN	-	-	30

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA, T_J = 25°C	600	--	--	V
		V_{GS} = 0 V, I_D = 250 μA, T_J = 150°C	--	650	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.6	--	V/°C
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 47 A	--	700	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 480 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	5.0	
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 23.5 A	--	0.058	0.07	
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 23.5 A	--	40	--	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	5.0	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	5900	8000	pF
C_{oss}	Output Capacitance		--	3200	4200	pF
C_{rss}	Reverse Transfer Capacitance		--	250	--	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1.0 MHz	--	160	--	pF
C_{oss} eff.	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	--	420	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 300 V, I_D = 47 A	--	185	430	ns
t_r	Turn-On Rise Time	R_G = 25 Ω	--	210	450	ns
$t_{d(off)}$	Turn-Off Delay Time		--	520	1100	ns
t_f	Turn-Off Fall Time	(Note 4)	--	75	160	ns
Q_g	Total Gate Charge	V_{DS} = 480 V, I_D = 47 A	--	210	270	nC
Q_{gs}	Gate-Source Charge	V_{GS} = 10 V	--	38	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	--	110	--	nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	47	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	141	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 47 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 47 A	--	590	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F/dt =100 A/μs (Note 4)	--	25	--	μC

Notes:

1. Repetitive Rating: Pulse-width limited by maximum junction temperature.

2. I_{AS} = 18 A, R_G = 25 Ω, starting T_J = 25°C

3. I_{SD} ≤ 47 A, di/dt ≤ 200 A/μs, V_{DD} = 380 V, starting T_J = 25°C

4. Essentially independent of operating temperature typical characteristics.

FCA47N60 / FCA47N60_F109 — N-Channel SuperFET® MOSFET

Typical Characteristics

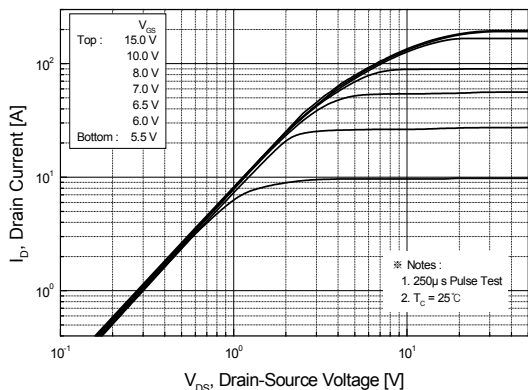### Figure 1. On-Region Characteristics

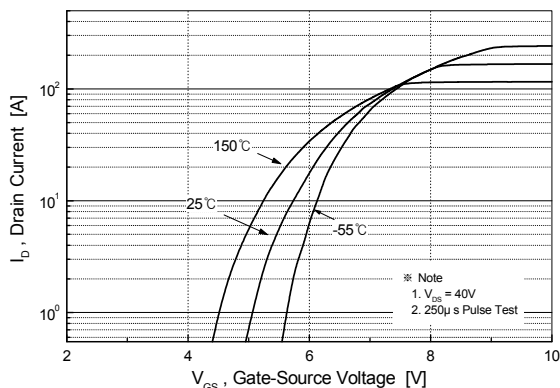### Figure 2. Transfer Characteristics

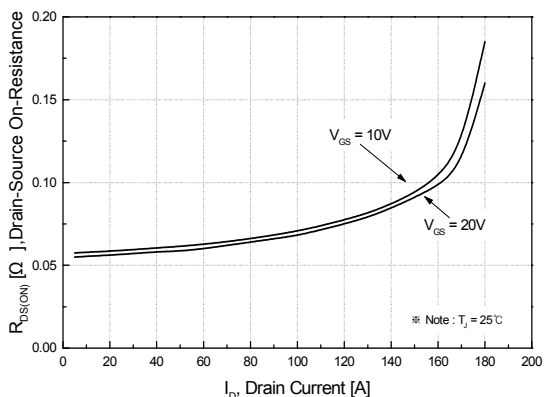### Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue
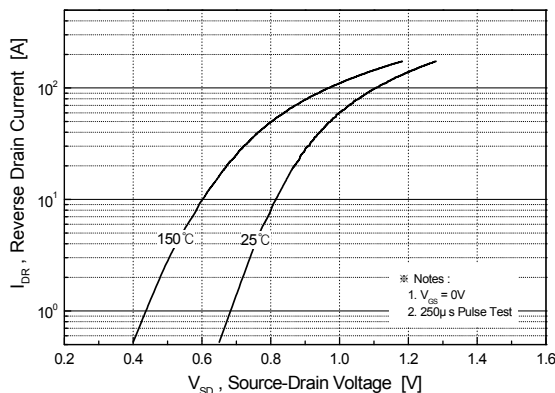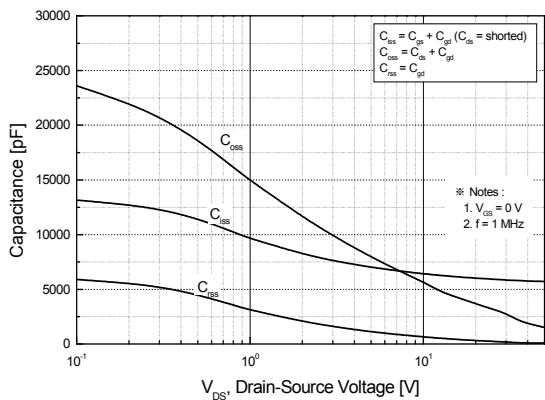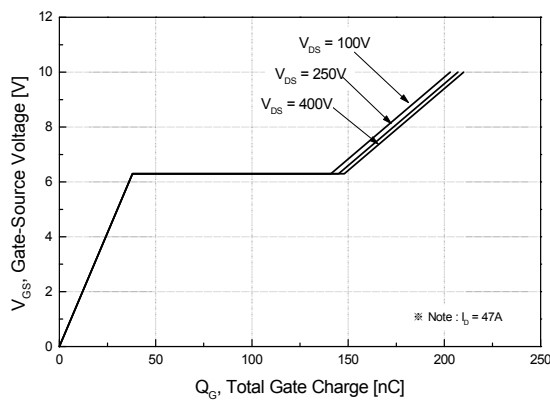

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)
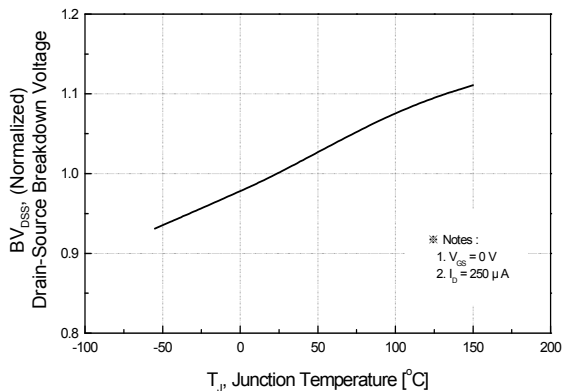
Figure 7. Breakdown Voltage Variation vs. Temperature

Y-axis: BV_{DSS}, (Normalized) Drain-Source Breakdown Voltage

X-axis: T_J, Junction Temperature [°C]

※ Notes :
1. V_{GS} = 0 V
2. I_D = 250 μA

Figure 8. On-Resistance Variation vs. Temperature

Y-axis: $R_{DS(ON)}$, (Normalized) Drain-Source On-Resistance

X-axis: T_J, Junction Temperature [°C]

※ Notes :
1. V_{GS} = 10 V
2. I_D = 47 A
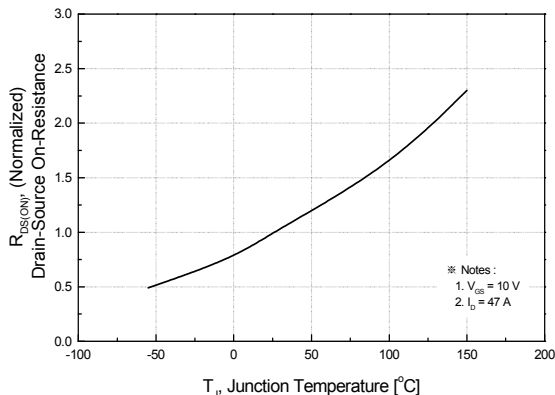
Figure 9. Safe Operating Area

Operation in This Area is Limited by $R_{DS(on)}$

100 us
1 ms
10 ms
DC

Y-axis: I_D, Drain Current [A]

X-axis: V_{DS}, Drain-Source Voltage [V]

※ Notes :
1. T_C = 25 °C
2. T_J = 150 °C
3. Single Pulse
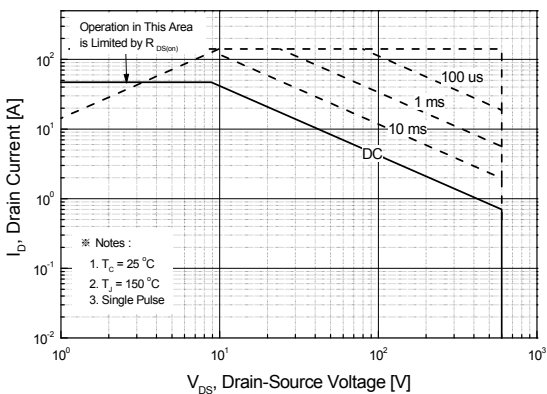
Figure 10. Maximum Drain Current vs. Case Temperature

Y-axis: I_D, Drain Current [A]

X-axis: T_C, Case Temperature [°C]
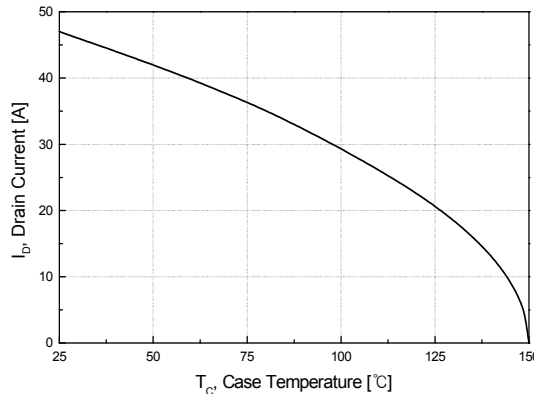
Figure 11. Transient Thermal Response Curve

D = 0.5
0.2
0.1
0.05
0.02
0.01
single pulse

Y-axis: $Z_{\theta JC}(t)$, Thermal Response

X-axis: t_1, Square Wave Pulse Duration [sec]

※ Notes :
1. $Z_{\theta JC}(t)$ = 0.3 °C/W Max.
2. Duty Factor, D = t_1/t_2
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$

P_{DM}
t_1
t_2
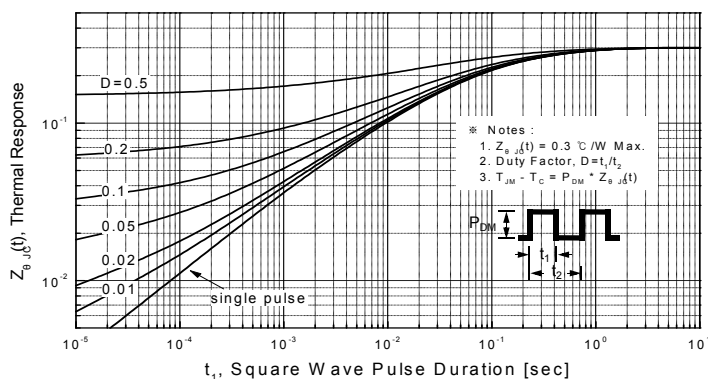
Figure 12. Gate Charge Test Circuit & Waveform
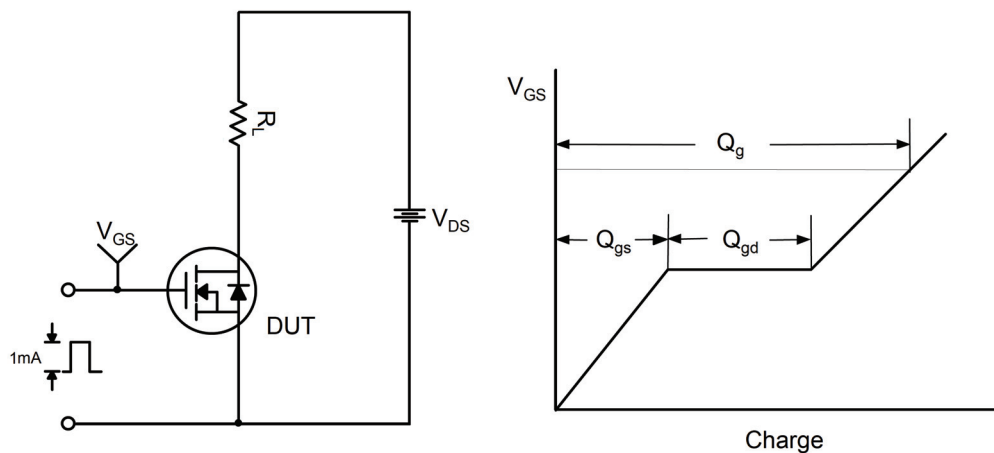
Figure 13. Resistive Switching Test Circuit & Waveforms
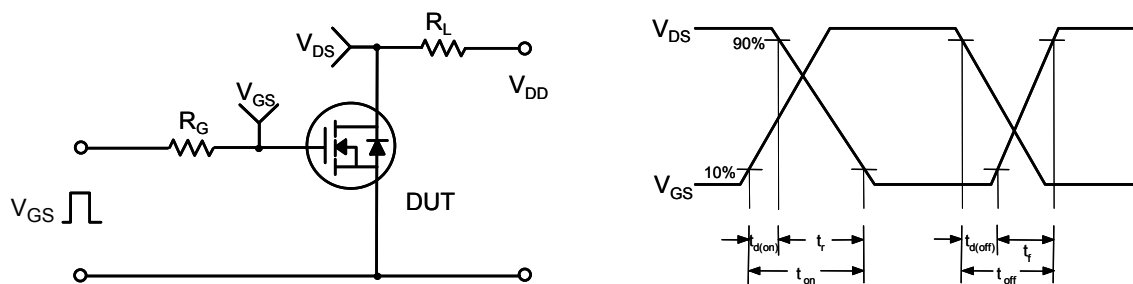
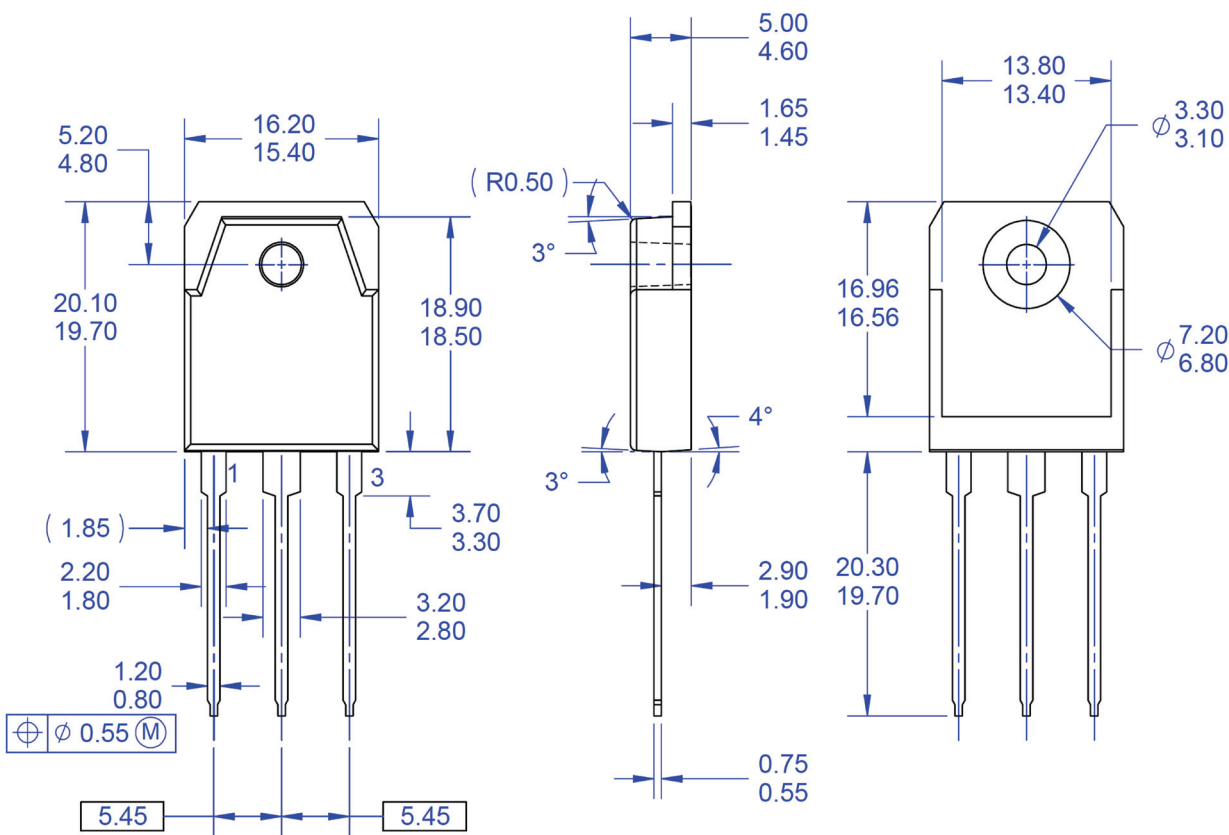
Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$
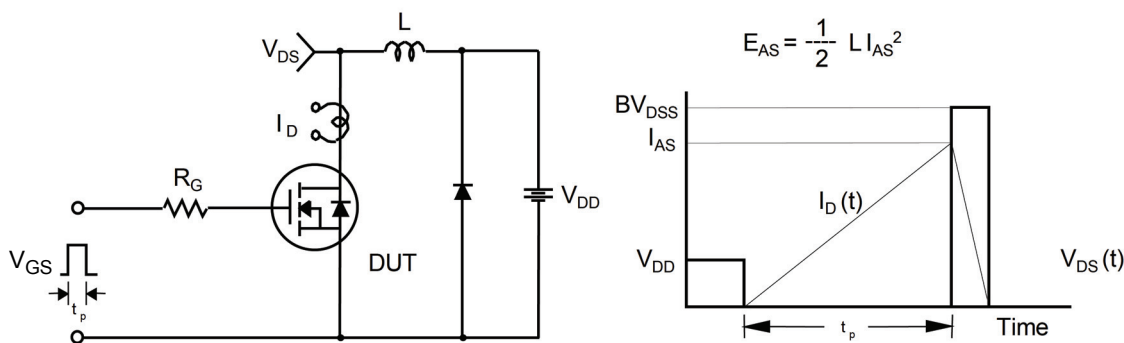
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop
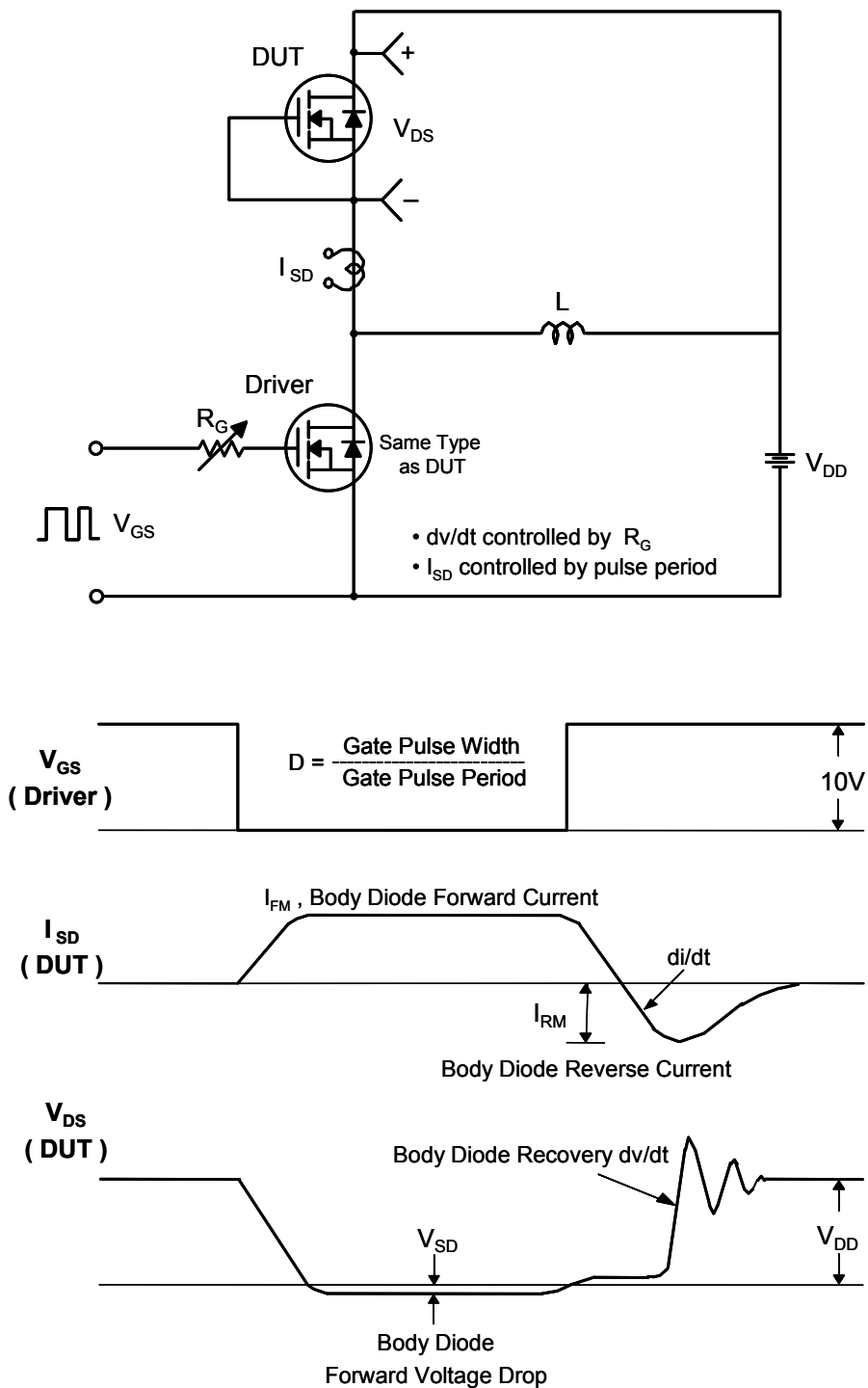
Mechanical Dimensions

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO EIAJ
   SC-65 PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSION AND TOLERANCING PER
   ASME14.5-2009.
D) DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH, AND TIE BAR EXTRUSSIONS.
E) DRAWING FILE NAME: TO3PN03AREV1.
F) FAIRCHILD SEMICONDUCTOR.
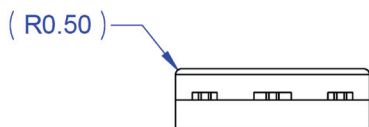
Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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