

Features

- High speed
 - $t_{AA} = 12 \text{ ns}$
- Low active power
 - $I_{CC} = 250 \text{ mA}$ at 83.3 MHz
- Low Complementary Metal Oxide Semiconductor (CMOS) standby power
 - $I_{SB2} = 50 \text{ mA}$
- Operating voltages of $3.3 \pm 0.3 \text{ V}$
- 2.0 V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Available in Pb-free 48-ball FBGA package

Functional Description

The CY7C1071DV33 is a high performance CMOS Static RAM organized as 2,097,152 words by 16 bits. The input and output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when:

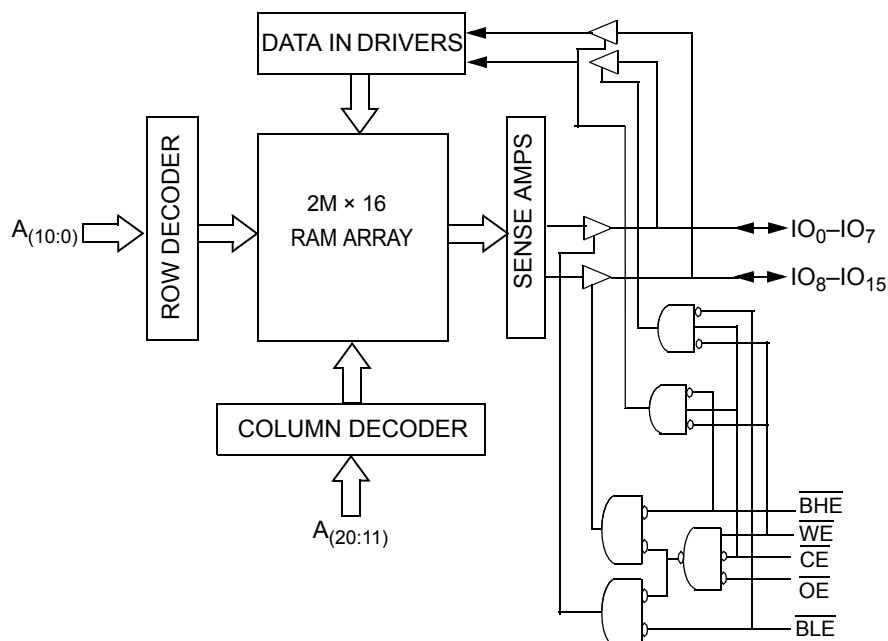
- Deselected (\overline{CE} HIGH)
- Outputs are disabled (\overline{OE} HIGH)
- Both byte high enable and byte low enable are disabled (\overline{BHE} , \overline{BLE} HIGH)
- The write operation is active (\overline{CE} LOW and \overline{WE} LOW)

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{20}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{20}).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appears on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See the [Truth Table on page 10](#) for a complete description of read and write modes.

For a complete list of related documentation, [click here](#).

Logic Block Diagram



Contents

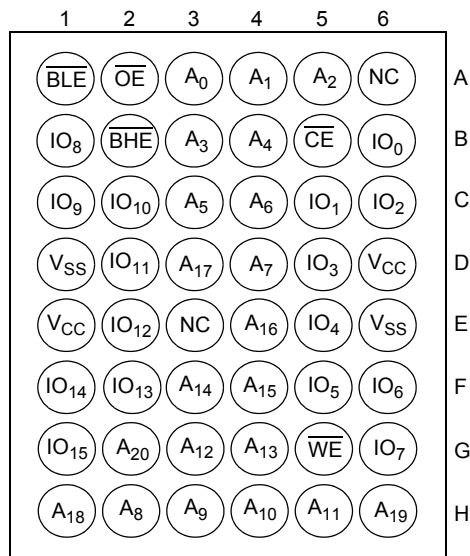
| | | | |
|---|-----------|--|-----------|
| Selection Guide | 3 | Ordering Information | 10 |
| Pin Configuration | 3 | Ordering Code Definitions | 10 |
| Maximum Ratings | 4 | Package Diagram | 11 |
| Operating Range | 4 | Acronyms | 12 |
| DC Electrical Characteristics | 4 | Document Conventions | 12 |
| Capacitance | 4 | Units of Measure | 12 |
| Thermal Resistance | 4 | Document History Page | 13 |
| AC Test Loads and Waveforms | 5 | Sales, Solutions, and Legal Information | 14 |
| Data Retention Characteristics | 5 | Worldwide Sales and Design Support | 14 |
| AC Switching Characteristics | 6 | Products | 14 |
| Switching Waveforms | 7 | PSoC Solutions | 14 |
| Truth Table | 10 | | |

Selection Guide

| Description | -12 | Unit |
|------------------------------|-----|------|
| Maximum Access Time | 12 | ns |
| Maximum Operating Current | 250 | mA |
| Maximum CMOS Standby Current | 50 | mA |

Pin Configuration

Figure 1. 48-ball FBGA [1]



Note

1. NC pins are not connected to the die.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

| | |
|---|-----------------------------------|
| Storage Temperature | -65 °C to +150 °C |
| Ambient Temperature with Power Applied | -55 °C to +125 °C |
| Supply Voltage on V _{CC} Relative to GND [2] | -0.3 V to +4.6 V |
| DC Voltage Applied to Outputs in High Z State [2] | -0.5 V to V _{CC} + 0.5 V |

| | |
|----------------------------------|-------------------------------------|
| DC Input Voltage [2] | -0.5 V to V _{CC} + 0.5 V |
| Current into Outputs (LOW) | 20 mA |
| Static Discharge Voltage | > 2001 V (MIL-STD-883, Method 3015) |
| Latch up Current | > 200 mA |

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Industrial | -40 °C to +85 °C | 3.3 V ± 0.3 V |

DC Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | -12 | | Unit |
|---------------------|---|---|------|-----------------------|------|
| | | | Min | Max | |
| V _{OH} | Output HIGH Voltage | Min V _{CC} , I _{OH} = -4.0 mA | 2.4 | - | V |
| V _{OL} | Output LOW Voltage | Min V _{CC} , I _{OL} = 8.0 mA | - | 0.4 | V |
| V _{IH} [2] | Input HIGH Voltage | | 2.0 | V _{CC} + 0.3 | V |
| V _{IL} [2] | Input LOW Voltage | | -0.3 | 0.8 | V |
| I _{IX} | Input Leakage Current | GND ≤ V _{IN} ≤ V _{CC} | -1 | +1 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _{OUT} ≤ V _{CC} , Output Disabled | -1 | +1 | μA |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max, f = f _{max} = 1/t _{RC} , I _{OUT} = 0 mA CMOS levels | - | 250 | mA |
| I _{SB1} | Automatic CE Power Down Current – TTL Inputs | Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{max} | - | 60 | mA |
| I _{SB2} | Automatic CE Power Down Current – CMOS Inputs | Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3$ V, V _{IN} ≥ V _{CC} - 0.3 V, or V _{IN} ≤ 0.3 V, f = 0, V _{CC} = V _{CC(max)} | - | 50 | mA |

Capacitance

| Parameter ^[3] | Description | Test Conditions | Max | Unit |
|--------------------------|-------------------|--|-----|------|
| C _{IN} | Input Capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V | 16 | pF |
| C _{OUT} | I/O Capacitance | | 20 | pF |

Thermal Resistance

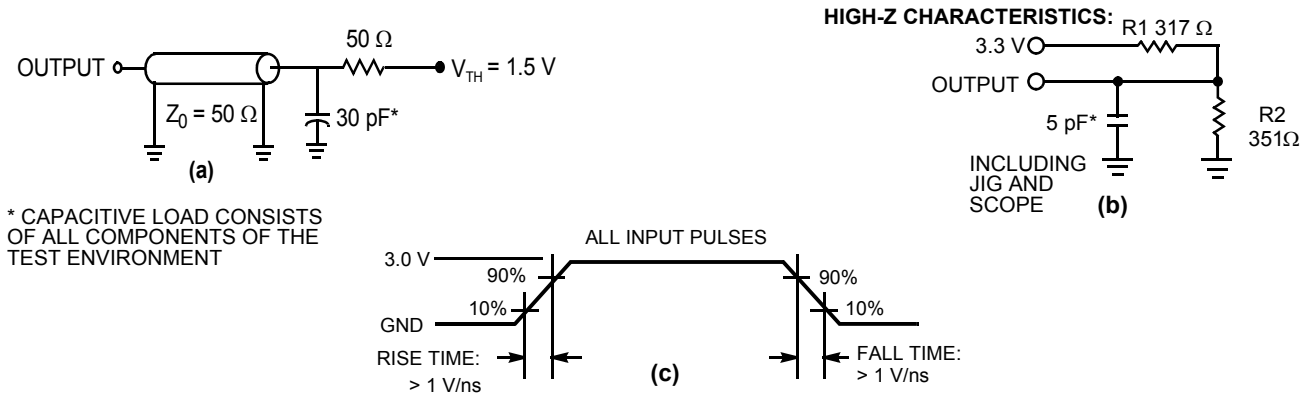
| Parameter ^[3] | Description | Test Conditions | 48-ball FBGA | Unit |
|--------------------------|--|---|--------------|------|
| θ _{JA} | Thermal Resistance (Junction to Ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 24.72 | °C/W |
| θ _{JC} | Thermal Resistance (Junction to Case) | | 5.79 | °C/W |

Notes

- V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 1 V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms [4]

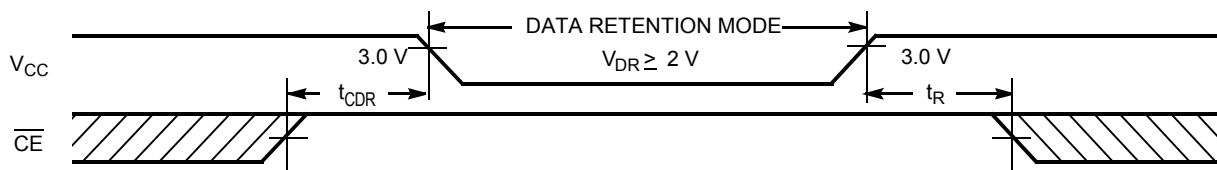


Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------------------|--------------------------------------|---|-----------------|-----|-----|------|
| V _{DR} | V _{CC} for Data Retention | | 2 | — | — | V |
| I _{CCDR} | Data Retention Current | V _{CC} = 2 V, $\overline{CE} \geq V_{CC} - 0.2$ V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V | — | — | 50 | mA |
| t _{CDR} ^[5] | Chip Deselect to Data Retention Time | | 0 | — | — | ns |
| t _R ^[6] | Operation Recovery Time | | t _{RC} | — | — | ns |

Figure 3. Data Retention Waveform



Notes

- Valid SRAM operation does not occur until the power supplies reach the minimum operating V_{DD} (3.0 V). 100 μs (t_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation begins to include reduction in V_{DD} to the data retention (V_{CCDR}, 2.0 V) voltage.
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min)} ≥ 50 μs or stable at V_{CC(min)} ≥ 50 μs.

AC Switching Characteristics

 Over the Operating Range ^[7]

| Parameter | Description | -12 | | Unit |
|--|--|-----|-----|---------|
| | | Min | Max | |
| Read Cycle | | | | |
| t_{power} | $V_{CC(typ)}$ to the first access ^[8] | 100 | – | μs |
| t_{RC} | Read Cycle Time | 12 | – | ns |
| t_{AA} | Address to Data Valid | – | 12 | ns |
| t_{OHA} | Data Hold from Address Change | 3 | – | ns |
| t_{ACE} | \overline{CE} LOW to Data Valid | – | 12 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | – | 7 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[9] | 1 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[9] | – | 7 | ns |
| t_{LZCE} | \overline{CE} LOW to Low Z ^[9] | 3 | – | ns |
| t_{HZCE} | \overline{CE} HIGH to High Z ^[9] | – | 7 | ns |
| t_{PU} | \overline{CE} LOW to Power Up ^[10] | 0 | – | ns |
| t_{PD} | \overline{CE} HIGH to Power Down ^[10] | – | 12 | ns |
| t_{DBE} | Byte Enable to Data Valid | – | 7 | ns |
| t_{LZBE} | Byte Enable to Low Z ^[9] | 1 | – | ns |
| t_{HZBE} | Byte Disable to High Z ^[9] | – | 7 | ns |
| Write Cycle ^[11, 12] | | | | |
| t_{WC} | Write Cycle Time | 12 | – | ns |
| t_{SCE} | \overline{CE} LOW to Write End | 9 | – | ns |
| t_{AW} | Address Setup to Write End | 9 | – | ns |
| t_{HA} | Address Hold from Write End | 0 | – | ns |
| t_{SA} | Address Setup to Write Start | 0 | – | ns |
| t_{PWE} | \overline{WE} Pulse Width | 9 | – | ns |
| t_{SD} | Data Setup to Write End | 7 | – | ns |
| t_{HD} | Data Hold from Write End | 0 | – | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[9] | 3 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[9] | – | 7 | ns |
| t_{BW} | Byte Enable to End of Write | 9 | – | ns |

Notes

- Test conditions are based on signal transition time of 3 ns or less and timing reference levels of 1.5 V and input pulse levels of 0 to 3.0 V. Test conditions for the read cycle use output loading shown in part (a) of [Figure 2 on page 5](#), unless specified otherwise.
- t_{power} is the minimum amount of time that the power supply must be at typical V_{CC} values until the first memory access can be performed.
- t_{HZOE} , t_{HZCE} , t_{HZWE} , t_{HZBE} and t_{LZOE} , t_{LZCE} , t_{LZWE} , t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of [Figure 2 on page 5](#). Transition is measured at ± 200 mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal memory write time is defined by the overlap of \overline{CE} , $\overline{WE} = V_{IL}$. Chip enables must be active and \overline{WE} and byte enables must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing must be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle 2 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled) [13, 14]

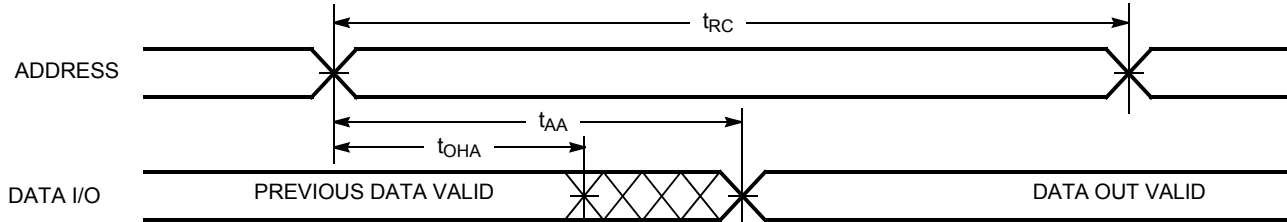
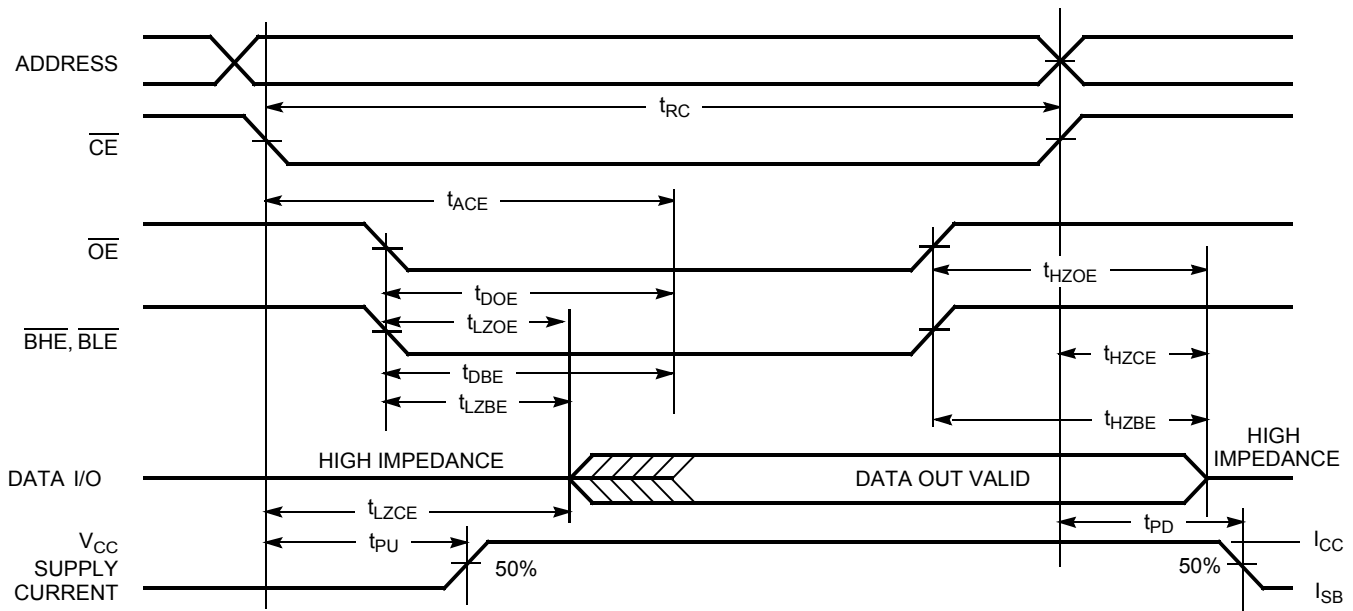


Figure 5. Read Cycle 2 (\overline{OE} Controlled) [14, 15]



Notes

- 13. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} or \overline{BLE} or both = V_{IL} .
- 14. \overline{WE} is HIGH for read cycle.
- 15. Address valid before or similar to \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle 1 ($\overline{\text{CE}}$ Controlled) [16, 17]

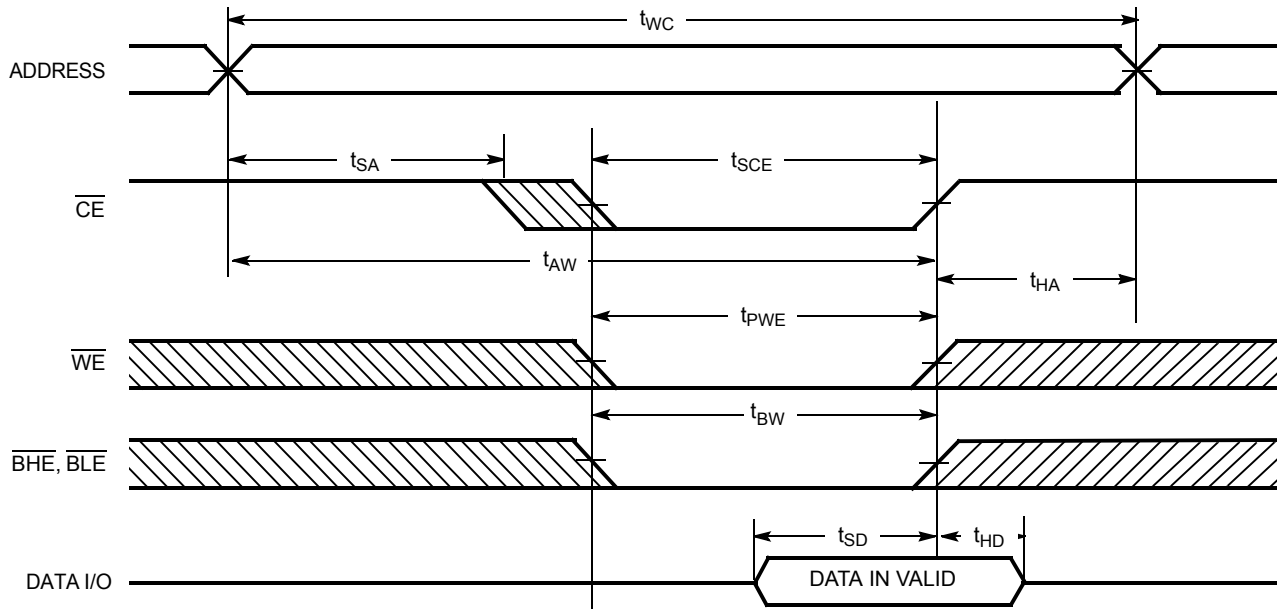
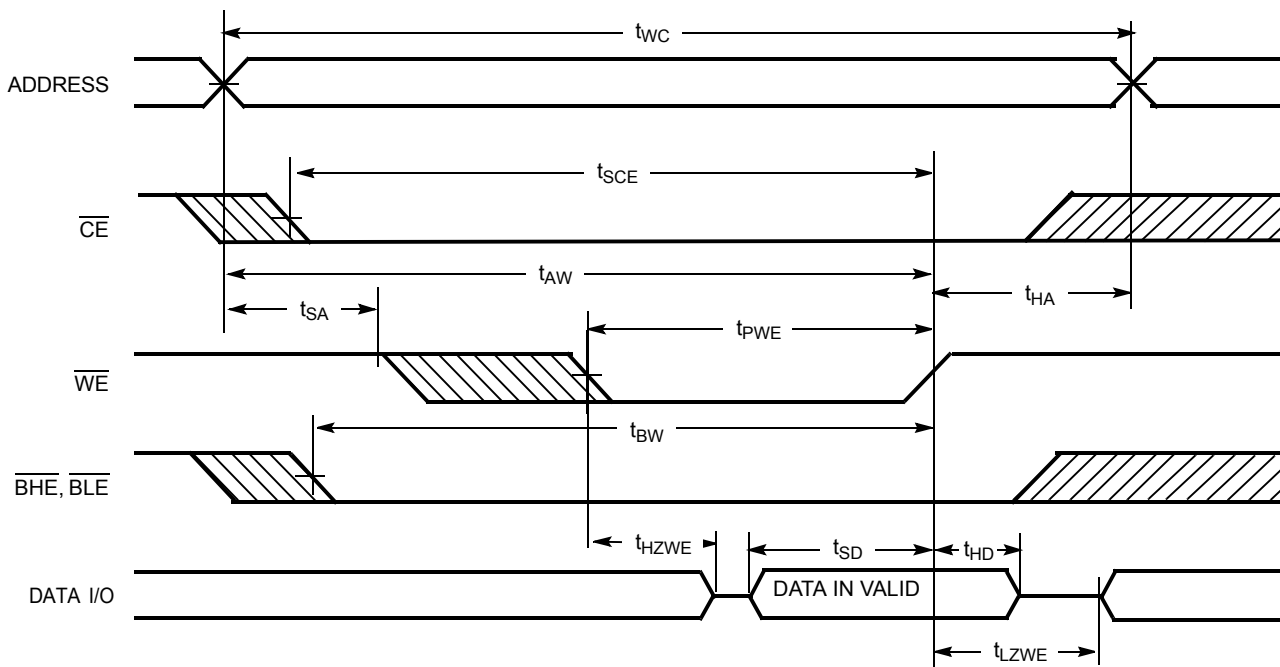


Figure 7. Write Cycle 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [16, 17]

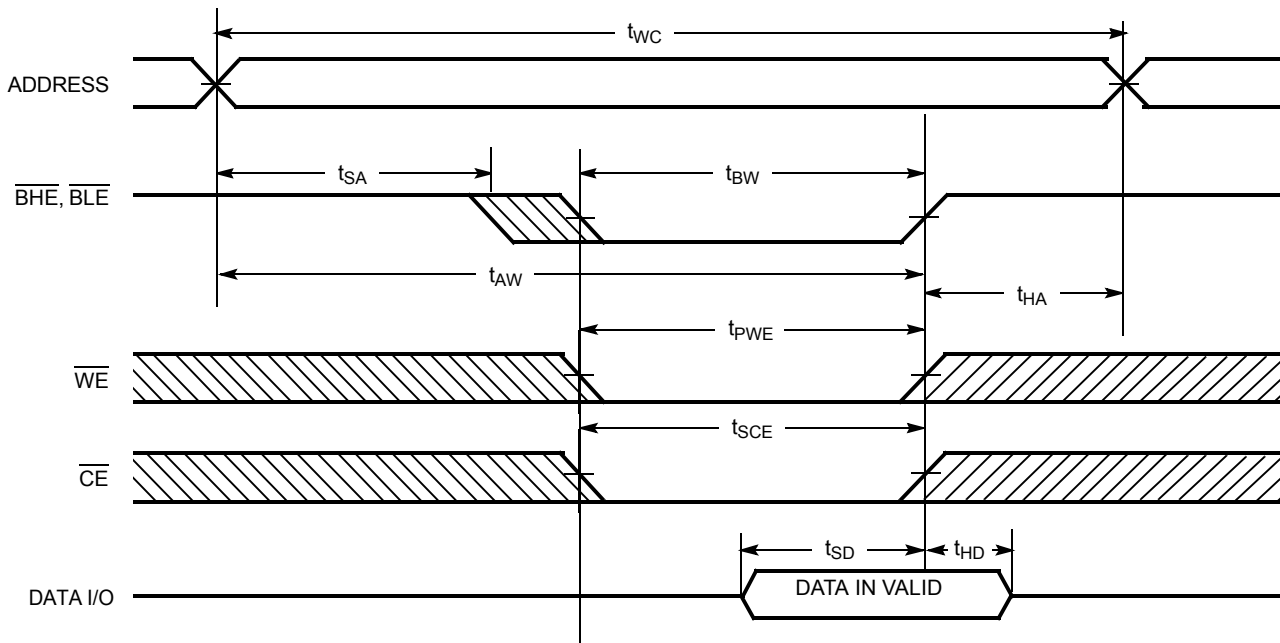


Notes

- 16. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ or both = V_{IH} .
- 17. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 8. Write Cycle 3 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

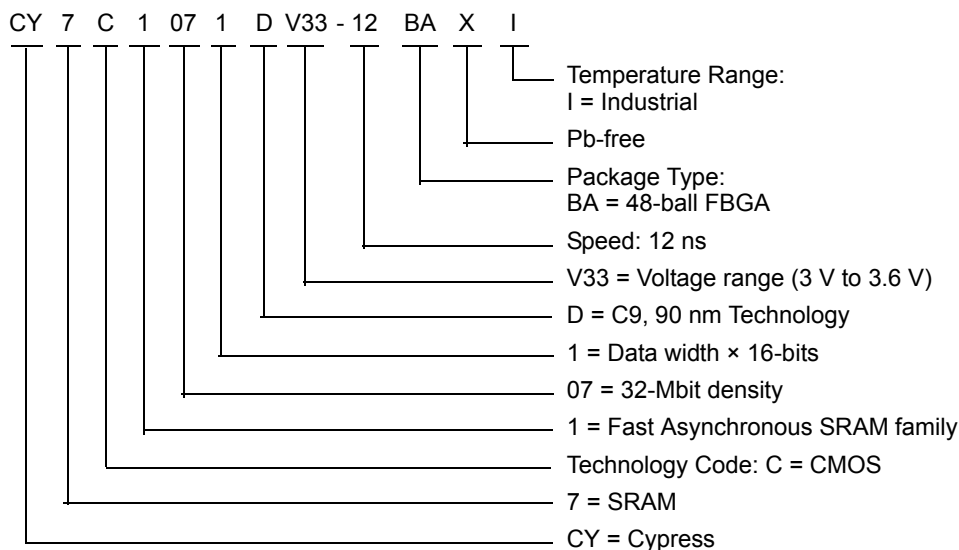


Truth Table

| \overline{CE} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O ₀ -I/O ₇ | I/O ₈ -I/O ₁₅ | Mode | Power |
|-----------------|-----------------|-----------------|------------------|------------------|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H | X | X | X | X | High Z | High Z | Power-down | Standby (I _{SB}) |
| L | L | H | L | L | Data Out | Data Out | Read All Bits | Active (I _{CC}) |
| L | L | H | L | H | Data Out | High Z | Read Lower Bits Only | Active (I _{CC}) |
| L | L | H | H | L | High Z | Data Out | Read Upper Bits Only | Active (I _{CC}) |
| L | X | L | L | L | Data In | Data In | Write All Bits | Active (I _{CC}) |
| L | X | L | L | H | Data In | High Z | Write Lower Bits Only | Active (I _{CC}) |
| L | X | L | H | L | High Z | Data In | Write Upper Bits Only | Active (I _{CC}) |
| L | H | H | X | X | High Z | High Z | Selected, Outputs Disabled | Active (I _{CC}) |

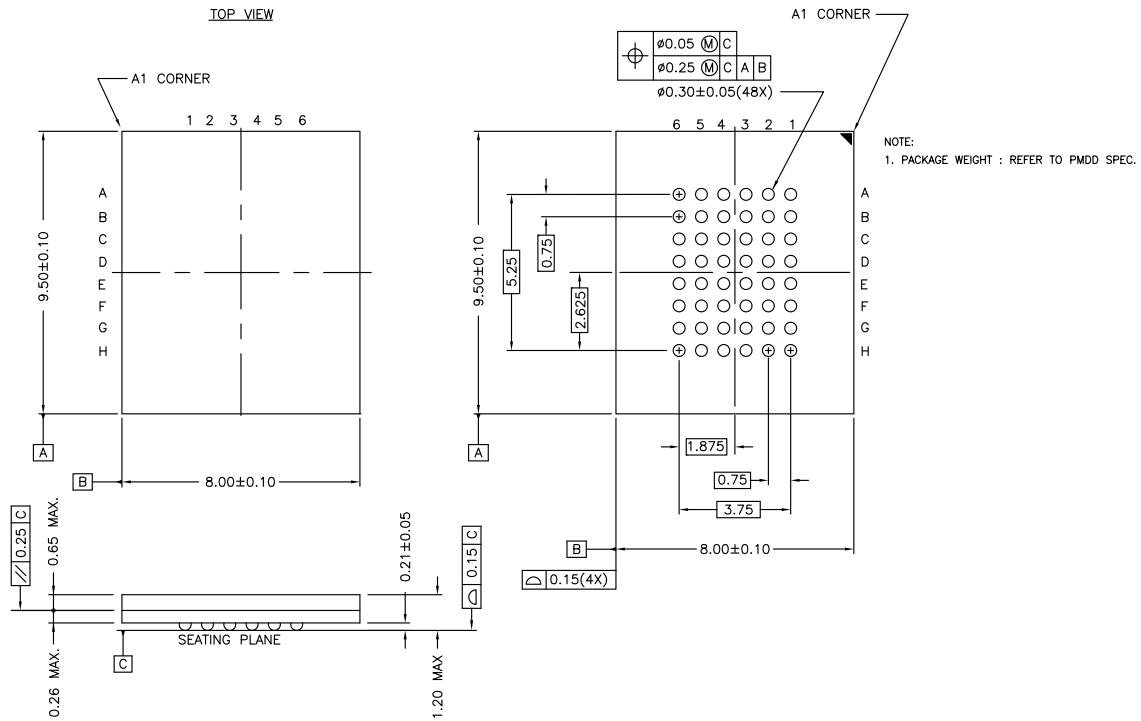
Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|---------------------|-----------------|---|-----------------|
| 12 | CY7C1071DV33-12BAXI | 51-85191 | 48-ball FBGA (8 × 9.5 × 1.2 mm) (Pb-free) | Industrial |

Ordering Code Definitions


Package Diagram

Figure 9. 48-ball FBGA (8 × 9.5 × 1.2 mm) BA48J Package Outline, 51-85191



51-85191 *C

Acronyms

| Acronym | Description |
|------------------------|---|
| $\overline{\text{CE}}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| FPBGA | fine-pitch ball grid array |
| I/O | input/output |
| $\overline{\text{OE}}$ | output enable |
| SRAM | static random access memory |
| TTL | transistor-transistor logic |
| $\overline{\text{WE}}$ | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

Document History Page

| Document Title: CY7C1071DV33, 32-Mbit (2 M × 16) Static RAM | | | | |
|---|---------|-----------------|-----------------|---|
| Document Number: 001-12063 | | | | |
| REV. | ECN NO. | Submission Date | Orig. of Change | Description of Change |
| ** | 605460 | See ECN | VKN | New Data sheet |
| *A | 1192183 | See ECN | VKN / KKVTMP | Removed CE ₂ feature Updated block diagram Changed I _{CC} spec from 160 mA to 225 mA Changed C _{IN} spec from 8 pF to 10 pF Changed C _{OUT} spec from 10 pF to 12 pF Changed t _{BW} spec from 8 ns to 9 ns |
| *B | 2711136 | 05/29/2009 | VKN / PYRS | Added 10 ns speed bin In 12 ns speed bin, changed I _{SB1} from 70 to 60 mA and I _{SB2} from 60 to 50 mA Changed C _{IN} from 8 pF to 16 pF and C _{OUT} from 10 pF to 20 pF Changed Θ _{JA} from 28.37 °C/W to 24.72 °C/W Removed 119-Ball PBGA package Added 48-Ball FBGA package |
| *C | 2759408 | 09/03/2009 | VKN / AESA | Removed 10ns speed Marked thermal specs as "TBD" Changed t _{DOE} , t _{HZOE} , t _{HZCE} , t _{DBE} , t _{HZBE} , t _{HZWE} specs from 6 ns to 7ns Added -12B2XI part (Dual CE option) |
| *D | 2813370 | 11/23/2009 | VKN | Changed I _{CC} spec from 225 mA to 250 mA. |
| *E | 2925803 | 04/30/2010 | VKN / AESA | Converted from Preliminary to Final Removed Dual CE option from the data sheet Updated links in Sales , Solutions , and Legal Information |
| *F | 3109063 | 12/13/2010 | AJU | Added Ordering Code Definitions . |
| *G | 3132969 | 01/11/2011 | AJU | Added Acronyms and Units of Measure . Changed all instances of IO to I/O. Updated in new template. |
| *H | 3268861 | 05/28/2011 | AJU | Updated Functional Description (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). |
| *I | 3411360 | 10/17/2011 | TAVA | Updated Features . Updated DC Electrical Characteristics . Updated Switching Waveforms . Updated Package Diagram . |
| *J | 4573215 | 11/18/2014 | TAVA | Added related documentation hyperlink in page 1. Updated Figure 9 in Package Diagram (spec 51-85191 *B to *C). |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|--------------------------|--|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/Rf | cypress.com/go/wireless |

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2007-2014. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Cypress Semiconductor:

[CY7C1071DV33-12BAXI](#) [CY7C1071DV33-12BAXIT](#)