CY62138F MoBL®

2-Mbit (256 K × 8) Static RAM

Features

- High speed: 45 ns
- Wide voltage range: 4.5 V to 5.5 V
- Pin compatible with CY62138V
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 5 µA
- Ultra low active power
  - Typical active current: 1.6 mA @ f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin SOIC and 32-pin thin small outline package (TSOP) II packages

Functional Description

The CY62138F is a high performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW).

To write to the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{17}).

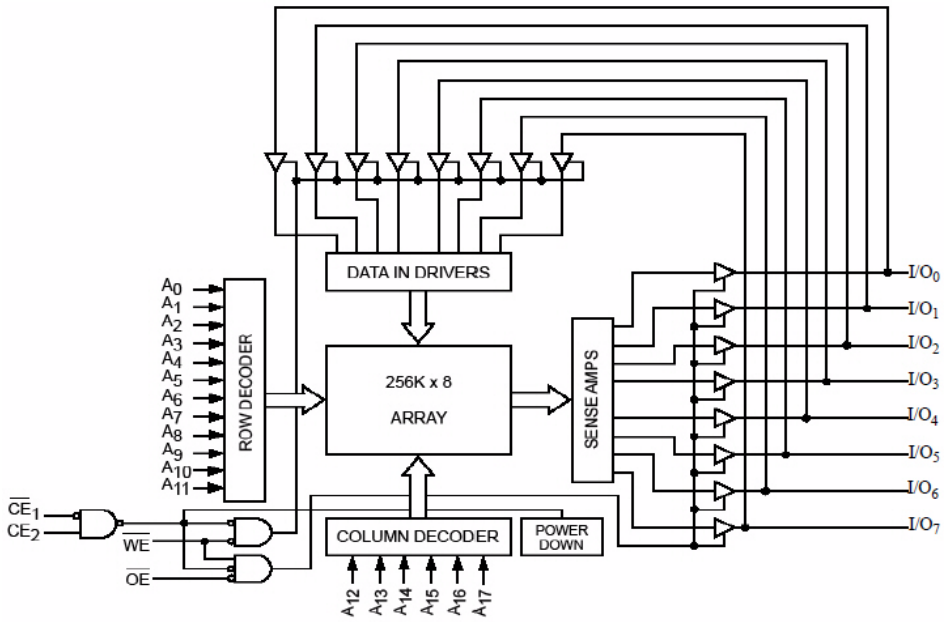
To read from the device, take Chip Enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and output enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

The CY62138F device is suitable for interfacing with processors that have TTL I/P levels. It is not suitable for processors that require CMOS I/P levels. Please see Electrical Characteristics on page 4 for more details and suggested alternatives.

For a complete list of related documentation, click here.

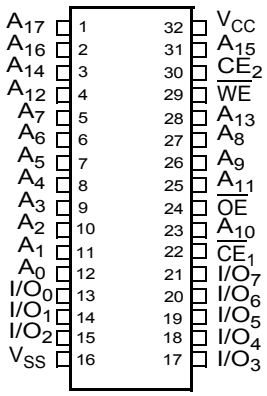
Logic Block



Contents

Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout (Top View)



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ [1]	Max		Typ [1]	Max	Typ [1]	Max	Typ [1]	Max
CY62138FLL	4.5 V	5.0 V	5.5 V	45	1.6	2.5	13	18	1	5

Note
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential ..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

DC voltage applied to outputs in High Z state [2, 3] ..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

DC Input Voltage [2, 3] ..... –0.5 V to 6.0 V (V_{CCmax} + 0.5 V)

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL–STD–883, Method 3015) ..... > 2001 V

Latch-up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [4]
CY62138FLL	Industrial	–40 °C to +85 °C	4.5 V to 5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns			Unit
				Min	Typ [5]	Max	
V_{OH}	Output HIGH voltage	V_{CC} = 4.5 V	I_{OH} = –1.0 mA	2.4	–	–	V
		V_{CC} = 5.5 V	I_{OH} = –0.1 mA	–	–	3.4 [6]	
V_{OL}	Output LOW voltage	I_{OL} = 2.1 mA		–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 4.5 V to 5.5 V		2.2	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage	V_{CC} = 4.5 V to 5.5 V		–0.5	–	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply Current	f = f_{max} = 1/t_{RC}	V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA, CMOS levels	–	13	18	mA
		f = 1 MHz		–	1.6	2.5	
I_{SB2} [7]	Automatic CE Power-down current CMOS inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2 V or CE_2 ≤ 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$		–	1	5	µA

Notes

2. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
3. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
4. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
6. Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5 V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note AN6081 for technical details and options you may consider.
7. Chip enables ($\overline{CE_1}$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

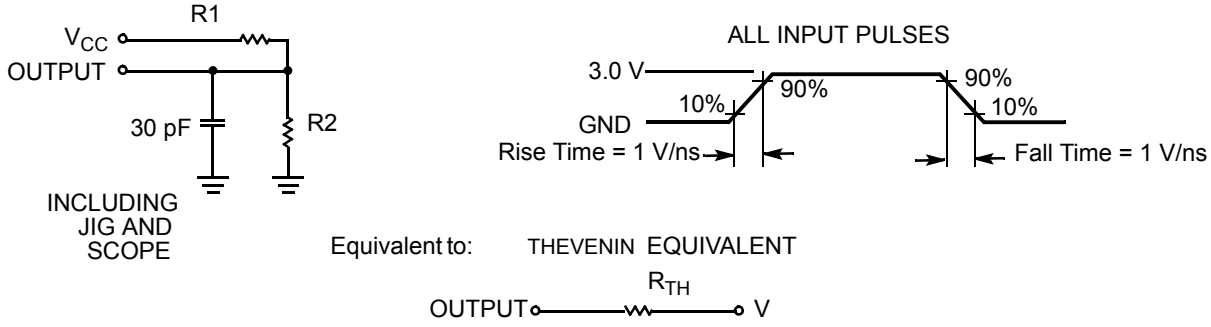
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	32-pin SOIC	32-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch two-layer printed circuit board	44.53	44.16	°C/W
Θ_{JC}	Thermal resistance (junction to case)		24.05	11.97	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	5.0 V	Unit
R1	1800	Ω
R2	990	Ω
R_{TH}	639	Ω
V_{TH}	1.77	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

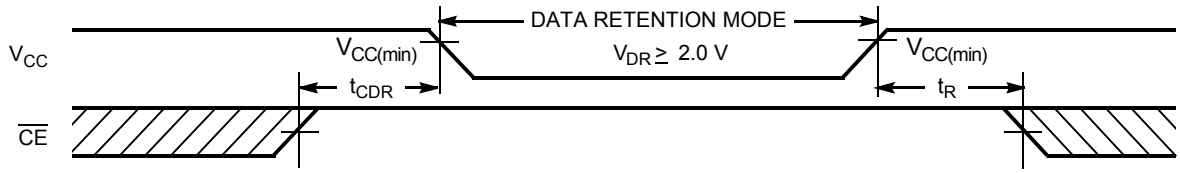
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for Data retention		2.0	–	–	V
I_{CCDR} [10]	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	1	5	µA
t_{CDR} [9]	Chip deselect to data retention time		0	–	–	ns
t_R [11]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform [12]



Notes

9. Tested initially and after any design or process changes that may affect these parameters. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
10. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
12. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Switching Characteristics

Over the Operating Range

Parameter [13, 14]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and $\overline{CE}_2$ HIGH to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [15]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [15, 16]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and $\overline{CE}_2$ HIGH to low Z [15]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH or $\overline{CE}_2$ LOW to high Z [15, 16]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and $\overline{CE}_2$ HIGH to power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH or $\overline{CE}_2$ LOW to power-down	–	45	ns
Write Cycle [17, 18]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and $\overline{CE}_2$ HIGH to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [15, 16]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [15]	10	–	ns

Notes

13. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Notes is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
17. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
18. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 4. Read Cycle 1 (Address Transition Controlled) [19, 20]

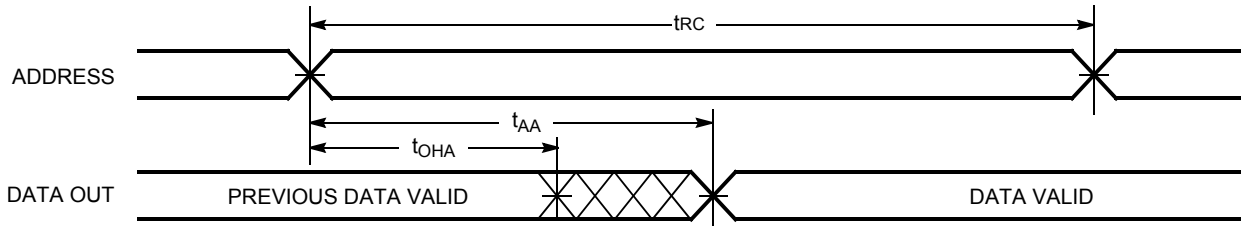
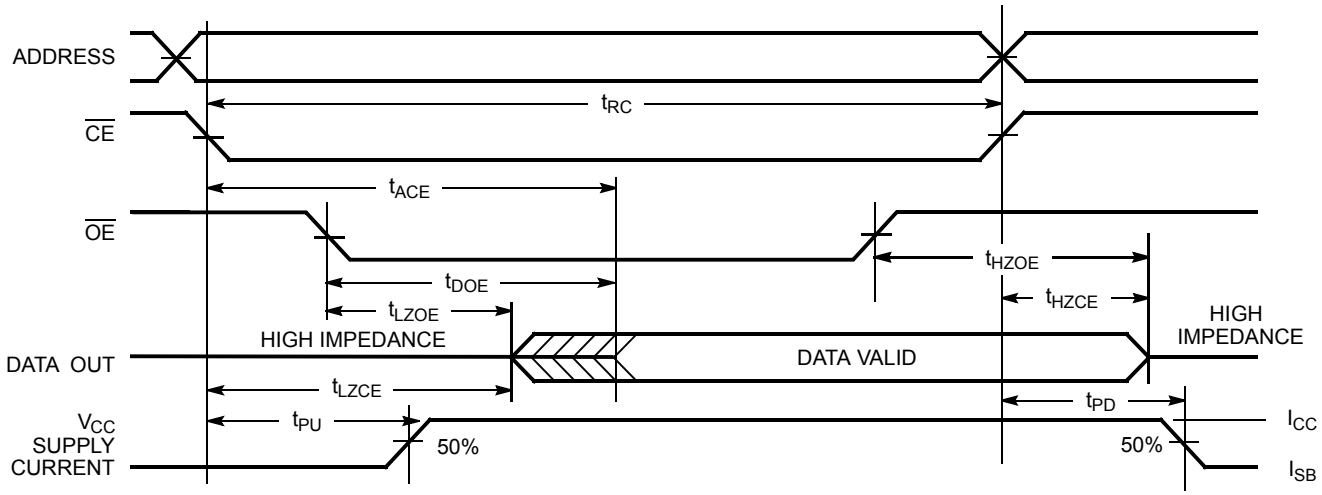


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [20, 21, 22]



Notes

19. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid before or similar to $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
22. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [23, 24, 25, 26]

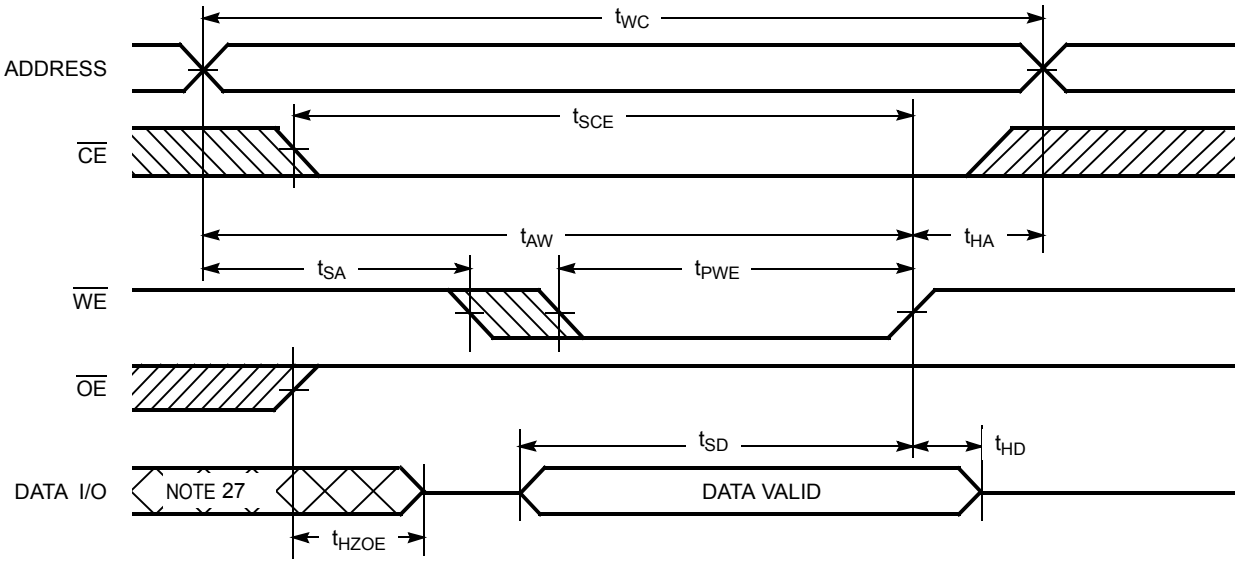
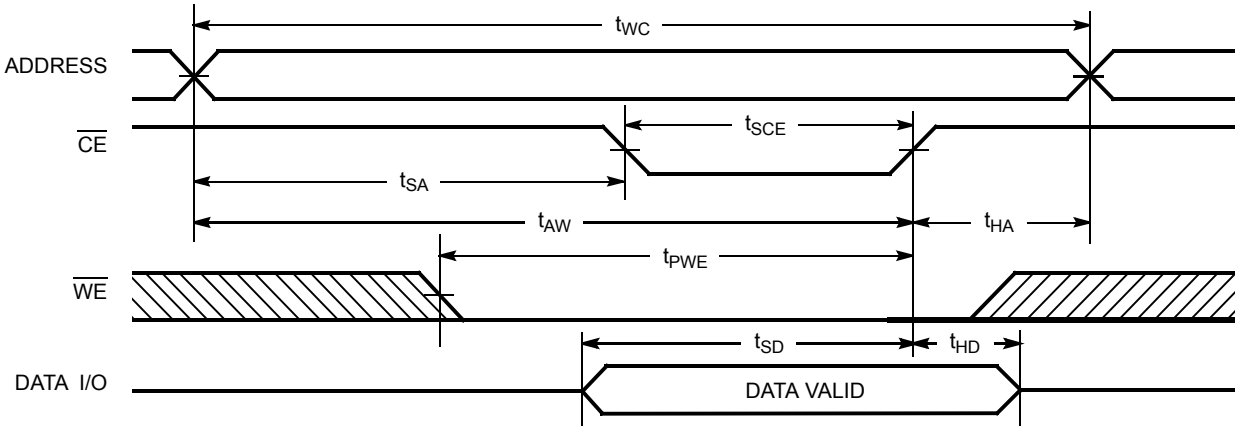


Figure 7. Write Cycle No. 2 ($\overline{CE_1}$ or $\overline{CE_2}$ Controlled) [23, 24, 25, 26]

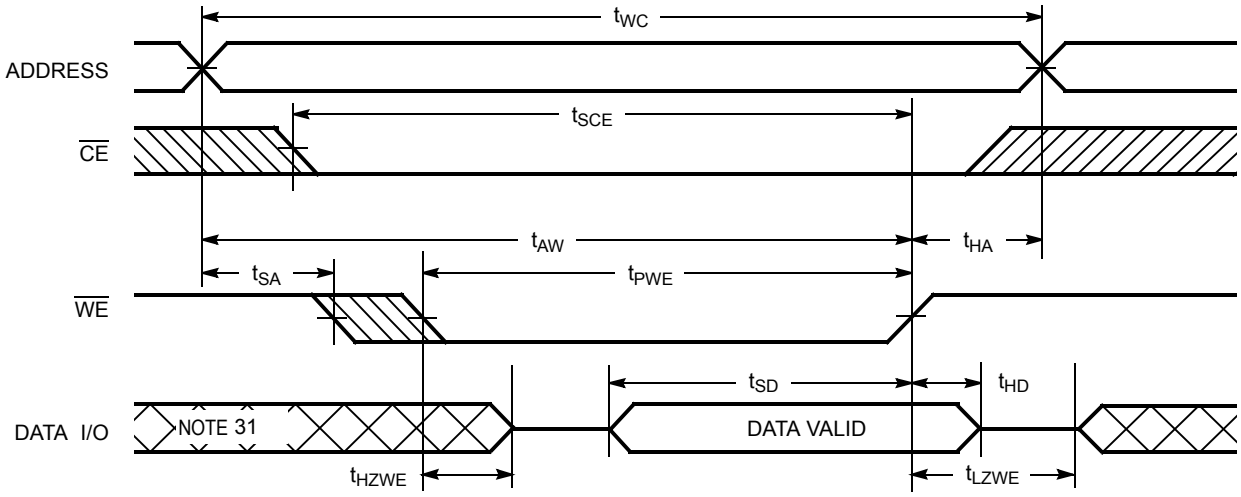


Notes

23. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
25. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
26. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
27. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [28, 29, 30]



Notes

28. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and $\overline{CE}_2$. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
29. If $\overline{CE}_1$ goes HIGH or $\overline{CE}_2$ goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
30. The minimum write cycle pulse width should be equal to the sum of t_{HZWE} and t_{SD}.
31. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X[32]	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X[32]	L	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data out	Read	Active (I_{CC})
L	H	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	X	Data in	Write	Active (I_{CC})

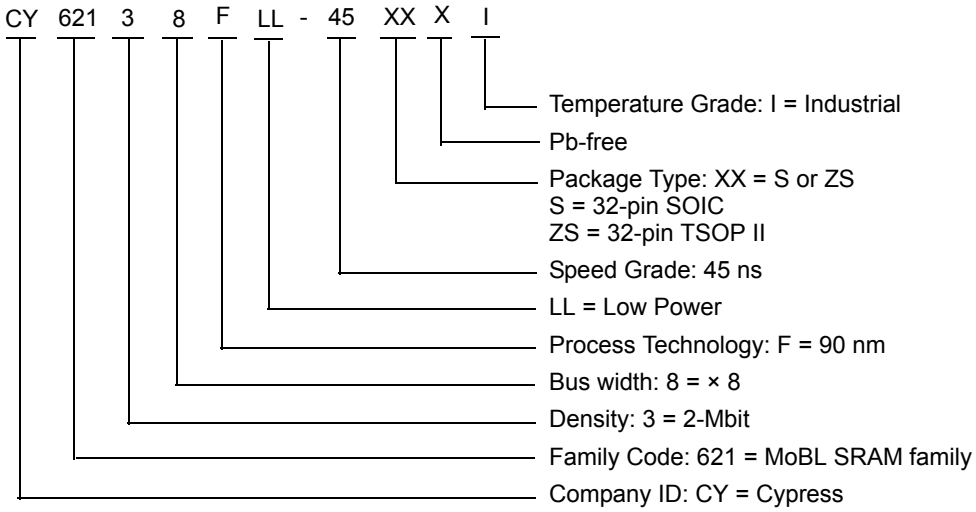
Note
32. The 'X' (Don't care) state for the Chip enables ($\overline{CE}_1$ and $\overline{CE}_2$) in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62138FLL-45SXI	51-85081	32-pin SOIC (Pb-free)	Industrial

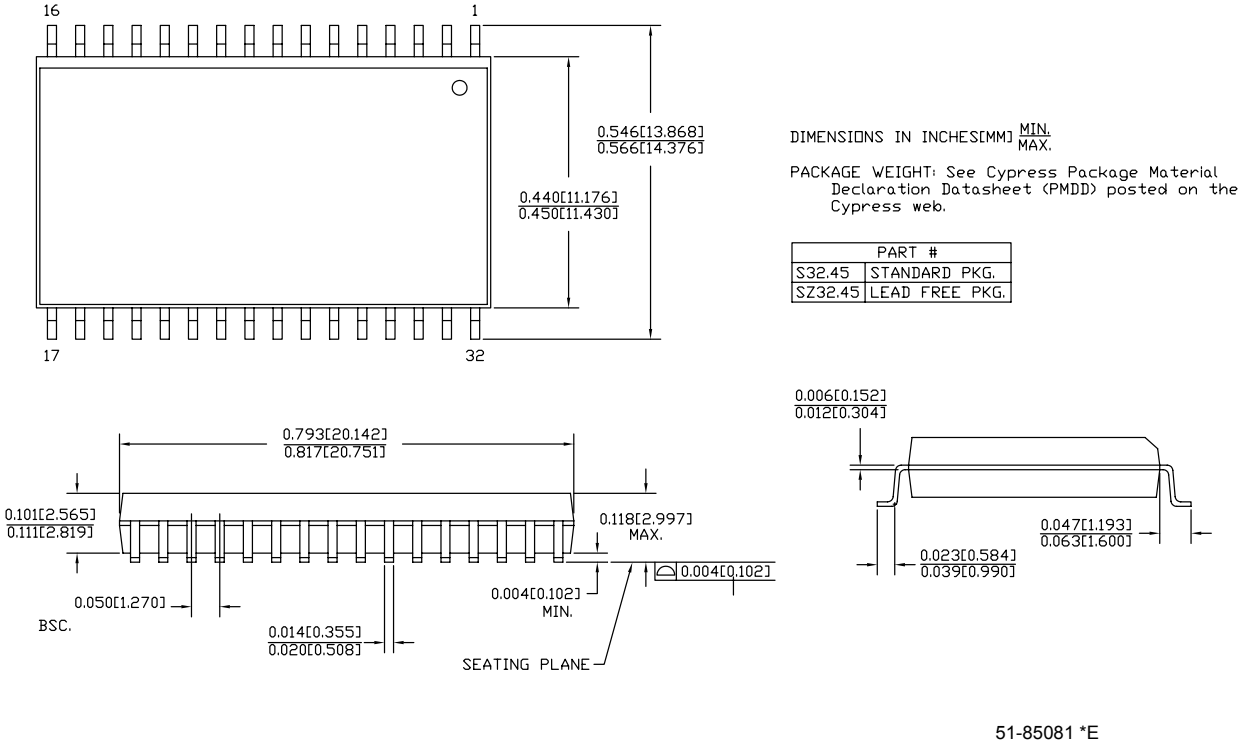
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



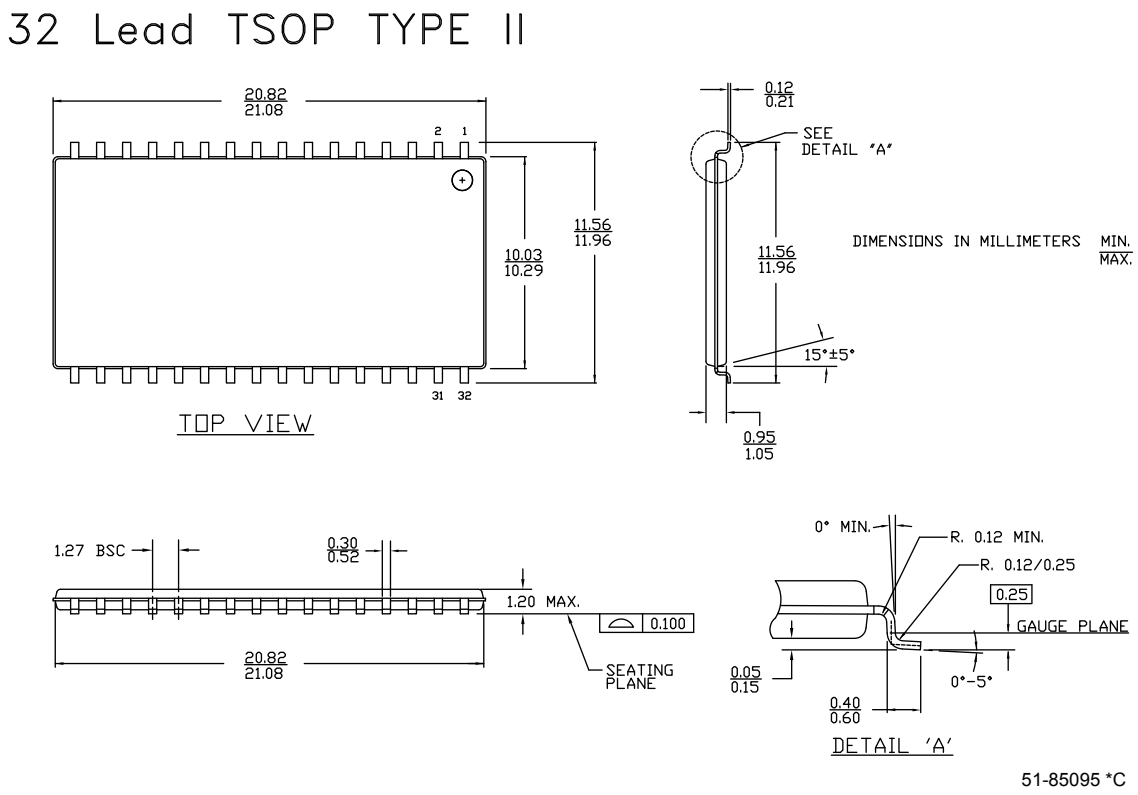
Package Diagrams

Figure 9. 32-pin SOIC (450 Mils) S32.45/SZ32.45 Package Outline, 51-85081



Package Diagrams (continued)

Figure 10. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Documents Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62138F MoBL®, 2-Mbit (256 K × 8) Static RAM Document Number: 001-13194				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	797956	See ECN	VKN	New data sheet.
*A	940341	See ECN	VKN	Added footnote #7 related to I_{SB2} and I_{CCDR}
*B	3055174	13/10/2010	RAME	Added Acronyms and Units of Measure. Added Ordering Code Definitions. Footnotes updated Updated Package Diagram Figure 9 and Figure 10. Updated as per new template
*C	3061313	15/10/2010	RAME	Minor change: Corrected “IO” to “I/O”
*D	3232735	04/18/2011	RAME	Removed the Note “For best practice recommendations, refer to the Cypress application note “System Design Guidelines” at http://www.cypress.com ” in page 1.
*E	3287636	06/20/2011	RAME	Updated Package Diagrams. Updated in new template.
*F	3846281	12/19/2012	TAVA	Updated Ordering Information (Updated part numbers). Updated Package Diagrams: spec 51-85081 – Changed revision from *C to *E.
*G	4013949	06/04/2013	MEMJ	Updated Functional Description. Updated Electrical Characteristics: Added one more Test Condition “V_{CC} = 5.5 V, I_{OH} = –0.1 mA” for V_{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 6 and referred the same note in maximum value for V_{OH} parameter corresponding to Test Condition “V_{CC} = 5.5 V, I_{OH} = –0.1 mA”.
*H	4099045	08/19/2013	VINI	Updated Switching Characteristics: Added Note 13 and referred the same note in “Parameter” column. Updated in new template.
*I	4380445	05/15/2014	NILE	Updated Switching Characteristics: Added Note 18 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 30 and referred the same note in Figure 8. Completing Sunset Review.
*J	4578447	01/16/2015	NILE	Added related documentation hyperlink in page 1. Updated Figure 10 in Package Diagrams (spec 51-85095 *B to *C).

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