

## Features

- RoHS compliant\*
- Low capacitance - 0.02 pF (I/O to I/O)
- ESD protection to IEC 61000-4-2 (Level 4)

## Applications

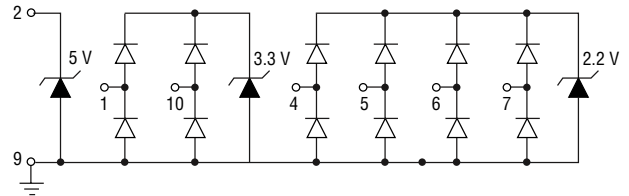
- USB 3.1
- USB 3.0

# CDDFN10-0516P - Surface Mount TVS Diode Array

## General Information

The CDDFN10-0516P device provides ESD protection for high-speed data ports, meeting IEC 61000-4-2 (Level 4) requirements. The Transient Voltage Suppressor array, protecting up to six data lines, offers Working Peak Reverse Voltages of 5 V (one line), 3.3 V (two lines) and 2.2 V (four lines) compatible with USB 3.1.

The DFN10 packaged device has an ultra-low typical capacitance of only 0.02 pF between I/O lines. This allows it to be used for protecting sensitive components used on high-speed interfaces. The small footprint of the device allows for flow-through routing on the PCB, helping to maintain matched impedances of the high-speed data lines.



## Absolute Maximum Ratings (@ T<sub>A</sub> = 25 °C Unless Otherwise Noted)

Parameter	Symbol	CDDFN10-0516P	Unit
Peak Pulse Current (t <sub>p</sub> = 8/20 μS) (1)	I <sub>pp</sub>	4	A
ESD (per IEC 61000-4-2 Contact)		10	kV
ESD (per IEC 61000-4-2 Air)		15	kV
Operating Temperature	T <sub>J</sub>	-40 to +85	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

## Electrical Characteristics (@ T<sub>A</sub> = 25 °C Unless Otherwise Noted)

Pin 2 (V <sub>BUS</sub> ) to Ground					
Parameter	Symbol	Min.	Typ.	Max.	Unit
Working Peak Reverse Voltage	V <sub>WM_BUS</sub>			5	V
Breakdown Voltage @ 1 mA	V <sub>BR_BUS</sub>	6			V
Snap-back Voltage @ 50 mA	V <sub>SB_BUS</sub>	5.5			V
Leakage Current @ V <sub>WM_BUS</sub>	I <sub>R_BUS</sub>			2.5	μA
Clamping Voltage @ I <sub>pp</sub> = 4 A	V <sub>C_BUS</sub>		6.5		V
Channel Capacitance @ 0 V, 1 MHz	C <sub>IN_BUS</sub>		17	22	pF
Pin 1 or 10 (D+, D-) to Ground (Unless Otherwise Noted)					
Parameter	Symbol	Min.	Typ.	Max.	Unit
Working Peak Reverse Voltage	V <sub>WM_USB</sub>			3.3	V
Breakdown Voltage @ 1 mA	V <sub>BR_USB</sub>	4.5			V
Snap-back Voltage @ 50 mA	V <sub>SB_USB</sub>	3.6			V
Leakage Current @ V <sub>WM_USB</sub>	I <sub>R_USB</sub>			1	μA
Forward Voltage @ 15 mA	V <sub>F_USB</sub>		0.9		V
Clamping Voltage @ I <sub>pp</sub> = 4 A	V <sub>C_USB</sub>		7.2		V
Channel Capacitance @ 1.65 V, 1 MHz	C <sub>IN_USB</sub>		0.35	0.5	pF
Channel to Channel Capacitance @ 1.65 V, 1 MHz (2) (3)	C <sub>CROSS_USB</sub>		0.02	0.04	pF

Note 1: Pin 2 (V<sub>BUS</sub>) to Ground

Note 2: Between Pins 1 and 10 (D+ to D-)

Note 3: Pin 9 = 0 V

(Continued on next page)

\*RoHS Directive 2002/95/EC Jan. 27, 2003 including annex and RoHS Recast 2011/65/EU June 8, 2011. Specifications are subject to change without notice.

The device characteristics and parameters in this data sheet can and do vary in different applications and actual device performance may vary over time. Users should verify actual device performance in their specific applications.

**CDDFN10-0516P - Surface Mount TVS Diode Array****BOURNS®****Electrical Characteristics - Continued (@ T<sub>A</sub> = 25 °C Unless Otherwise Noted)**

<b>Pin 4, 5, 6 or 7 (SSTX+, SSRX+, SSTX-, SSRX-) to Ground (Unless Otherwise Noted)</b>					
<b>Parameter</b>	<b>Symbol</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>
Working Peak Reverse Voltage	V <sub>WM_SS</sub>			2.2	V
Breakdown Voltage @ 1 mA	V <sub>BR_SS</sub>	4.5			V
Snap-back Voltage @ 50 mA	V <sub>SB_SS</sub>	2.4			V
Leakage Current @ V <sub>WM_SS</sub>	I <sub>R_SS</sub>			1	μA
Forward Voltage @ 15 mA	V <sub>F_SS</sub>		0.9		V
Clamping Voltage @ I <sub>PP</sub> = 4 A	V <sub>C_SS</sub>		4.5		V
Channel Capacitance @ 1.2 V, 1 MHz	C <sub>IN_SS</sub>		0.35	0.5	pF
Channel to Channel Capacitance @ 1.2 V, 1 MHz (3) (4)	C <sub>CROSS_SS</sub>		0.02	0.04	pF

Note 3: Pin 9 = 0 V

Note 4: Between any two I/O; Pins 4, 5, 6 or 7 (SSTX+, SSRX+, SSTX-, SSRX-)

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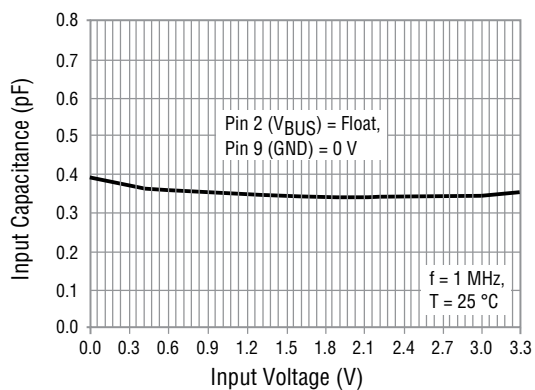
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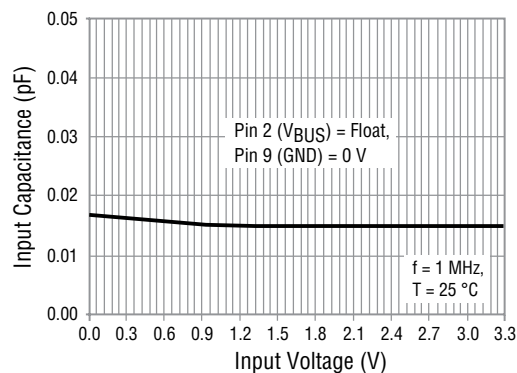
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## Performance Curves

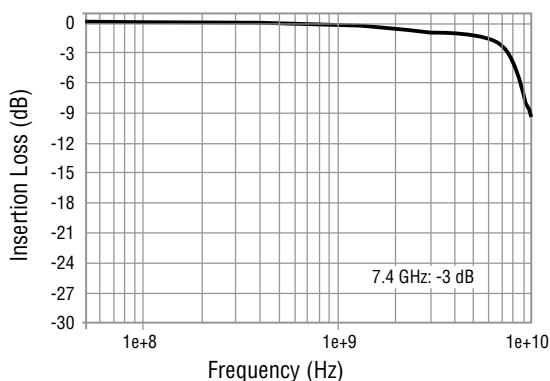
### Typical Voltage vs. Capacitance $C_{IN}$ (4)



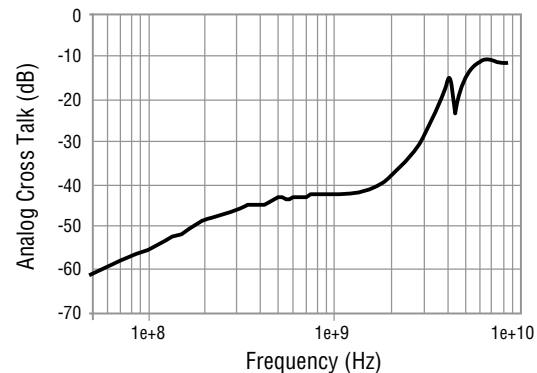
### Typical Voltage vs. Capacitance $C_{CROSS}$ (5)



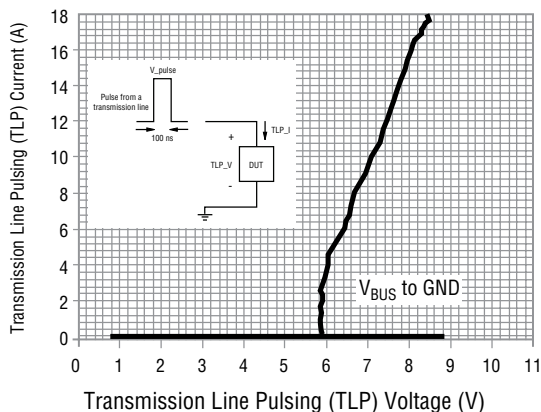
### Typical Insertion Loss $S_{21}$ (4)



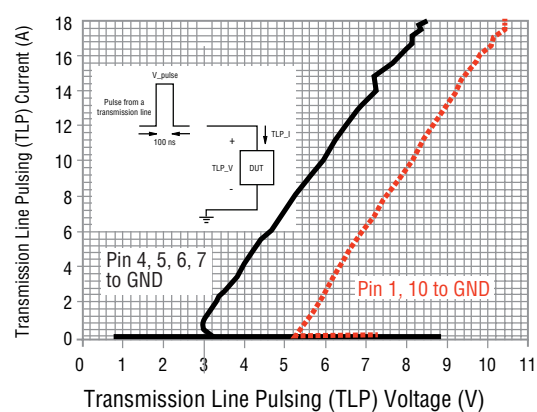
### Typical Analog Cross Talk (5)



### Typical Transmission Line Pulsing (TLP)



### Typical Transmission Line Pulsing (TLP)



Note 4: Any I/O Pin (1, 10, 4, 5, 6, or 7) to Ground (D+, D-, SSTX+, SSRX+, SSTX-, SSRX-)

Note 5: Between any two I/O Pins (1, 10, 4, 5, 6, or 7) (D+, D-, SSTX+, SSRX+, SSTX-, SSRX-)

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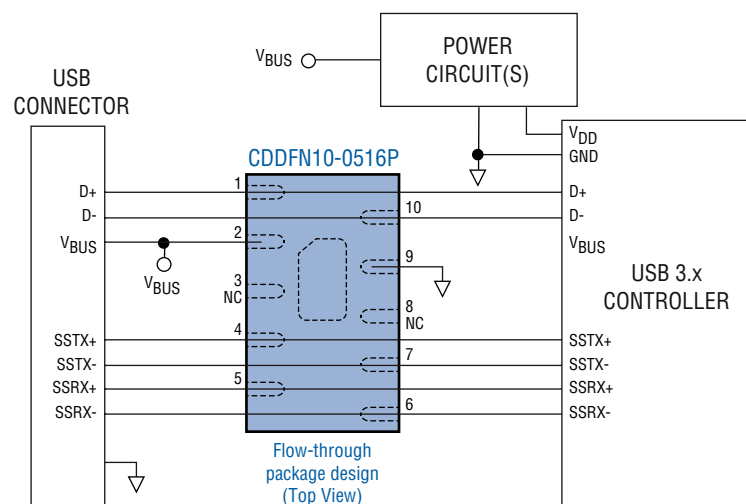
# CDDFN10-0516P - Surface Mount TVS Diode Array

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## Applications Information

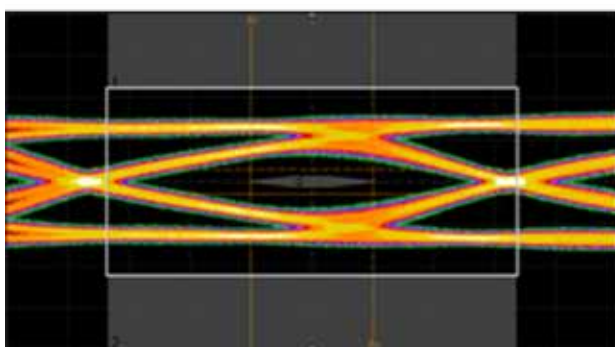
The Model CDDFN10-0516P was designed to provide ESD and surge protection for USB 3.0 and USB 3.1 applications. USB 3.x controller ICs typically have device level ESD ratings of about 2 kV per ANSI/ESDA/JEDEC JS-001-2010, to prevent ESD damage in a manufacturing environment. For this ANSI/ESDA/JEDEC JS-001-2010 test, a 100 pF capacitor is discharged into the device input through a 1500 ohm resistor. A system level ESD requirement is, however, typically specified to IEC 61000-4-2, which is more stringent than JESD22-A114F requirements. The IEC 61000-4-2 test discharges a 150 pF capacitor through a 330 ohm resistor. The CDDFN10-0516P is designed to enable a USB3.x controller IC to meet system ESD levels as high as 10 kV (contact test) per the IEC 61000-4-2 Standard. The device also provides up to 4 A (8/20  $\mu$ S) of surge protection on the 5 V  $V_{BUS}$  line per IEC 61000-4-5.

The Bourns® Model CDDFN10-0516P provides protection for six signal lines and a 5 V power bus. Its ultra-low capacitance minimizes signal distortion on USB 3.1 super-speed data lines with 10 Gbps data rates. The figure below shows the connection diagram for one part of a USB 3.x application. USB 3.1 provides three voltage/current options for bus power: 5 V @ up to 2 A, 12 V @ up to 5 A and 20 V @ up to 5 A. The  $V_{BUS}$  line should only be connected to Pin 2 of the CDDFN10-0516P device if the bus voltage is limited to the 5 V option. In cases where the bus voltage is 12 V or 20 V, a separate device is required to protect the  $V_{BUS}$  line.



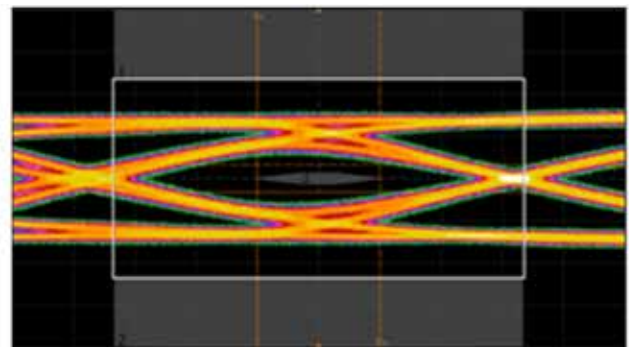
The flow-through package design of the Model CDDFN10-0516P simplifies signal routing on the printed circuit board. This minimizes the effect of the device connection on the signal line impedance and on system performance. The 10 Gbps eye diagrams below show that the loading of Pins 4 through 7 has a minimal impact on the performance of the USB 3.1 super-speed data lines.

**Performance Without Protection**



-15 ps 0 +15 ps

**Performance With Protection**



-15 ps 0 +15 ps

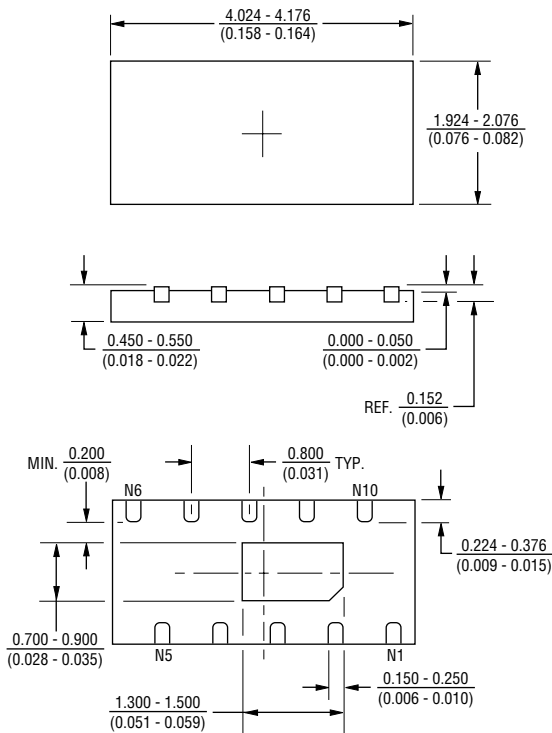
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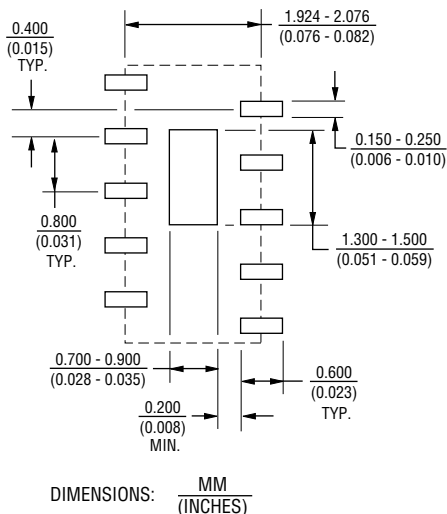


## Product Dimensions

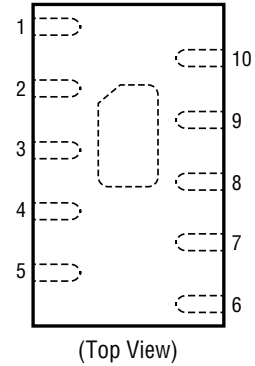
This is a molded DFN10 package with lead free 100 % Matte Sn on the lead frame. It has a flammability rating of UL 94V-0.



## Recommended Footprint



## Device Pinout

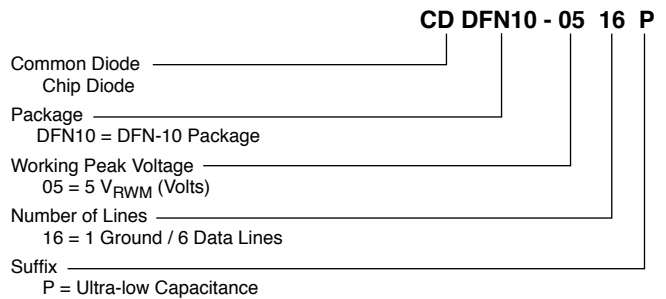


Pin	Function
1, 10	D+, D- (USB Differential Pair)
2	VBUS
3, 8	N.C.
4, 5, 6, 7	SSTX+, SSTX-, SSRX+, SSRX- (Super-Speed Pairs)
9	Ground
Center Pad	Ground

## Typical Part Marking

CDDFN10-0516P .....516

## How to Order



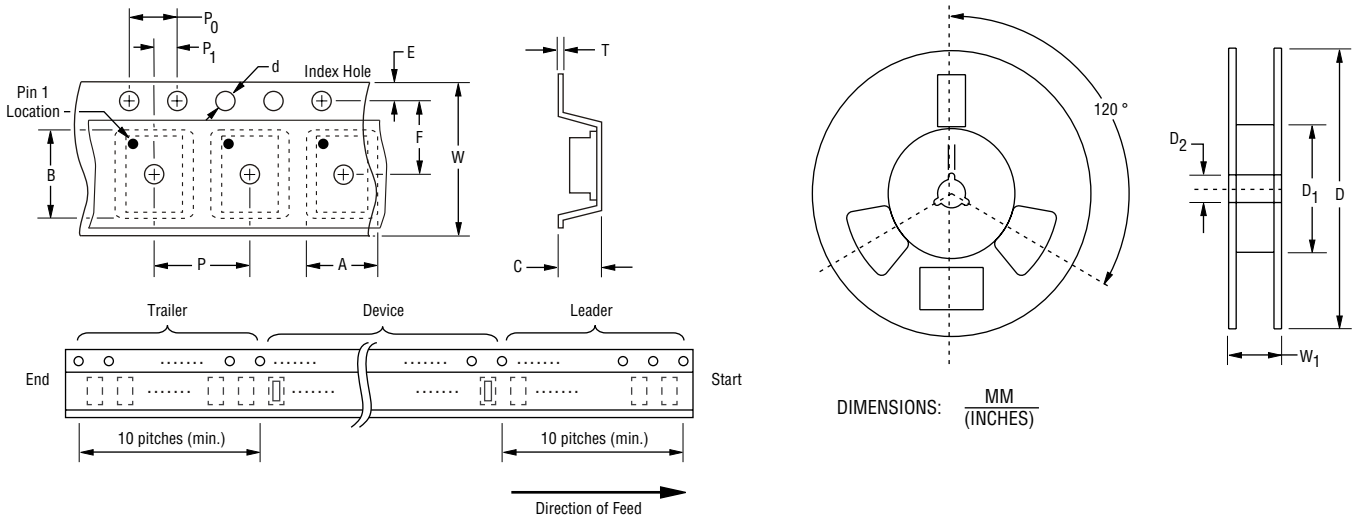
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## Packaging Information

The product is packaged in an 8 mm x 4 mm tape and reel format per EIA-481-A standard.



Item	Symbol	DFN-10
Carrier Width	A	$\frac{2.21 \pm 0.05}{(0.087 \pm 0.002)}$
Carrier Length	B	$\frac{4.22 +0.05/-0.04}{(0.166 +0.002/-0.002)}$
Carrier Depth	C	$\frac{0.81 \pm 0.05}{(0.032 \pm 0.002)}$
Sprocket Hole	d	$\frac{1.50 +0.1/-0}{(0.059 +0.004/-0)}$
Reel Outside Diameter	D	$\frac{180 \pm 3}{(7.087 \pm .118)}$
Reel Inner Diameter	D <sub>1</sub>	$\frac{50.0}{(1.969)}$ MIN.
Feed Hole Diameter	D <sub>2</sub>	$\frac{13.0 +0.5/-0.2}{(0.512 +0.020/-0.008)}$
Sprocket Hole Position	E	$\frac{1.75 \pm 0.10}{(0.069 \pm 0.004)}$
Punch Hole Position	F	$\frac{5.50 \pm 0.05}{(0.217 \pm 0.002)}$
Punch Hole Pitch	P	$\frac{4.00 \pm 0.10}{(0.157 \pm 0.004)}$
Sprocket Hole Pitch	P <sub>0</sub>	$\frac{4.00 \pm 0.10}{(0.157 \pm 0.004)}$
Embossment Center	P <sub>1</sub>	$\frac{2.00 \pm 0.05}{(0.079 \pm 0.002)}$
Overall Tape Thickness	T	$\frac{0.6}{(0.024)}$ MAX.
Tape Width	W	$\frac{12.3}{(0.484)}$ MAX.
Reel Width	W <sub>1</sub>	$\frac{18.4}{(0.724)}$ MAX.
Quantity per Reel	--	3000

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