HMC6301BG46

v00.0716

MILLIMETERWAVE RECEIVER 57 GHz - 64 GHz

Features

Frequency Band: 57 - 64 GHz

RF Signal Bandwidth: up to 1.8 GHz

Noise Figure: 8 dB typical

Receiver Gain: 0 - 70 dB

Digital and Analog RF and IF Gain Control

Programmable Baseband Gain and Filter Bandwidth

Integrated Frequency Synthesizer

Integrated Image Reject Filter

Partially External Loop Filter

Support for External LO

On-chip Temperature Sensor

Support for 256-QAM Modulation

Integrated AM and FM Detectors

Universal Analog I/Q Baseband Interface

Three Wire Serial Digital Interface

75-Ball RoHS Compliant Wafer Level Ball Grid Array

Typical Applications

- Small Cell Backhaul
- 60 GHz ISM Band Data Transfer
- Multi-Gb/s Data Communication
- WiGig/802.11ad Radio
- High Definition Video Transmission
- Radar / High Resolution Imaging

General Description

The HMC6301BG46 is a complete MillimeterWave receiver integrated circuit in a 6 mm X 4 mm RoHS compliant wafer level ball grid array (WLBGA) package which includes a low noise amplifier (LNA), an image reject filter, an RF to IF downconverter, an IF filter, an I/Q downconverter, and a frequency synthesizer. The receiver operates from 57 GHz to 64 GHz with up to 1.8 GHz of double-sided modulation BW. An integrated synthesizer provides tuning in 250, 500 or 540 MHz steps with excellent phase noise to support up to 64-QAM modulation. Optionally, an external LO can be injected allowing for user selectable LO characteristics or phase coherent transmit and receive operation as well as modulation to 256-QAM. Support for a wide variety of modulation formats is provided through a universal analog baseband IQ interface. The receiver device also contains AM and FM detectors to demodulate OOK, FSK or MSK modulation for lower cost and lower power serial data links without the need for high speed data converters. Gain control is provided in the RF, IF and baseband stages and a low 8 dB typical noise figure is supported at maximum gain. Together with the HMC6300BG46 transmitter, a complete 60 GHz transmit/receive chipset is provided for multi-Gb/s operation in the unlicensed 60 GHz ISM band.

Functional Diagram

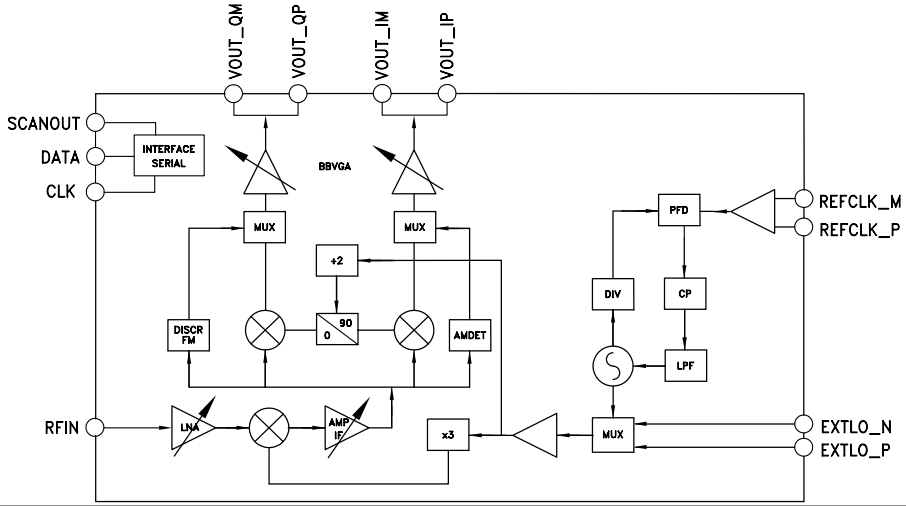

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Table 1. Electrical Specifications, TA = +25° C, See Test Conditions

Parameter	Condition	Min.	Typ.	Max.	Units
Frequency Range		57		64	GHz
Frequency Step Size	With 71.4286 MHz Ref Clk		250		MHz
Frequency Step Size	With 142.857 MHz Ref Clk		500		MHz
Frequency Step Size	With 154.2857 MHz Ref Clk		540		MHz
Modulation Bandwidth	Max BW setting, 3 dB BW Max BW setting, 5 dB BW		1.4 1.8		GHz
Receiver Gain		63	69		dB
Baseband Gain Control Range			41		dB
IF Gain Control Range (analog/digital)			12/15		dB
LNA Gain Control Range (analog/digital)			20/20		dB
Noise Figure	At Max Gain		8	13.5	dB
Input Power for 1dB Compression (P1dB)	Min LNA Gain		-19		dBm
Input Third-Order Intercept (IIP3)	Min LNA Gain		-9		dBm
Temperature Sensor Range	Four levels	-40		+85	˚C
Image Rejection (3 x LO-IF)			>35		dBc
Sideband Suppression (I/Q balance)		20	23		dBc
Phase Noise @ 100 kHz Offset			-75		dBc/Hz
Phase Noise @ 1 MHz Offset			-93		dBc/Hz
Phase Noise @ 10 MHz Offset			-114		dBc/Hz
Phase Noise @ 100 MHz Offset			-122		dBc/Hz
PLL Loop BW	Internal		300		kHz
Power Dissipation (single ended)			0.82		W
Power Dissipation (ext. LO)			0.57		W

Table 2. Test Conditions (unless otherwise Stated)

Description	Condition
Reference Frequency	71.4286 MHz
Temperature	+25˚C
Gain Settings	Max
IF Bandwidth	Max
Input Impedance	50Ω single ended
Output Impedance	100Ω differential

Table 3. Recommended Operation Conditions

Description	Mnemonic	Min.	Typ.	Max.	Units
POWER SUPPLY	VCC_{BUF}	2.565	2.7	2.835	V
	VCC_{LNA}	2.565	2.7	2.835	V
	VCC_{TRIP}	2.565	2.7	2.835	V
	VCC_{DIV}	2.565	2.7	2.835	V
	VCC_{VCO}	2.565	2.7	2.835	V
	VCC_{IF}	2.565	2.7	2.835	V
	VCC_{MIX}	2.565	2.7	2.835	V
	VDD_{SYN}	1.3	1.35	1.48	V
	VDD_{D}	1.3	1.35	1.48	V
INPUT VOLTAGE RANGE					
Serial Digital Interface -Logic High	DATA	0.9	1.2	1.4	V
	ENABLE	0.9	1.2	1.4	V
	CLK	0.9	1.2	1.4	V
	RESET	0.9	1.2	1.4	V
Serial Digital Interface – Logic Low	DATA	-0.05	0.1	0.3	V
	ENABLE	-0.05	0.1	0.3	V
	CLK	-0.05	0.1	0.3	V
	RESET	-0.05	0.1	0.3	V
Reference Clock	REFCLK_P		3.3 or 2.5V LVPECL/LVDS 1.2V CMOS		V
	REFCLK_K				
Baseband I & Q	BB_{IM}	10	50	200	mVp-p
	BB_{IP}	10	50	200	mVp-p
	BB_{QM}	10	50	200	mVp-p
	BB_{QP}	10	50	200	mVp-p
Baseband I & Q Common Mode	BB_{IM}		1.3		V
	BB_{IP}		1.3		V
	BB_{QM}		1.3		V
	BB_{QP}		1.3		V
Analog Gain Control	$AnaCtrl_{LNA}$	0.1		2.0	V
	$AnaCtrl_{IFVGA}$	0.1		2.25	V
EXTERNAL LO	EXTLO_P	0	+3	+6	dBm
	EXTLO_N	0	+3	+6	dBm
BASEBAND TEMPERATURE		-40		+85	°C
DRAIN CURRENT					
1.35 V			<1		mA
2.7 V			300		mA

Table 4. Power Consumption

Voltage (V)	Mnemonic	Typical Current (mA)	Typical power Consumption (mW)
2.7	VCC_{BUF}	70	189
2.7	VCC_{LNA}	15	41
2.7	VCC_{TRIP}	54	146
2.7	VCC_{DIV}	46	124
2.7	VCC_{VCO}	52	140
2.7	VCC_{IF}	30	81
2.7	VCC_{MIX}	32	86
1.35	VDD_{SYN}	0.08	0.1
1.35	VDD_{D}	10	13

Figure 1. Maximum Gain vs. Frequency over Temperature [1]

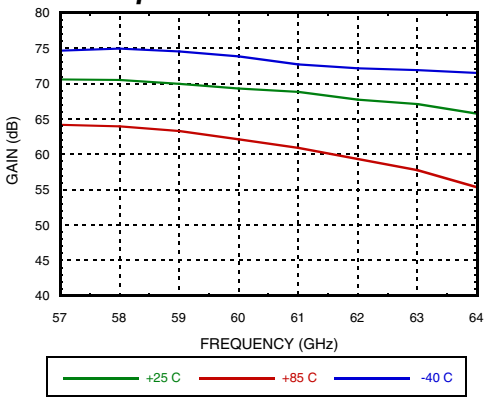


Figure 2. LNA Attenuation vs. Analog Control Voltage over Temperature [2][3]

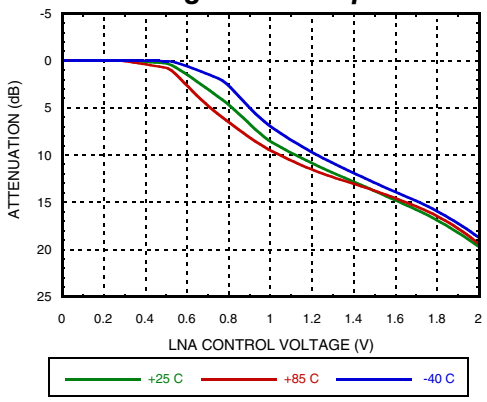


Figure 3. LNA Attenuation vs. Digital Setting over Temperature [2][3]

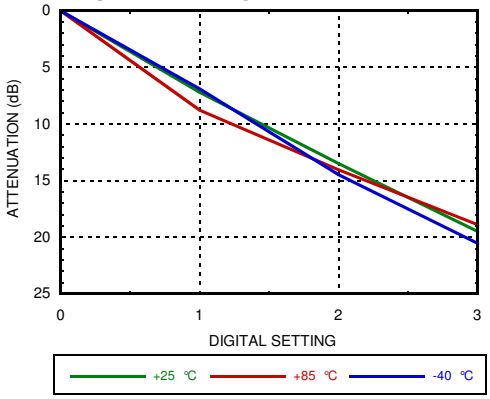


Figure 4. RF Return Loss vs. Frequency

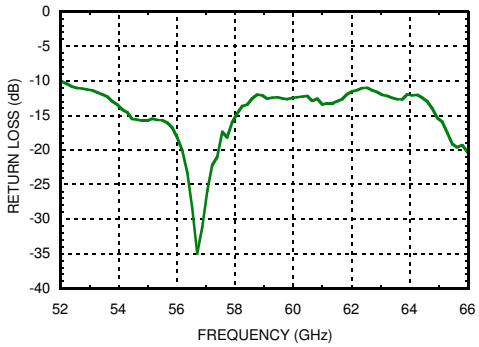


Figure 5. IF Attenuation vs. Analog Control Voltage over Temperature [2][4]

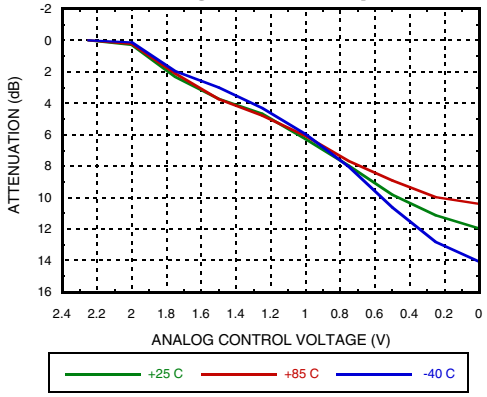
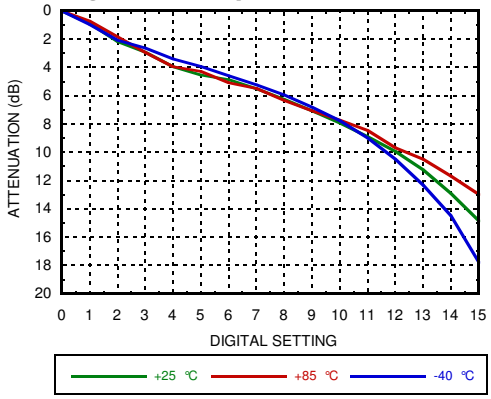


Figure 6. IF Attenuation vs. Digital Setting over Temperature [2][4]



[1] IF and RF attenuation = 0 dBm
[2] Measurement taken at 60 GHz
[3] IF attenuation = 0 dBm
[4] RF attenuation = 0 dBm

Figure 7. Baseband Attenuation vs. Frequency Over Temperature [1]

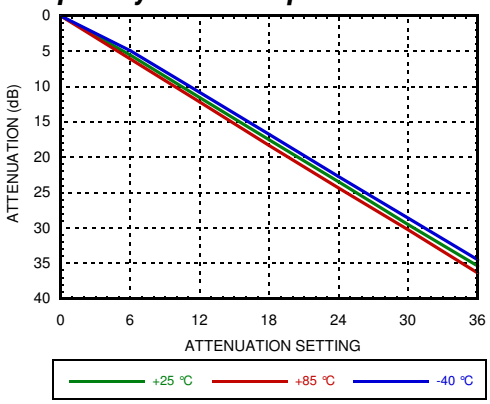


Figure 8. Input IP3 vs. Frequency over Temperature, Minimum LNA Gain [3]

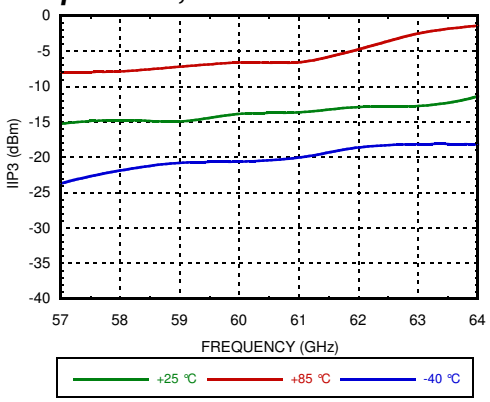


Figure 9. Input IP3 vs. Frequency over Temperature, Maximum LNA Gain [3]

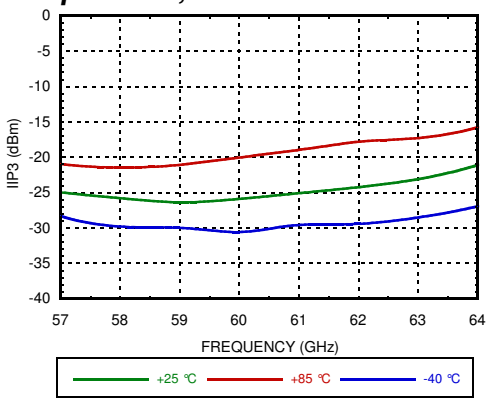


Figure 10. Sideband Suppression vs. Frequency over Temperature [2]

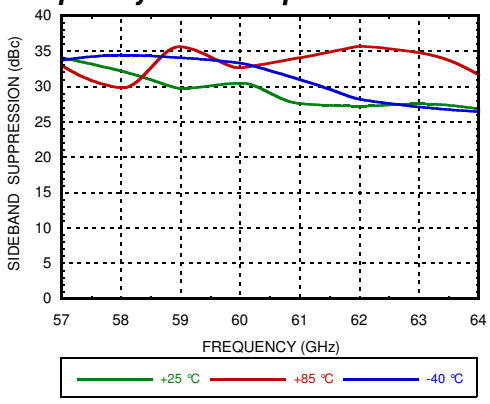


Figure 11. Noise Figure vs. Frequency over Temperature

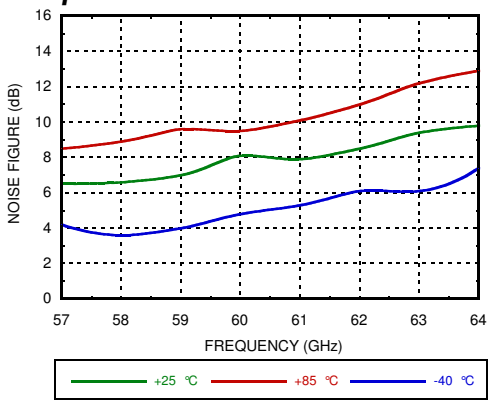
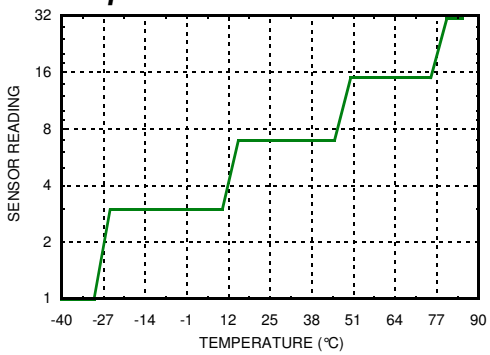


Figure 12. Temperature Sensor Reading vs. Temperature



[1] Measurement taken at 60 GHz
[2] Measurement taken at maximum gain
[3] Measurement taken at maximum IF gain and maximum baseband attenuation

Figure 13. Phase Noise vs. Frequency Offset over Temperature, Internal LO [1]

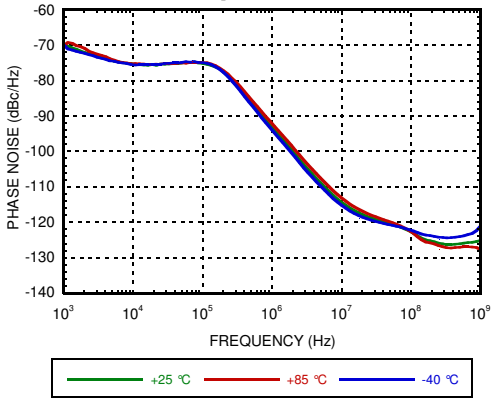
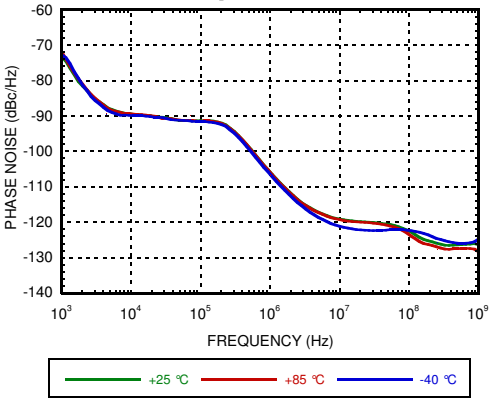


Figure 14. Phase Noise vs. Frequency Offset over Temperature, External LO [1]



[1] Measurement taken at 60 GHz and nominal bias

Table 5. Absolute Maximum Ratings

VCC_{BUF}	2.85 V
VCC_{LNA}	2.85 V
VCC_{TRIP}	2.85 V
VCC_{DIV}	2.85 V
VCC_{VCO}	2.85 V
VCC_{IF}	2.85 V
VCC_{MIX}	2.85 V
VDD_{SYN}	1.6 V
VDD_{D}	1.6 V
Serial Digital Interface Input Voltage	1.5 V
Baseband Outputs (BB, FM)	0.75 Vp-p
RF Input Power	0 dBm
External LO Power	10 dBm
Thermal Resistance (R_{TH}), Junction to Ground Paddle	8.23 °C/W
Storage Temperature	-55°C to 150°C
Operating Temperature	-40°C to 85°C
Reflow Temperature	260°C
ESD Sensitivity, Charged Device Model (CDM)	Class C3 (250 V)

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Figure 15. Outline Drawing

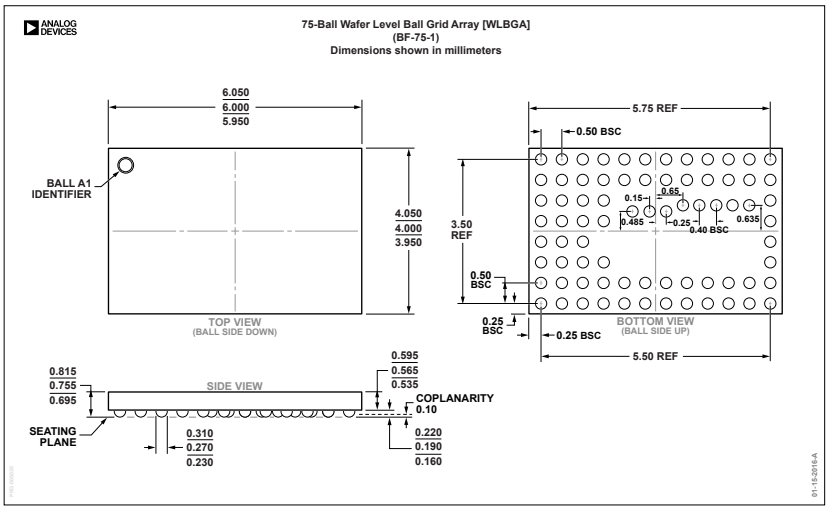


Table 6. Package Information

Part Number	Chip Bump Composition	MSL Rating [3]	Package Marking [1] [2]
HMC6301BG46	96.5 Tin (Sn), 3.0 Silver (Ag), 0.5 Copper (Cu)	MSL1	HMC6301BG46 TX BBFZ #YYWW XXX XXXXX-XX

[1] Pb-free, year and week number, #YYWW
[2] Assembly Lot number, XXX XXXXXX-XX
[3] Max peak reflow temperature of 260 °C; The peak reflow temperature should not exceed the maximum temperature for which the package is qualified according to the moisture sensitivity level (MSL1)

Table 7. Pin Descriptions

Pin Number	Mnemonic	Description
A1	CLK	Serial digital interface clock (1.2 V CMOS).
A2	SCANOUT	Serial digital interface out (1.2 V CMOS).
A3	VOUT_QM	Quadrature Negative Baseband Output. This pin is dc coupled and matched to 50Ω.
A4	VOUT_QP	Quadrature Positive Baseband Output. This pin is dc coupled and matched to 50Ω.
A5	VCC_{BUF}	Power supply for the buffer (2.7 Vdc).
A6	VOUT_IM	In-Phase Negative Baseband Output. This pin is dc coupled and matched to 50Ω.
A7	VOUT_IP	In-Phase Positive Baseband Output. This pin is dc coupled and matched to 50Ω.
A8	RESET	Serial digital interface reset. (1.2 V CMOS).
A9-A12, B10-B12	VCC_{DIV}	Power supply for the divider (2.7Vdc).
B1	ENABLE	Serial digital interface enable (1.2 V CMOS).
B2	DATA	Serial digital interface data (1.2 V CMOS).
B3, B4, B6, B7,C1, D1, F1, G2, H1, H5	GND	Analog Ground Connect.
B5	VDD_{D}	Power supply for digital circuits (1.3 Vdc).
B8	EXTFIL_P	External PLL loop filter (positive).
B9	EXTFIL_N	External PLL loop filter (negative).
C9-C12	VSS_{DIV}	Digital ground for the Synthesizer .
D9-D12	VSS_{LPF}	Digital ground for the Synthesizer .
E1	RFIN	Radio Frequency Input. This pin is AC coupled and matched to 50 Ω.
E10-E11	VSS_{CP}	Digital ground for the Synthesizer .
E12	REF_{CLKP}	External Reference Clock (Positive). This pin can be dc or ac matched to 50 ohms.
F9, G12	VDD_{SYN}	Power Supply for the Synthesizer (1.3 Vdc).
F10-F11	VSS_{REF}	Digital ground for the Synthesizer .
F12	REF_{CLKN}	External Reference Clock (Negative). This pin can be dc or ac matched to 50 ohms.
G1	$ANACTRL_{LNA}$	Analog Gain Control for the Low Noise Amplifier. Leave floating for digital control.
G3	VCC_{MIX}	Power supply for the mixer (2.7 Vdc).
G5	VCC_{TRIP}	Power supply for the tripler (2.7 Vdc).
G6	$VREG_{OUT}$	Regulator Output for the VCO.
G7-G8, H6, H9-H12	VSS_{VCO}	Digital ground for the Synthesizer .
G9-G10	VCC_{VCO}	Power supply for the VCO (2.7Vdc).
G11	VCO_{RCAP}	External capacitor connection for VCO regulator
H2	VCC_{LNA}	Power supply for the LNA (2.7 Vdc).
H3	VCC_{IF}	Power supply for the IF (2.7 Vdc).
H4	$ACTL_{IFVGA}$	Analog Gain Control for IFVGA. Tie high for digital control.
H7	EXTLO_N	External LO (negative) Input.
H8	EXTLO_P	External LO (positive) Input.

Theory of Operation

An integrated frequency synthesizer creates a low-phase noise LO between 16.3 and 18.3 GHz. The step size of the synthesizer equates to 250 MHz steps at RF when used with 71.42857 MHz reference crystal or 500 MHz if used with 142.857 reference crystal. To support IEEE channels (ISM band) with a 540 MHz step size, a 154.2857 MHz reference crystal should be used.

A 57 to 64 GHz signal enters the chip through a single-ended LNA input. The LNA provides 20 dB of variable gain. The LO is multiplied by three and mixed with the LNA output to downconvert to an 8.14 to 9.1 GHz sliding IF. An integrated notch filter removes the image frequency at 40 - 46 GHz. The IF signal is filtered and amplified with 14 dB of variable gain. If the chip is configured for IQ baseband output, the IF signal is feds into a quadrature demodulator using the LO/2 to downconvert to baseband. There are also options to use on-chip demodulators capable of demodulating AM/FM/FSK/MSK waveforms.

The phase noise and quadrature balance of the on-chip synthesizer is sufficient to support up to 64-QAM modulation. For higher order modulation up to 256-QAM or less than 250 MHz step size, the HMC6301BG46 can be operated using an external LO.

The HMC6301BG46 receiver is ideal for FDD operation along with the HMC6300BG46 transmitter chip. However, both devices can support TDD operation by enabling and disabling the circuits. All of the enables are placed in register array 4 which allows for full chip enable or disable in one SPI write.

There are no special power sequencing requirements for the HMC6301BG46; all voltages are to be applied simultaneously.

Resister Array Assignment and Serial Interface

The register arrays for both the receiver and transmitter are organized into 32 rows of 8 bits. Using the serial interface, the arrays are written or read one row at a time as shown in Figure 16 and Figure 17 respectively. Figure 16 shows the sequence of signals on the ENABLE, CLK, and DATA lines to write one 8-bit row of the register array. The ENABLE line goes low, the first of 18 data bits (bit 0) is placed on the DATA line, and 2 ns or more after the DATA line stabilizes, the CLK line goes high to clock in data bit 0. The DATA line should remain stable for at least 2 ns after the rising edge of CLK.

A write operation requires 18 data bits and 18 clock pulses, as shown in Figure 16. The 18 data bits contain the 8-bit register array row data (LSB is clocked in first), followed by the register array row address (ROW0 through ROW23, 000000 to 001111, LSB first), the Read/Write bit (set to 1 to write), and finally the Rx chip address 111, LSB first).

The RX IC serial interface has been tested to 500 MHz, and the interface is 1.2 V CMOS levels.

Note that the register array row address is 6 bits, but only four are used to designate 16 rows, the two MSBs are 0.

After the 18th clock pulse of the write operation, the ENABLE line returns high to load the register array on the IC; prior to the rising edge of the ENABLE line, no data is written to the array. The CLK line should have stabilized in the low state at least 2 ns prior to the rising edge of the ENABLE line.

Figure 16. Timing Diagram for Writing a Row of the Receiver Serial Interface

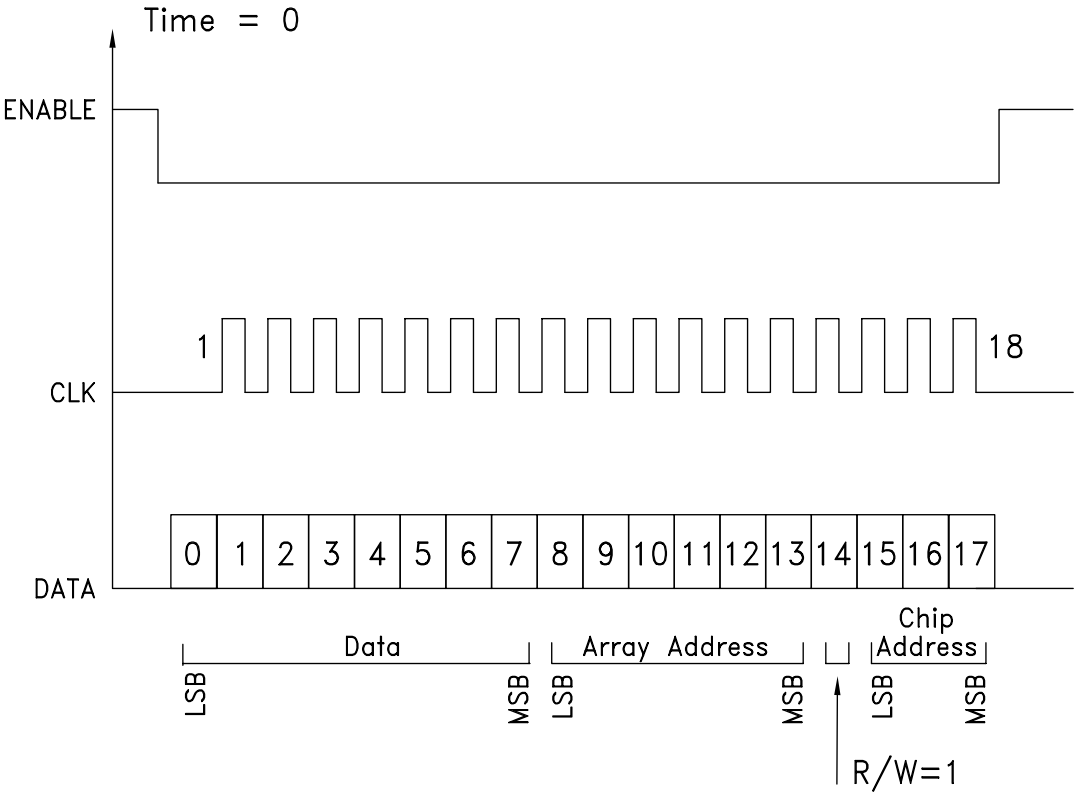


Figure 17. Timing Diagram for Reading a Row of the Receiver Serial Interface

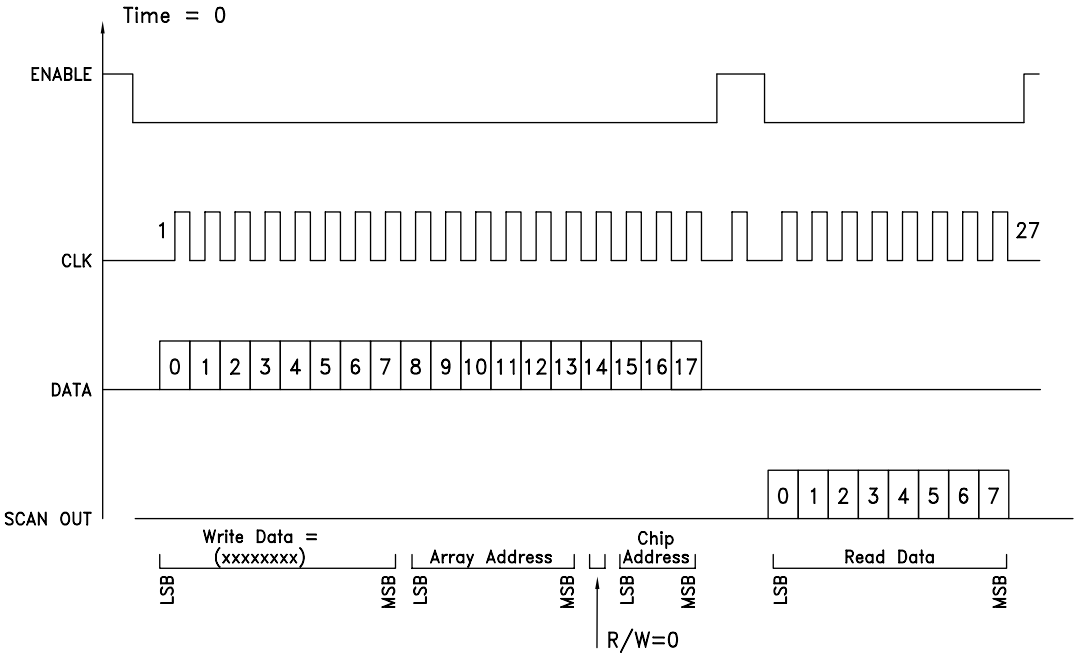


Table 8. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW0		
ROW0<7>	lna_pwrdwn	Active high to power down the LNA
ROW0<6>	bbamp_pwrdn_i	Active high to power down the baseband I channel
ROW0<5>	bbamp_pwrdn_q	Active high to power down the baseband Q channel
ROW0<4>	divider_pwrdn	Active high to power down the LO divider
ROW0<3>	rfmix_pwrdn	Active high to power down the RF mixer
ROW0<2>	ifmix_pwrdn / ifmix_pwrdn_i	Active high to power down the I-channel IF mixer
ROW0<1>	tripler_pwrdn	Active high to power down the LO tripler
ROW0<0>	ifvga_pwrdn	Active high to power down the IFVGA
ROW1		
ROW1<7>	ipc_pwrdn	Active high to power down on-chip current reference generator
ROW1<6>	ifmix_pwrdn_q	Active high to power down the Q-channel IF mixer
ROW1<5>	if_bgmux_pwrdn	Active high to power down one of three on-chip bandgap refs (IF) and associated mux
ROW1<4>	ask_pwrdn	Active high to power down the ASK demodulator
ROW1<3>	bbamp_atten1_0	Controls first baseband attenuator; ROW1<2:3> = 11 is 18 dB attenuation 10 is 12 dB attenuation 01 is 6 dB attenuation 00 is 0 dB attenuation
ROW1<2>	bbamp_atten1_1	
ROW1<1>	bbamp_sel_ask	Active high to multiplex the AM detector output into the I channel baseband amplifier input
ROW1<0>	bbamp_sigshort	Active high to short the input to the I and Q channel baseband amplifiers
ROW2		
ROW2<7>	bbamp_attenfi_0	Controls I Channel baseband fine attenuator; ROW2<5:7> ≥ 101 is 5 dB attenuation 100 is 4 dB attenuation 011 is 3 dB attenuation 010 is 2 dB attenuation 001 is 1 dB attenuation 000 is 0 dB attenuation
ROW2<6>	bbamp_attenfi_1	
ROW2<5>	bbamp_attenfi_2	
ROW2<4>	bbamp_attenfq_0	Controls Q Channel baseband fine attenuator; ROW2<2:4> ≥ 101 is 5 dB attenuation 100 is 4 dB attenuation 011 is 3 dB attenuation 010 is 2 dB attenuation 001 is 1 dB attenuation 000 is 0 dB attenuation
ROW2<3>	bbamp_attenfq_1	
ROW2<2>	bbamp_attenfq_2	
ROW2<1>	bbamp_atten2_0	Controls second baseband attenuator; ROW1<0:1> = 11 is 18 dB attenuation 10 is 12 dB attenuation 01 is 6 dB attenuation 00 is 0 dB attenuation
ROW2<0>	bbamp_atten2_1	

Table 8. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW3		
ROW3<7>	bbamp_selbw0	Selects the low pass corner of the baseband amplifiers; ROW3<6:7> = 00 is ≈ 1.4 GHz 01 is ≈ 500 MHz 10 is ≈ 300 MHz 11 is ≈ 200 MHz
ROW3<6>	bbamp_selbw1	
ROW3<5>	bbamp_selfastrec	Selects the high pass corner of the baseband amplifiers; ROW3<4:5> = 00 is ≈ 45 kHz 01 is ≈ 350 kHz 10 is ≈ 1.6 MHz
ROW3<4>	bbamp_selfastrec2	
ROW3<3>	bg_monitor_sel<1>	For diagnostic purposes; ROW3<3:0> = 0011 for normal operation
ROW3<2>	bg_monitor_sel<0>	
ROW3<1>	if_refsel	
ROW3<0>	lna_refsel	
ROW4		
ROW4<7>	ifvga_bias<2>	Controls bias and IF filter alignment in the IF variable gain amplifier; ROW4<7:1> = 1001111 for normal operation
ROW4<6>	ifvga_bias<1>	
ROW4<5>	ifvga_bias<0>	
ROW4<4>	ifvga_tune<3>	
ROW4<3>	ifvga_tune<2>	
ROW4<2>	ifvga_tune<1>	
ROW4<1>	ifvga_tune<0>	
ROW4<0>	enDigVGA	Active high to enable digital control of IFVGA gain
ROW5		
ROW5<7>	ifvga_vga_adj<3>	Controls IF variable gain amplifier; ROW5<7:4> 0000 is highest gain 1111 is lowest gain
ROW5<6>	ifvga_vga_adj<2>	
ROW5<5>	ifvga_vga_adj<1>	
ROW5<4>	ifvga_vga_adj<0>	
ROW5<3>	rfmix_tune<3>	Controls IF filter alignment in the RF mixer; ROW5<3:0> = 1111 for normal operation
ROW5<2>	rfmix_tune<2>	
ROW5<1>	rfmix_tune<1>	
ROW5<0>	rfmix_tune<0>	
ROW6		
ROW6<7>	tripler_bias<13>	Controls the bias of the frequency tripler; ROW6<7:0> = 10111111 for normal operation
ROW6<6>	tripler_bias<12>	
ROW6<5>	tripler_bias<11>	
ROW6<4>	tripler_bias<10>	
ROW6<3>	tripler_bias<9>	
ROW6<2>	tripler_bias<8>	
ROW6<1>	tripler_bias<7>	
ROW6<0>	tripler_bias<6>	

Table 8. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW7		
ROW7<7>	tripler_bias<5>	Controls bias of the frequency tripler; ROW7<7:2> = 011011 for normal operation
ROW7<6>	tripler_bias<4>	
ROW7<5>	tripler_bias<3>	
ROW7<4>	tripler_bias<2>	
ROW7<3>	tripler_bias<1>	
ROW7<2>	tripler_bias<0>	
ROW7<1>	bbamp_selfm	Active high to multiplex the FM detector output into the Q channel baseband amplifier input
ROW7<0>	fm_pwrdn	Active high to power down FM demodulator
ROW8		
ROW8<7>	lna_bias<2>	Controls bias of the low noise amplifier; ROW8<7:5> = 100 for normal operation
ROW8<6>	lna_bias<1>	
ROW8<5>	lna_bias<0>	
ROW8<4>	lna_gain<1>	Controls LNA variable gain; ROW8<4:3> 00 is highest gain 11 is lowest gain
ROW8<3>	lna_gain<0>	
ROW8<2>	ifvga_q_cntrl<2>	Controls the Q of the IF filter in the IF variable gain amplifier; ROW8<2:0> = 000 for highest Q and highest gain. To reduce Q and widen bandwidth, increment ROW8<2:0> in the sequence: 001 100 101 111
ROW8<1>	ifvga_q_cntrl<1>	
ROW8<0>	ifvga_q_cntrl<0>	
ROW9		
ROW9<7>	enAnaV_LNA	Active high to enable analog gain control of LNA
ROW9<6>	enbar_TempS	Active high to power down the temperature sensor
ROW9<5>	en_tempFlash	Active high to enable temperature sensor
ROW9<4>	en_Sep_ifmix_pwrdn_q	Enable separate power down for IF mixer I/Q 0 for normal operation
ROW9<3>	Not used	Not used
ROW9<2>	Not used	Not used
ROW9<1>	Not used	Not used
ROW9<0>	Not used	Not used
ROW10 (not used)		
ROW11 (not used)		
ROW12 (not used)		
ROW13 (not used)		
ROW14 (not used)		
ROW15 (not used)		

Table 8. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW16		
ROW16<7>	byp_synth_LDO	Factory Diagnostics, 0 for normal operation
ROW16<6>	en_cpShort	Factory Diagnostics, 0 for normal operation
ROW16<5>	en_cpCMFB	Enable sCMFB circuit for charge pump, set to 1 when synthesizer is in use
ROW16<4>	en_cp_dump	Enables auxiliary circuit for charge pump, set to 1 when synthesizer is in use
ROW16<3>	en_cpTRIST	Factory Diagnostics, 0 for normal operation
ROW16<2>	en_cp	Enables charge pump, set to 1 when synthesizer is in use
ROW16<1>	en_synth_LDO	Enables LDO for synthesizer, set to 1 when synthesizer is in use
ROW16<0>	enbar_synthBG	Factory Diagnostics, 0 for normal operation
ROW17		
ROW17<7>	en_lockd_clk	Enables lock detector for synthesizer, set to 1 when synthesizer is in use
ROW17<6>	en_test_divOut	Factory Diagnostics, 0 for normal operation
ROW17<5>	en_vtune_flash	Enables flash ADCs for VCO vtune port, set to 1 when synthesizer is in use
ROW17<4>	en_reBuf_DC	Enables DC-coupling for reference clock buffer
ROW17<3>	en_refBuf	Enables reference clock buffer, set to 1 when synthesizer is in use
ROW17<2>	en_stick_div	Factory Diagnostics, 0 for normal operations
ROW17<1>	en_FBDiv_cml2cmos	Enables auxiliary circuit for the feedback divider chain, set to 1 when synthesizer is in use
ROW17<0>	en_FBDiv	Enables feedback divider chain, set to 1 when synthesizer is in use
ROW18		
ROW18<7>	Not used	Not used
ROW18<6>	en_nb250m	Active high to enable 250 MHz channel step size
ROW18<5>	byp_vco_LDO	Factory Diagnostics, 0 for normal operation
ROW18<4>	en_extLO	Enables external LO, set to 0 when synthesizer is in use
ROW18<3>	en_vcoPk	Factory Diagnostics, 0 for normal operation
ROW18<2>	en_vco	Enables internal VCO, set to 1 when synthesizer is in use
ROW18<1>	en_vco_reg	Enables internal regulator for VCO, set to 1 when synthesizer is in use
ROW18<0>	enbar_vcoGB	Factory Diagnostics, 0 for normal operation
ROW19		
ROW19<7>	Not used	Not used
ROW19<6>	Not used	Not used
ROW19<5>	Not used	Not used
ROW19<4>	Not used	Not used
ROW19<3>	Not used	Not used
ROW19<2>	Not used	Not used
ROW19<1>	refsel_synthBG	Factory Diagnostics, 1 for normal operation
ROW19<0>	muxRef	Factory Diagnostics, 0 for normal operation

Table 8. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW20		
ROW20<7>	Not used	Not used
ROW20<6>	Fbdiv_code<6>	Feedback divider ratio for the integer-N internal synthesizer based on tables 15, 16 & 17
ROW20<5>	Fbdiv_code<5>	
ROW20<4>	Fbdiv_code<4>	
ROW20<3>	Fbdiv_code<3>	
ROW20<2>	Fbdiv_code<2>	
ROW20<1>	Fbdiv_code<1>	
ROW20<0>	Fbdiv_code<0>	
ROW21		
ROW21<7>	Not used	Not used
ROW21<6>	Not used	Not used
ROW21<5>	Not used	Not used
ROW21<4>	refsel_vcoBG	Factory Diagnostics, 1 for normal operation
ROW21<3>	vco_biasTrim<3>	Sets VCO tank bias current ROW21<3:0> = 0010 for normal operation
ROW21<2>	vco_biasTrim<2>	
ROW21<1>	vco_biasTrim<1>	
ROW21<0>	vco_biasTrim<0>	
ROW22		
ROW22<7>	Not used	Not used
ROW22<6>	Not used	Not used
ROW22<5>	Not used	Not used
ROW22<4>	vco_bandSel<4>	Set for desired frequency. Tables 15, 16 & 17 contain approximate band setting depending on reference clock frequency. ROW22<4:0> = Valid range 00000-10011
ROW22<3>	vco_bandSel<3>	
ROW22<2>	vco_bandSel<2>	
ROW22<1>	vco_bandSel<1>	
ROW22<0>	vco_bandSel<0>	
ROW23		
ROW23<7>	ICP_BiasTrim<2>	Sets charge pump current ROW23<7:5> = 011 for normal operation
ROW23<6>	ICP_BiasTrim<1>	
ROW23<5>	ICP_BiasTrim<0>	
ROW23<4>	vco_offset<0>	Sets internal VCO output swing ROW23<4:0> = 00010 for normal operation
ROW23<3>	vco_offset<1>	
ROW23<2>	vco_offset<2>	
ROW23<1>	vco_offset<3>	
ROW23<0>	vco_offset<4>	

Table 8. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW24 (read only)		
ROW24<7>	Not used	Not used
ROW24<6>	Not used	Not used
ROW24<5>	Not used	Not used
ROW24<4>	Not used	Not used
ROW24<3>	lockdet	Monitor for lock detect, 1 indicates valid lock
ROW24<2>	dn	Monitor VCO amplitude
ROW24<1>	up	Monitor VCO amplitude
ROW24<0>	center	Monitor VCO amplitude
ROW25 (read only)		
ROW25<7>	vtune_flashp<7>	VCO amplitude monitor (positive)
ROW25<6>	vtune_flashp<6>	
ROW25<5>	vtune_flashp<5>	
ROW25<4>	vtune_flashp<4>	
ROW25<3>	vtune_flashp<3>	
ROW25<2>	vtune_flashp<2>	
ROW25<1>	vtune_flashp<1>	
ROW25<0>	vtune_flashp<0>	
ROW26 (read only)		
ROW26<7>	vtune_flashn<7>	VCO amplitude monitor (negative)
ROW26<6>	vtune_flashn<6>	
ROW26<5>	vtune_flashn<5>	
ROW26<4>	vtune_flashn<4>	
ROW26<3>	vtune_flashn<3>	
ROW26<2>	vtune_flashn<2>	
ROW26<1>	vtune_flashn<1>	
ROW26<0>	vtune_flashn<0>	
ROW27 (read only)		
ROW27<7>	Not used	Not used
ROW27<6>	Not used	Not used
ROW27<5>	Not used	Not used
ROW27<4>	tempS<4>	Thermometer encoded temperature reading ROW27<4:0> = 00000 is lowest temperature 11111 is highest temperature
ROW27<3>	tempS<3>	
ROW27<2>	tempS<2>	
ROW27<1>	tempS<1>	
ROW27<0>	tempS<0>	
ROW28 (not used)		
ROW29 (not used)		
ROW30 (not used)		
ROW31 (not used)		

Table 9. Synthesizer Settings, IEEE Channels Using 308.5714 MHz Reference

Frequency (GHz)	Divider Setting Fbdiv_Code<5:0> ROW20<5:0>	Typical Band Setting vco_bandSel<4:0> ROW22<4:0>
57.24	001010	00001
57.78	001011	00010
58.32 (IEEE CH 1)	001100	00010
58.86	001101	00010
59.40	001110	00011
59.94	001111	00011
60.48 (IEEE CH 2)	010000	00100
61.02	010001	00100
61.56	010010	00101
62.10	010011	00101
62.64 (IEEE CH 3)	010100	00101
63.18	010101	00110
63.72	010110	00110
64.26	010111	00110
64.8 (IEEE CH 4)	011000	00111
65.34	011001	00111
65.88	011010	01000

Table 10. 500 MHz Channels Using 142.8571 MHz Reference

Frequency (GHz)	Divider Setting	Typical Band Setting
56.5	010001	00001
57	010010	00001
57.5	010011	00010
58	010100	00010
58.5	010101	00010
59	010110	00011
59.5	010111	00011
60	011000	00100
60.5	011001	00100
61	011010	00101
61.5	011011	00101
62	011100	00101
62.5	011101	00110
63	011110	00110
63.5	011111	00110
64	100000	00111

Table 11. 250 MHz Channels Using 70.42857 MHz Reference

Frequency (GHz)	Divider Setting	Typical Band Setting
56.5	0100010	00001
56.75	0100011	00001
57	0100100	00010
57.25	0100101	00010
57.5	0100110	00011
57.75	0100111	00011
58	0101000	00100
58.25	0101001	00100
58.5	0101010	00101
58.75	0101011	00101
59	0101100	00110
59.25	0101101	00110
59.5	0101110	00111
59.75	0101111	00111
60	0110000	01000
60.25	0110001	01000
60.5	0110010	01001
60.75	0110011	01001
61	0110100	01010
61.25	0110101	01010
61.5	0110110	01011
61.75	0110111	01011
62	0111000	01100
62.25	0111001	01100
62.5	0111010	01101
62.75	0111011	01101
63	0111100	01110
63.25	0111101	01110
63.5	0111110	01111
63.75	0111111	01111
64	1000000	01111

Figure 18. Evaluation PCB Daughter Board

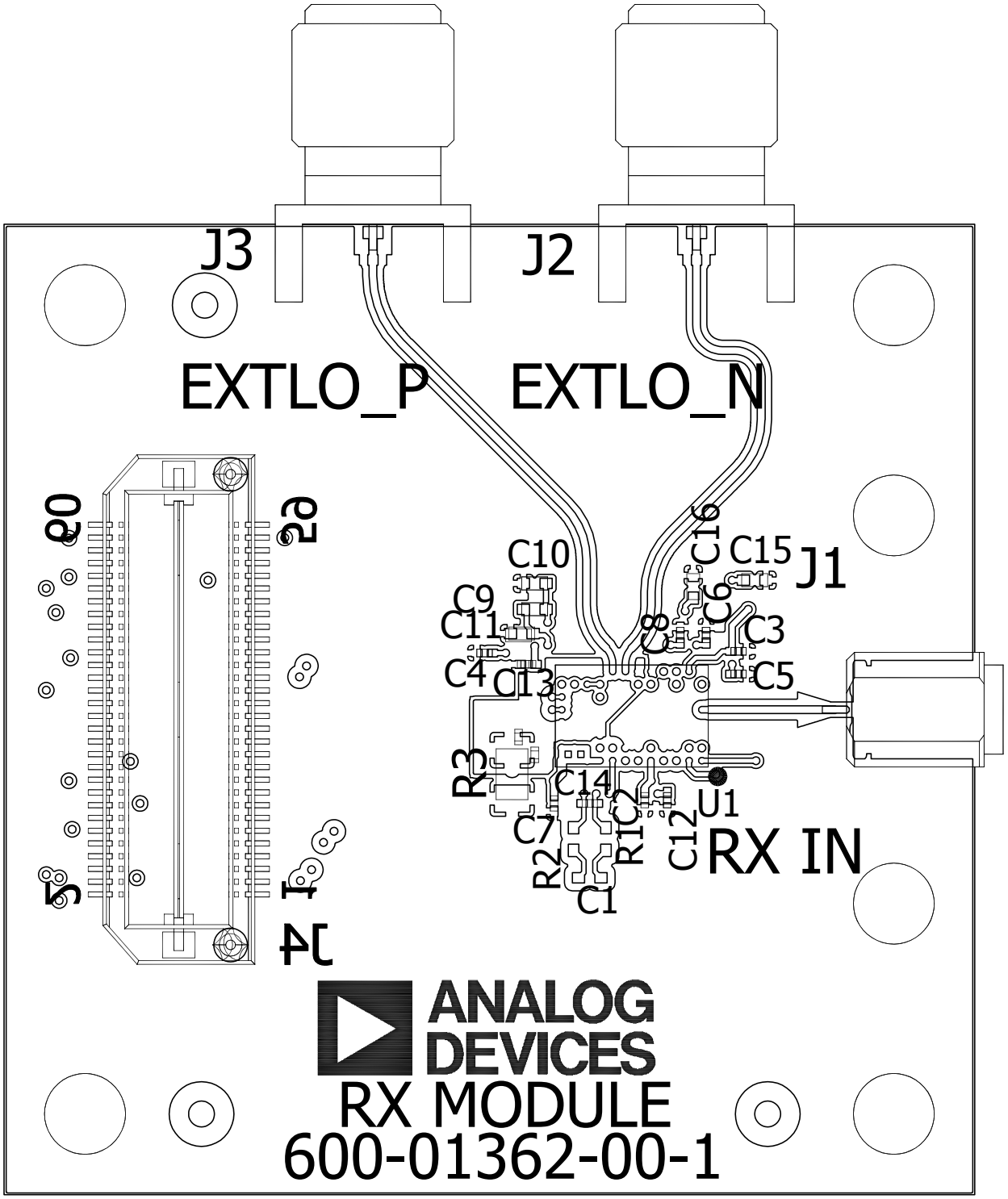


Figure 19. Evaluation PCB Schematic

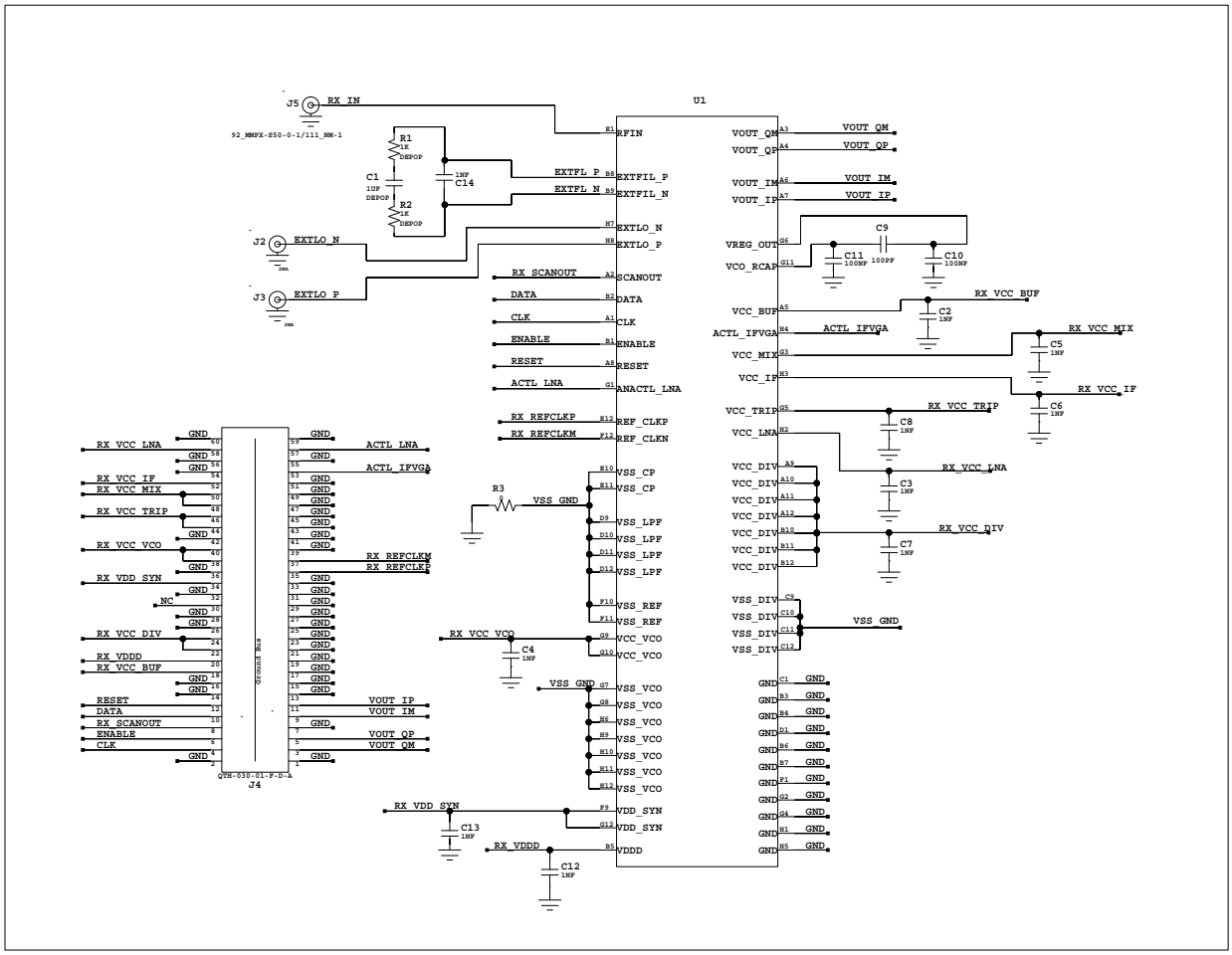


Figure 20. Evaluation PCB Mother Board

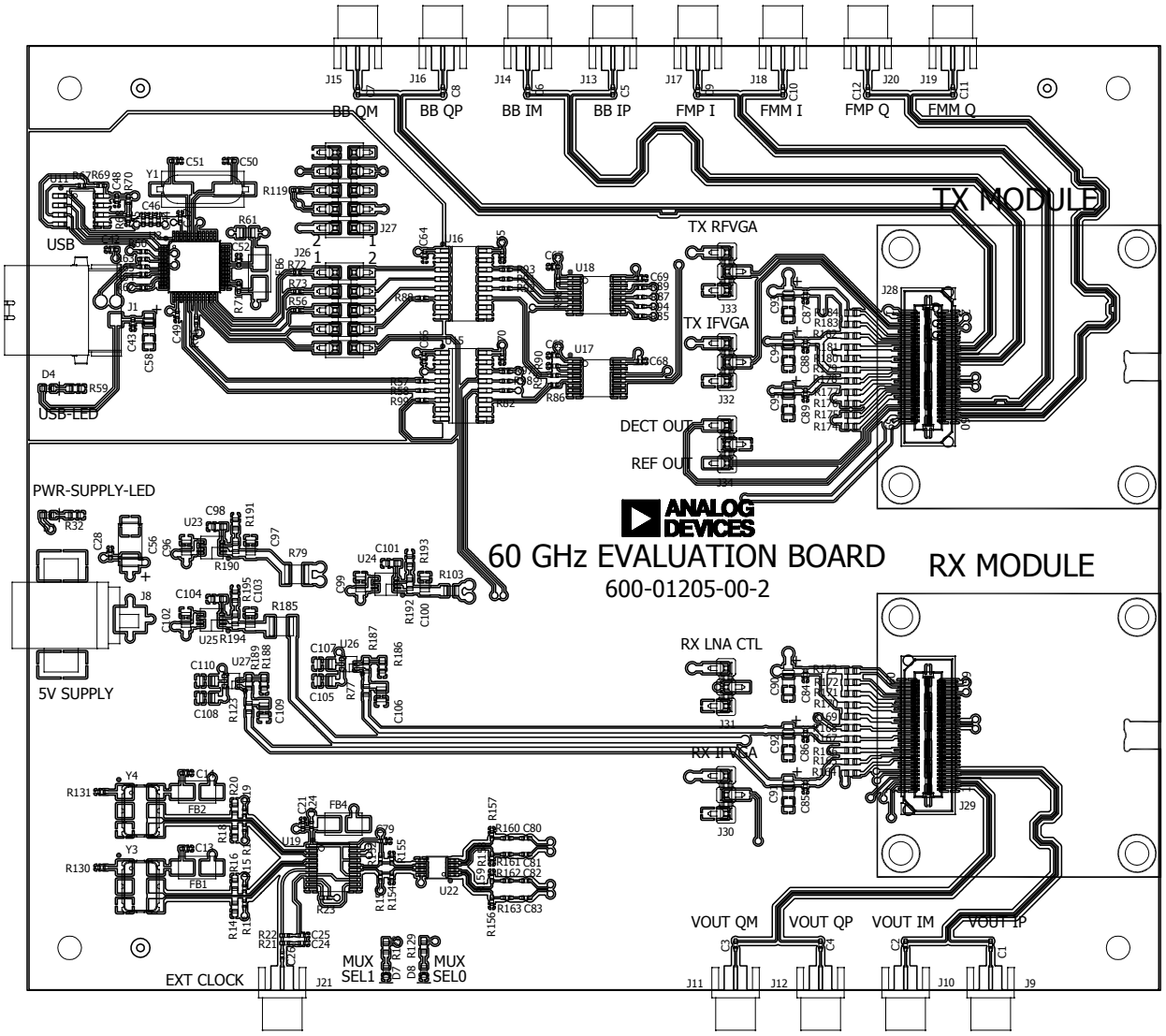


Table 12. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC6301BG46 Evaluation PCB	EV1HMC6301BG46 [1]
Evaluation Kit	HMC6301BG46 Evaluation Kit	EK1HMC6350 [2]

[1] Reference this number when ordering an HMC6301BG46 PCB only.
[2] Reference this number when ordering an HMC6301BG46 Evaluation Kit. The EK1HMC6350 kit contains everything that is needed to set up a simplex 60 GHz millimeter-wave link using standard RF cable interfaces for baseband input and output. The kit comes with two mother board PCBs that provide on board crystals, USB interface, supply regulators, and SMA cables for connectorized IQ interfaces. Supplied software allows the user to read from and write to all chip level registers using Graphical User Interface (GUI) or upload previously saved register settings.

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