Enpirion Power Datasheet
EY1602 40V, Low Quiescent Current, 50mA Linear Regulator

The Altera® Enpirion® EY1602 is a wide input voltage range, low quiescent current linear regulator ideally suited for "always-on" and "keep alive" applications. The EY1602 operates from an input voltage of +6V to +40V under normal operating conditions, consuming only 18µA of quiescent current at no load.

The EY1602 has an adjustable output voltage range from 1.223V to 12V. It features an EN pin that can be used to put the device into a low-quiescent current shutdown mode where it draws only 1.8µA of supply current. The device features automatic thermal shutdown and current limit protection.

The EY1602 is rated over the -40°C to +125°C temperature range and is available in an 8 lead EPSOIC with exposed pad package..

TABLE 1. KEY DIFFERENCES IN FAMILY OF 40V LDO PARTS

PART NUMBER	MIN. I_{OUT}	ADJ OR FIXED V_{OUT}
EY1602SI-ADJ	50mA	ADJ
EY1603TI-ADJ	150mA	ADJ

Features

- Wide V_{IN} range of 6V to 40V
- Adjustable output voltage from 1.223V to 12V
- Guaranteed 50mA output current
- Ultra low 18µA typical quiescent current
- Low 1.8µA of typical shutdown current
- ±1% accurate voltage reference
- Low dropout voltage of 120mV at 50mA
- 40V tolerant logic level (TTL/CMOS) enable input
- Stable operation with 10µF output capacitor
- 5kV ESD HBM rated
- Thermal shutdown and current limit protection

Applications

- FPGA applications
- Industrial
- Networking
- Telecom

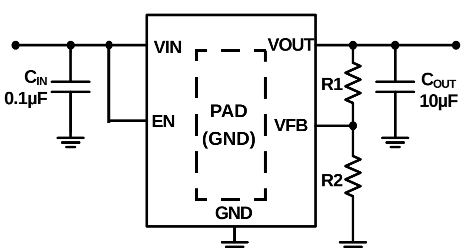


FIGURE 1. TYPICAL APPLICATION

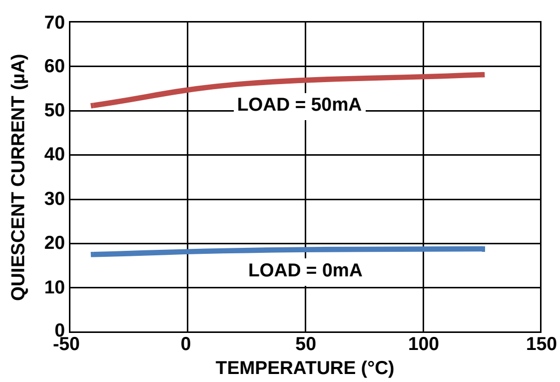


FIGURE 2. QUIESCENT CURRENT vs LOAD CURRENT (AT UNITY GAIN), V_{IN} = 14V

101 Innovation Drive
San Jose, CA 95134
www.altera.com

Ordering Information

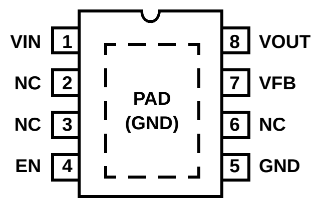
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	ENABLE PIN	OUTPUT VOLTAGE (V)	PACKAGE (Pb-Free)	PKG. DWG. #
EY1602SI-ADJ (Notes 1)	1602AS	-40 to +125	Yes	Adjustable	8 Ld EPSOIC	M8.15B
EVB-EY1602SI-ADJ	Evaluation Platform					

NOTES:

1. Add "-T*" suffix for tape and reel.
2. These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

EY1602SI-ADJ
(8 LD EPSOIC)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1	VIN	Input voltage pin. A minimum 0.1µF X5R/X7R capacitor is required for proper operation. Range: 6V to 40V
2, 3, 6	NC	Pins have internal termination and can be left not connected. Connection to ground is optional.
4	EN	High on this pin enables the device. Range: 0V to V_{IN}
5	GND	Ground pin.
7	VFB	This pin is connected to the external feedback resistor divider, which sets the LDO output voltage.Range: 0V to 3V
8	VOUT	Regulated output voltage. A 10µF X5R/X7R output capacitor is required for stability. Range: 0V to 12V
-	PAD	It is recommended to solder the PAD to the ground plane.

Absolute Maximum Ratings

VIN Pin to GND Voltage . . . . .GND - 0.3V to +45V
VOUT Pin to GND Voltage . . . . .GND - 0.3V to 16V
EN Pin to GND Voltage . . . . GND - 0.3V to VIN
VFB Pin to GND Voltage . . . . GND - 0.3V to3V
Output Short-circuit Duration. . . . . .Indefinite
ESD Rating
Human Body Model (Tested per JESD22-A114E). 5kV
Machine Model (Tested per JESD-A115-A) 200V
Charge Device Model (Tested per JESD22-C101C) . . . 2.2kV
Latch Up (Tested per JESD78B; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld EPSOIC Package (Notes 3, 4)	50	9

Maximum Junction Temperature . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +175°C
Pb-Free Reflow Profile . . . . —

Recommended Operating Conditions

Ambient Temperature Range . . . . -40°C to +125°C
VIN Pin to GND Voltage . . . .+6V to +40V
VOUT Pin to GND Voltage . . . .+1.223V to +12V
EN Pin to GND Voltage . . . . .0V to +40V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
4. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted. V_{IN} = 14V, I_{OUT} = 1mA, C_{IN} = 0.1µF, C_{OUT} = 10µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Input Voltage Range	V_{IN}		**6**		**40**	V
Guaranteed Output Current	I_{OUT}	V_{IN} = V_{OUT} + VDO	**50**			mA
VFB Reference Voltage	V_{REF}	EN = High, V_{IN} = 14V, I_{OUT} = 0.1mA	**1.211**	1.223	**1.235**	V
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	3V ≤ V_{IN} ≤ 40V, I_{OUT} = 1mA		0.04	**0.115**	%
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	V_{IN} = V_{OUT} +V_D, I_{OUT} = 100µA to 50mA		0.25	**0.5**	%
Dropout Voltage (Note 5)	ΔV_{DO}	I_{OUT} = 1mA, V_{OUT} = 3.3V		10	**38**	mV
		I_{OUT} = 50mA, V_{OUT} = 3.3V		130	**340**	mV
		I_{OUT} = 1mA, V_{OUT} = 5V		10	**48**	mV
		I_{OUT} = 50mA, V_{OUT} = 5V		120	**350**	mV
Shutdown Current	I_{SHDN}	EN = LOW		1.8	**3.64**	µA
Quiescent Current	IQ	EN = HIGH, I_{OUT} = 0mA		18	**24**	µA
		EN = HIGH, I_{OUT} = 1mA		22	**42**	µA
		EN = HIGH, I_{OUT} = 10mA		34	**60**	µA
		EN = HIGH, I_{OUT} = 50mA		56	**82**	µA
Power Supply Rejection Ratio	PSRR	f = 100Hz; Vin_ripple = 500mV_{P-P}; Load = 50mA		58		dB
EN FUNCTION						
EN Threshold Voltage	V_{EN_H}	V_{OUT} = Off to On			**1.485**	V
	V_{EN_L}	V_{OUT} = On to Off	**0.935**			V
EN Pin Current	I_{EN}	V_{OUT} = 0V		0.026		µA
EN to Regulation Time (Note 6)	t_{EN}			1.65	**1.93**	ms
PROTECTION FEATURES						
Output Current Limit	I_{LIMIT}	V_{OUT} = 0V	**60**	118		mA

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted. V_{IN} = 14V, I_{OUT} = 1mA, C_{IN} = 0.1µF, C_{OUT} = 10µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Thermal Shutdown	T_{SHDN}	Junction Temperature Rising		+165		°C
Thermal Shutdown Hysteresis	T_{HYST}			+20		°C

NOTES:

5. Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT} when V_{IN} = V_{OUT} + 3V.
6. Enable to Regulation is the time the output takes to reach 95% of its final value with V_{IN} = 14V and EN is taken from V_{IL} to V_{IH} in 5ns. The output voltage is set at 5V.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25 °C unless otherwise specified.

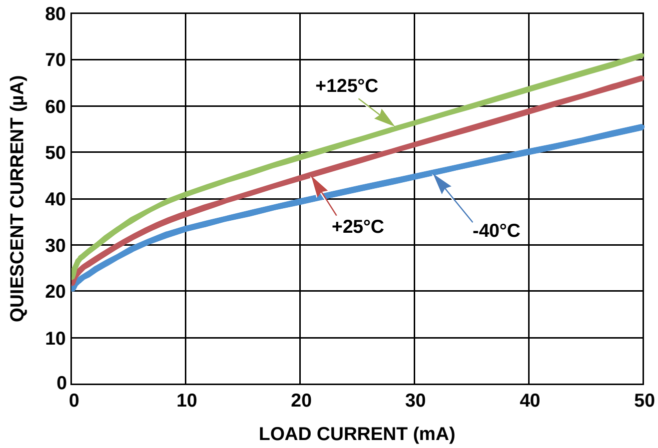


FIGURE 3. QUIESCENT CURRENT vs LOAD CURRENT

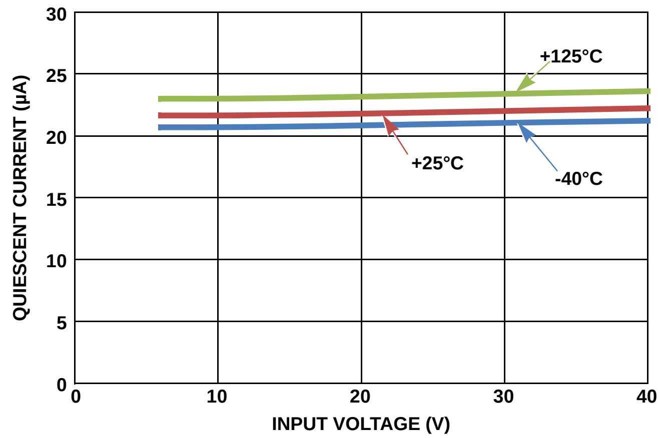


FIGURE 4. QUIESCENT CURRENT vs INPUT VOLTAGE (NO LOAD)

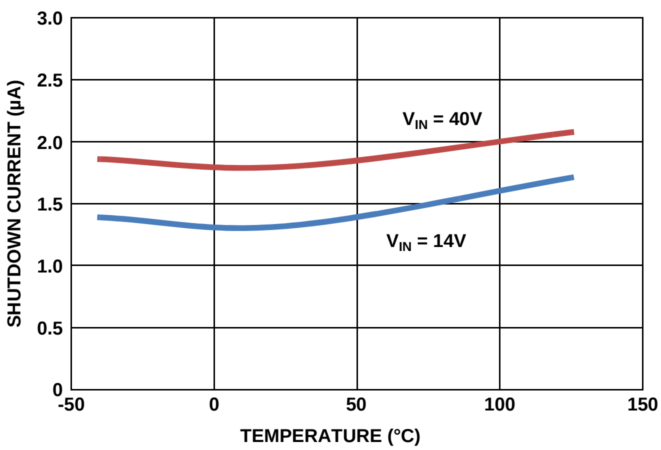


FIGURE 5. SHUTDOWN CURRENT vs TEMPERATURE (EN = 0)

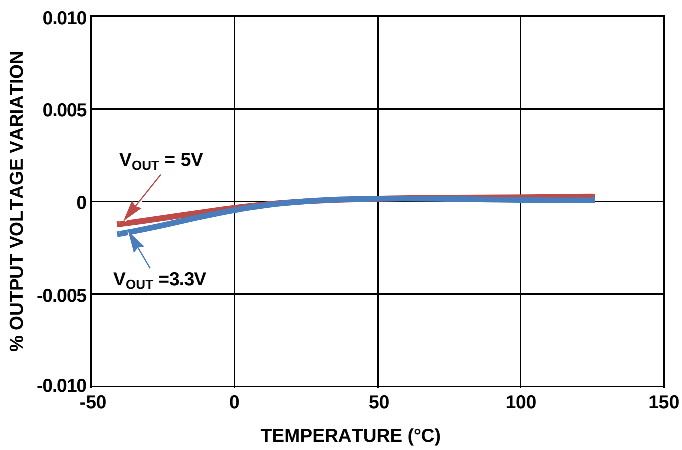


FIGURE 6. OUTPUT VOLTAGE vs TEMPERATURE (LOAD = 50mA)

Typical Performance Curves V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25 °C unless otherwise specified. **(Continued)**

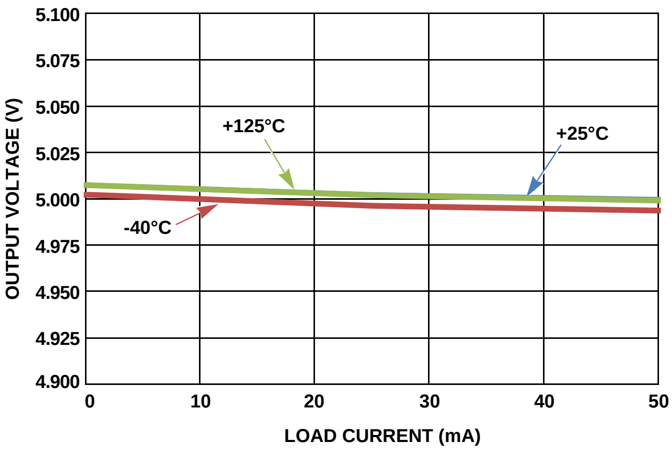


FIGURE 7. OUTPUT VOLTAGE vs LOAD CURRENT

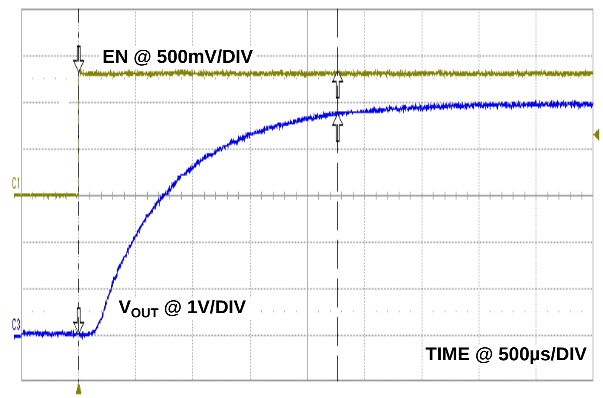


FIGURE 8. START-UP WAVEFORM

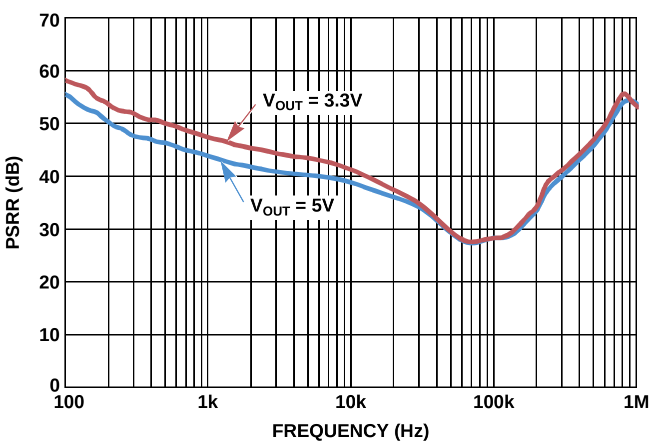


FIGURE 9. POWER SUPPLY REJECTION RATIO (LOAD = 50mA)

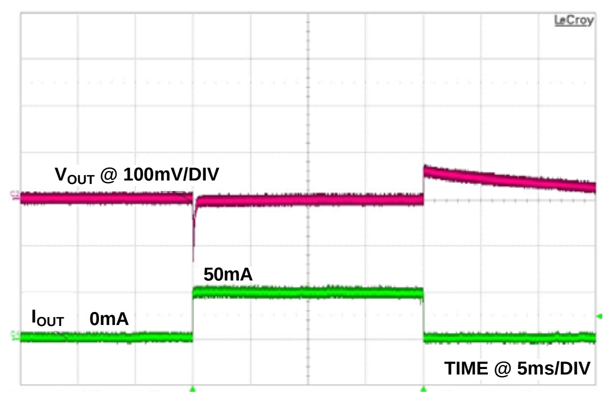
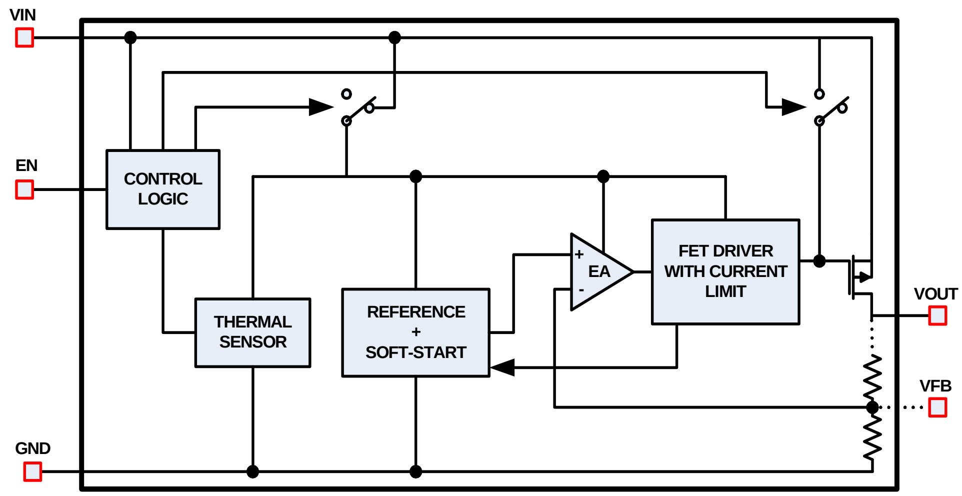


FIGURE 10. LOAD TRANSIENT RESPONSE

Block Diagram



Functional Description

Functional Overview

The EY1602 is a high performance, high voltage, low-dropout regulator (LDO) with 50mA sourcing capability. The part is rated to operate over the -40°C to +125°C temperature range. Featuring ultra-low quiescent current, it makes an ideal choice for “always-on” applications. It works well under a “load dump condition” where the input voltage could rise up to 40V. The device also features current limit and thermal shutdown protection.

Enable Control

The EY1602 features an Enable pin. When it is pulled low, the IC goes into shutdown mode. In this condition, the device draws less than 2µA. Driving the pin high turns the device on. For always on operation, the EN pin can be tied directly to VIN.

Current Limit Protection

The EY1602 has internal current limit functionality to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current largely independent of the output voltage. If the short or overload is removed from VOUT, the output returns to normal voltage regulation mode.

Thermal Fault Protection

In the event that the die temperature exceeds typically +165°C, the output of the LDO will shut down until the die temperature cools down to typically +145°C. The level of power dissipated, combined with the ambient temperature and the thermal impedance of the package, will determine if the junction temperature exceeds the thermal shutdown temperature. Also see the section on “Power Dissipation”.

Application Information

Input and Output Capacitors

For the output, a ceramic capacitor (X5R or X7R) with a capacitance of 10µF is recommended for the EY1602 to maintain stability. The ground connection of the output capacitor should be routed directly to the GND pin of the device and also placed close to the IC. A minimum of 0.1µF (X5R or X7R) is recommended at the input.

Output Voltage Setting

The output voltage is programmed using an external resistor divider, as shown in Figure 11.

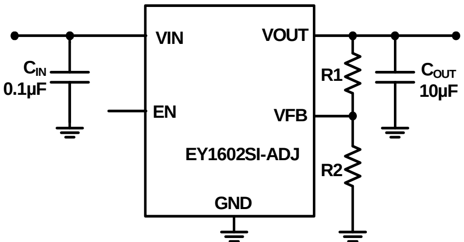


FIGURE 11. SETTING OUTPUT VOLTAGE

The output voltage is calculated using Equation 1:

$$V_{OUT} = 1.223V \times \left(\frac{R1}{R2} + 1\right) \quad \text{(EQ. 1)}$$

Power Dissipation

The junction temperature must not exceed the range specified in "Recommended Operating Conditions" on page 3. The power dissipation can be calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 2)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ will determine the maximum allowable junction temperature rise (ΔT_J), as shown in Equation 3:

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad \text{(EQ. 3)}$$

To calculate the maximum ambient operating temperature, use the junction-to-ambient thermal resistance (θ_{JA}), as shown in Equation 4:

$$T_{J(MAX)} = P_{D(MAX)} \times \theta_{JA} + T_A \quad \text{(EQ. 4)}$$

Board Layout Recommendations

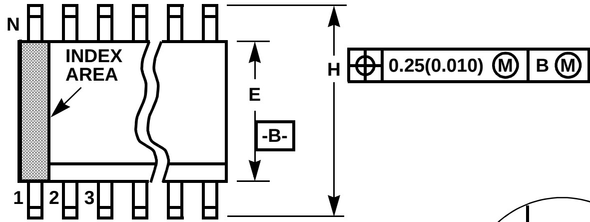
A good PCB layout is important to achieve expected performance. Consideration should be taken when placing the components and routing the trace to minimize the ground impedance, and keep the parasitic inductance low. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. The VFB feedback trace should be away from other noisy traces. Connect the exposed pad to the ground plane for better heat dissipation. Thermal vias on the PAD increases heat dissipation.

Document Revision History

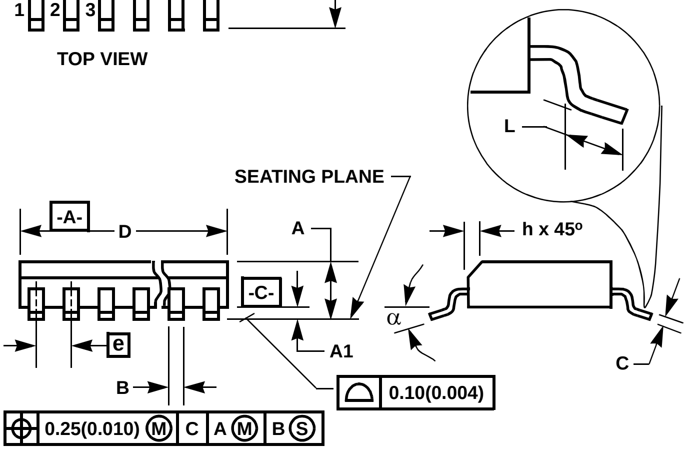
The table lists the revision history for this document.

Date	Version	Changes
June 2015	1.1	Updated the output voltage range.
February 2014	1.0	Initial release.

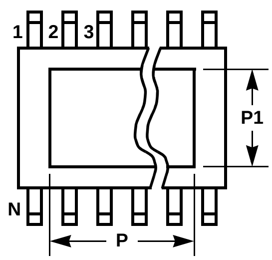
Small Outline Exposed Pad Plastic Packages (EPSOIC)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

M8.15B

8 LEAD NARROW BODY SMALL OUTLINE EXPOSED PAD PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.43	1.68	-
A1	0.001	0.005	0.03	0.13	-
B	0.0138	0.0192	0.35	0.49	9
C	0.0075	0.0098	0.19	0.25	-
D	0.189	0.196	4.80	4.98	3
E	0.150	0.157	3.81	3.99	4
e	0.050 BSC		1.27 BSC		-
H	0.230	0.244	5.84	6.20	-
h	0.010	0.016	0.25	0.41	5
L	0.016	0.035	0.41	0.89	6
N	8		8		7
α	0°	8°	0°	8°	-
P	-	0.094	-	2.387	11
P1	-	0.094	-	2.387	11

Rev. 5 8/10

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
11. Dimensions “P” and “P1” are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count and body size.