Enpirion® Power Datasheet

EN5395QI 9A PowerSoC Synchronous Buck PWM DC-DC Converter with Integrated Inductor 3-Pin VID Output Voltage Select

Description

The EN5395QI is a Power System on a Chip (PowerSoC) DC-DC converter. It is specifically designed to meet the precise voltage and fast transient requirements of present and future high-performance, low-power processor, DSP, FPGA, ASIC, memory boards, and system level applications in distributed power architecture. Advanced circuit techniques, ultra-high switching frequency, and innovative, high-density, integrated circuit and proprietary inductor technology deliver high-quality, ultra-compact, non-isolated DC-DC conversion. Operating this converter requires as few as five external components that include small value input and output ceramic capacitors and a soft-start capacitor.

Altera's Enpirion solution significantly helps in system design and productivity by offering greatly simplified board design, layout and manufacturing requirements. In addition, a reduction in the number of vendors required for the complete power solution helps to enable an overall system cost savings.

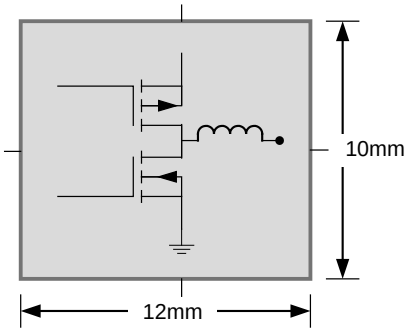
Applications

- Area constrained applications
- Noise sensitive applications
- Low voltage, distributed power architectures with 2.5V, 3.3V or 5V rails
- Computing
- Enterprise Storage
- Broadband, networking, LAN/WAN, optical
- DSL, STB, DVR, DTV, Industrial PC

Ordering Information

Part Number	Temp Rating (°C)	Package
EN5395QI	-40 to +85	58-pin QFN T&R
EVB-EN5395QI	QFN Evaluation Board	

Features



- ***Integrated Inductor Technology:*** Integrated Inductor, MOSFETS, Controller in a 10 x 12 x 1.85mm package
- Low Part Count: only 5 MLC Capacitors.
- Up to 30W continuous output power.
- Low output impedance optimized for ≤ 90 nm
- Master/slave configuration for paralleling.
- 5MHz operating frequency.
- High efficiency, up to 93%.
- Wide input voltage range of 2.375V to 5.5V.
- 3-Pin VID output voltage select to choose one of 7 pre-programmed output voltages.
- Output Enable pin and Power OK signal.
- Programmable soft-start time.
- Adjustable over-current protection.
- Thermal shutdown, short circuit, over-voltage and under-voltage protection.
- RoHS compliant, MSL level 3, 260C reflow.

Typical Application Circuit

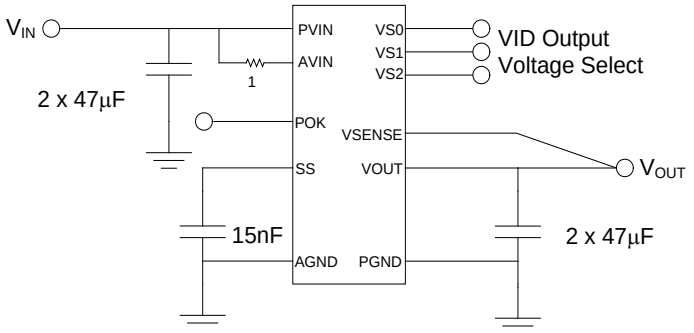


Figure 1. Simple Layout.

Pin Configuration

Below is a top view diagram of the EN5395Q package.

NOTE: NC pins are not to be electrically connected to each other or to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

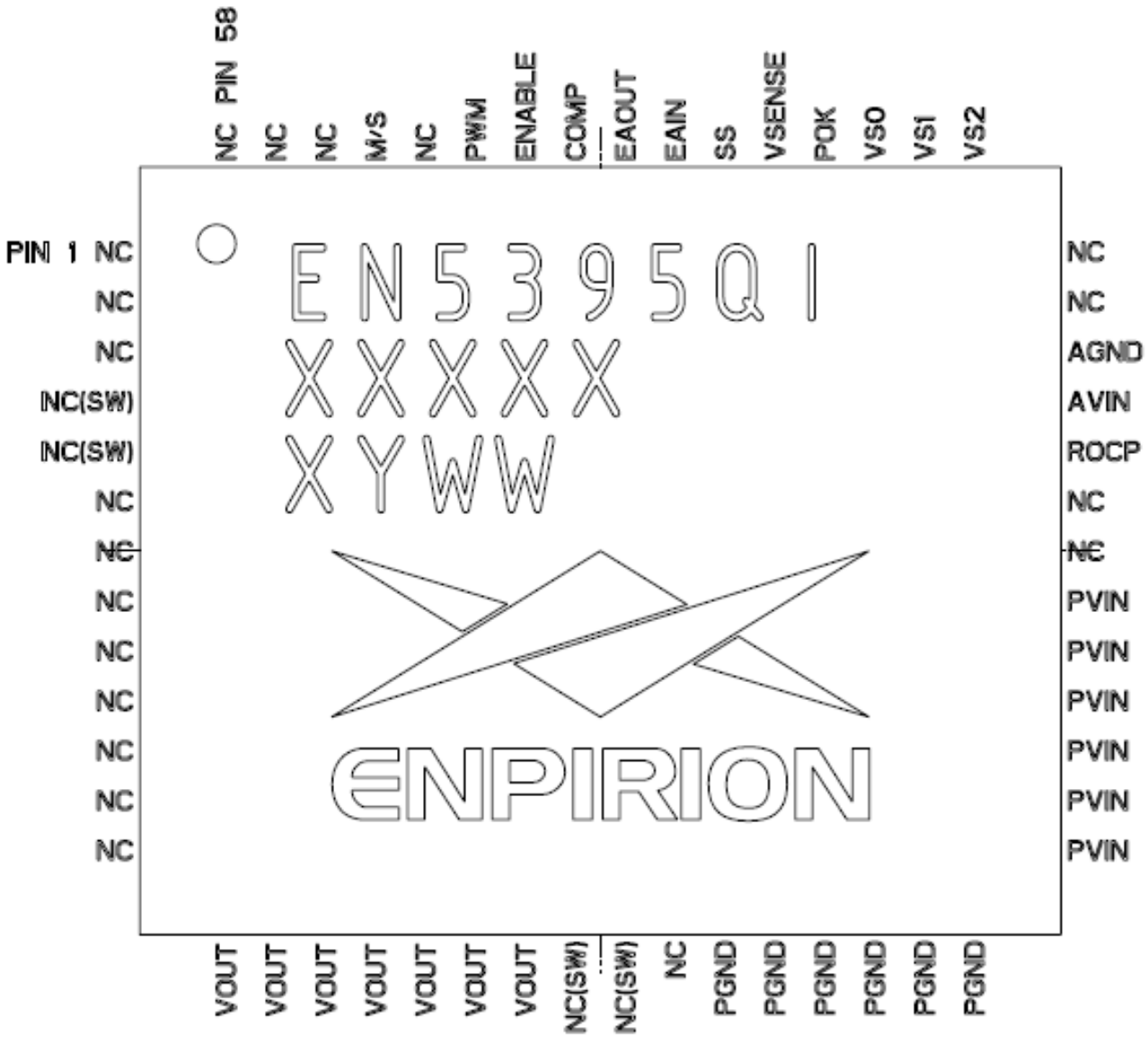


Figure 2. Pin Diagram, top view.

Pin Descriptions

PIN	NAME	FUNCTION
1-3	NC	NO CONNECT – This pin should not be electrically connected to any external signal, voltage, or ground. This pin may be connected internally. However, this pin must be soldered to the PCB.
4-5	NC(SW)	NO CONNECT – These pins are internally connected to the common drain output of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.
6-13	NC	NO CONNECT – This pin should not be electrically connected to any external signal, voltage, or ground. This pin may be connected internally. However, this pin must be soldered to the PCB.
14-20	VOUT	Regulated converter output. Connect these pins to the load and place output capacitor from these pins the PGND pins 24-26.
21-22	NC(SW)	NO CONNECT – These pins are internally connected to the common drain output of the internal MOSFETs. NC(SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.
23	NC	NO CONNECT – This pin should not be electrically connected to any external signal, voltage, or ground. This pin may be connected internally. However, this pin must be soldered to the PCB.
24-29	PGND	Output power ground. Refer to layout guideline section.
30-35	PVIN	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND.
36-37	NC	NO CONNECT – This pin should not be electrically connected to any external signal, voltage, or ground. This pin may be connected internally. However, this pin must be soldered to the PCB.
38	ROCP	Optional Over Current Protection adjust pin. Place ROCP resistor between this pin and AGND (pin 40) to adjust the over current trip point.
39	AVIN	Analog voltage input for the controller circuits. Connect this pin to the input power supply.
40	AGND	Analog ground for the controller circuits.
41-42	NC	NO CONNECT – This pin should not be electrically connected to any external signal, voltage, or ground. This pin may be connected internally. However, this pin must be soldered to the PCB.
43	VS2	Voltage select line 2 input. See Table 1.
44	VS1	Voltage select line 1 input. See Table 1.
45	VS0	Voltage select line 0 input. See Table 1.
46	POK	Power OK is an open drain transistor for power system state indication. POK is a logic high when VOUT is with -10% to +20% of VOUT nominal.
47	VSENSE	Remote voltage sense input. Connect this pin to the load voltage at the point to be regulated.
48	SS	Soft-Start node. The soft-start capacitor is connected between this pin and AGND. The value of this capacitor determines the startup timing.
49	EAIN	Optional Error Amplifier input. Allows for customization of the control loop.
50	EAOUT	Optional Error Amplifier output. Allows for customization of the control loop.
51	COMP	Output of the buffer leading to the error amplifier. Used for external modifications of the compensation network.
52	ENABLE	Input Enable. Applying a logic high, enables the output and initiates a soft-start. Applying a logic low disables the output.
53	PWM	PWM input/output. Used for optional master/slave configuration. When M/S pin is asserted “low”, PWM will output the gate-drive PWM waveform. When the M/S pin is asserted “high”, the PWM pin is configured as an input for PWM signal from the “master” device. PWM pin can drive up to 3 slave devices.
54	NC	NO CONNECT – This pin should not be electrically connected to any external signal, voltage, or ground. This pin may be connected internally. However, this pin must be soldered to the PCB.
55	M/S	Optional Master/Slave select pin. Asserting pin “low” places device in Master Mode for current sharing. PWM pin (53) will output PWM drive signal. Asserting pin “high” will place the device

PIN	NAME	FUNCTION
		in Slave Mode. PWM pin (53) will be configured to input (receive) PWM drive signal from "Master" device.
56-58	NC	NO CONNECT – Do not electrically connect these pins to each other or to PCB. CAUTION! May be internally connected.

Block Diagram

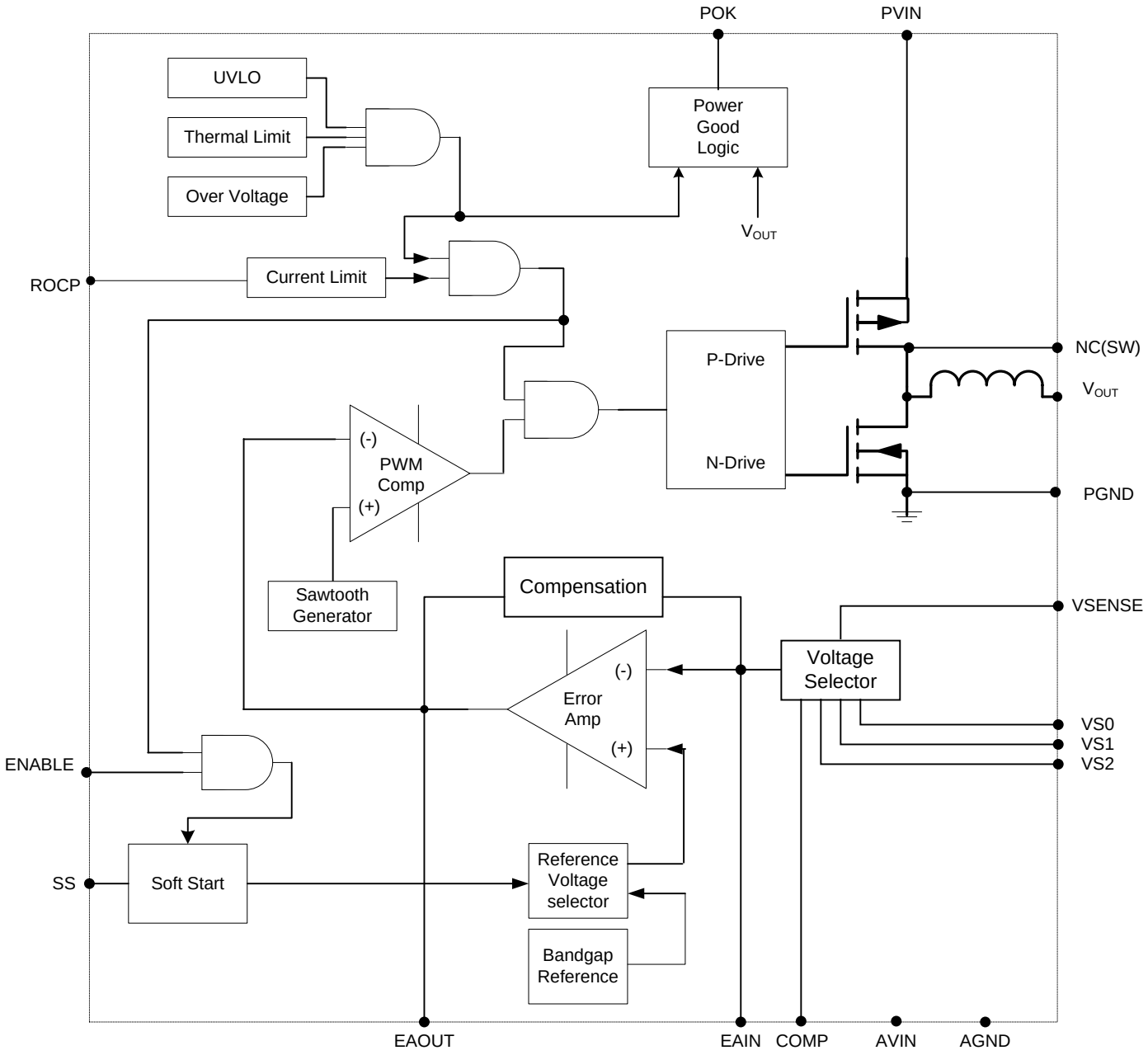


Figure 3. System block diagram.

Absolute Maximum Ratings

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond recommended operating conditions is not implied. Stress beyond absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Supply Voltage	V_{IN}	-0.5	7.0	V
Voltages on: ENABLE, V_{SENSE}, V_{S0}-V_{S2}, M/S		-0.5	V_{IN}	V
Voltages on: EAIN, EAOUT, COMP		-0.5	2.5	
Voltages on: SS, PWM		-0.5	3.0	
Voltages on: POK		-0.5	V_{IN} + 0.3	
Storage Temperature Range	T_{STG}	-65	150	°C
Reflow Temp, 10 Sec, MSL3 JEDEC J-STD-020A			260	°C
ESD Rating (based on Human Body Model)		2000		V

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.375	5.5	V
Output Voltage Range **(NOTE 1)**	V_{OUT}	0.75	V_{IN} - $V_{DROPOUT}$	V
Output Current **(NOTE 2)**	I_{OUT}	0	9	A
Operating Ambient Temperature	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

Note 1: $V_{DROPOUT}$ = I_{LOAD} x Dropout Resistance
Note 2: Reference figures 5 and 6 for the Output Current Derating Curves.

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) **(Note 3)**	θ_{JA}	18	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1.5	°C/W
Thermal Overload Trip Point	T_{J-TP}	+150	°C
Thermal Overload Trip Point Hysteresis		20	°C

Note 3: Based on four layer board and proper thermal design in line with JEDEC EIJ/JESD 51 standards

Electrical Characteristics

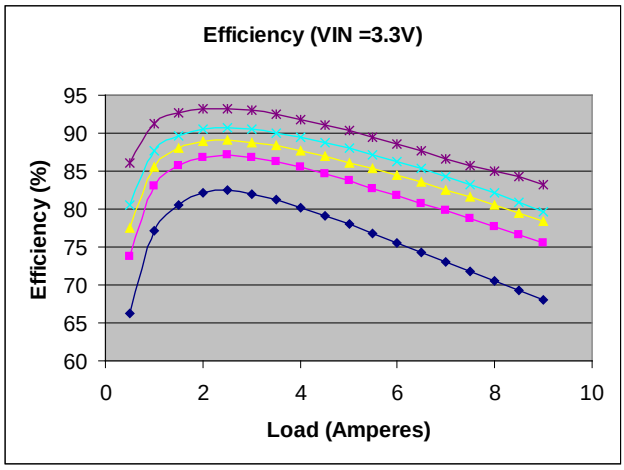
NOTE: V_{IN}=5.5V over operating temperature range unless otherwise noted.
Typical values are at T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT} Initial Accuracy	ΔV_{OUT_INIT}	T_A = 25C, 2.375V ≤ V_{IN} ≤ 5.5V I_{LOAD} = 1A; T_A = 25°C VID Output Voltage Setting (V): 1.2, 1.25, 1.5, 1.8, 2.5, 3.3 0.8	 -2 -3		 +2 +3	%
Overall V_{OUT} Accuracy (Line, Load, and Temperature combined)	ΔV_{OUT_ALL}	2.4V ≤ V_{IN} ≤ 5.5V -40°C ≤ T_A ≤ +85°C 0A ≤ I_{LOAD} ≤ 9A VID Output Voltage Setting (V): 1.2, 1.25, 1.5, 1.8, 2.5, 3.3 0.8	 -3 -4		 +3 +4	%
Transient Response Peak Deviation	ΔV_{OUT}	(I_{OUT} = 0% to 100% or 100% to 0% or rated load)		5		%

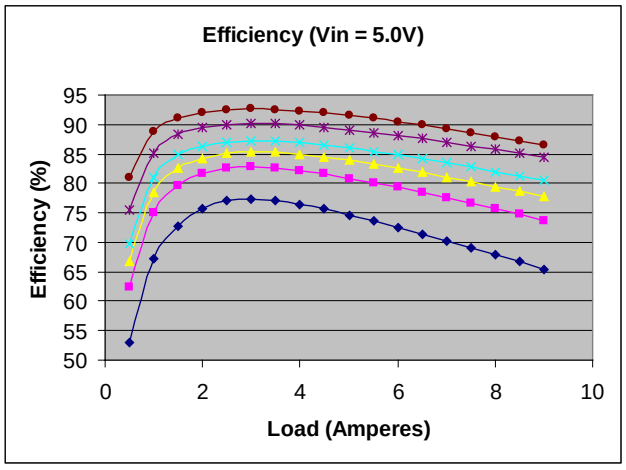
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
		V_{IN} = 5V, 1.2V ≤ V_{OUT} ≤ 3.3V C_{OUT} = 2 x 47 µF				
Under Voltage Lock out threshold	V_{UVLO}	V_{IN} Increasing V_{IN} Decreasing		2.2 2.1		V
Switching Frequency	F_{SWITCH}			5		MHz
Continuous Output Current	I_{OUT}	2.375V ≤ V_{IN} ≤ 5.5V 0.603 <V_{OUT} < V_{IN}-0.5 T_A = -40°C to +60°C *NOTE: reference figures 5 and 6 for the output current derating curves*	9			A
Current Limit Threshold	I_{OCP_TH}			11		A
Shut-Down Supply Current	I_S	ENABLE=0V		50		µA
Disable Threshold	$V_{DISABLE}$	Max voltage to ensure the converter is disabled			0.8	V
Enable Threshold	V_{ENABLE}	2.375V ≤ V_{IN} ≤ 5.5V 5.5V < V_{IN}	1.8 2.0			V
Enable Pin Current	I_{EN}	V_{IN} = 5.5V		50		µA
VS0-VS1, Enable Voltage Threshold	V_{TH}	Pin = Low Pin = High	0.0 1.4		0.4 V_{IN}	
VS0-VS2 Pin Input Current	I_{VSX}	V_{SX} = GND V_{SX} = V_{IN} V_{SX} = Open		50 0 0		µA
POK threshold High		Percentage of V_{OUT} Nominal		120		%
POK threshold Low		Percentage of V_{OUT} Nominal		90		%
POK Low Voltage		I_{POK} = 4mA (Max Sink Current)			0.4	V
POK High Voltage					V_{IN}	V
Dropout Resistance				50		mΩ
Current Balance	ΔI_{OUT}	With 2 – 4 converters in parallel, the difference between any 2 parts. ΔV_{IN} < 50mV; R_{TRACE} < 10mΩ.		+/-10		%

Typical Performance Characteristics

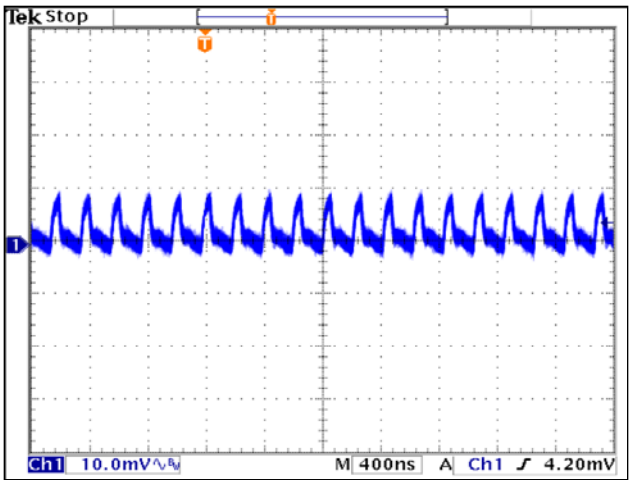
Circuit of Figure 1, V_{IN} = 5 V, V_{OUT} = 1.2 V and T_A = 25°C, unless otherwise noted.



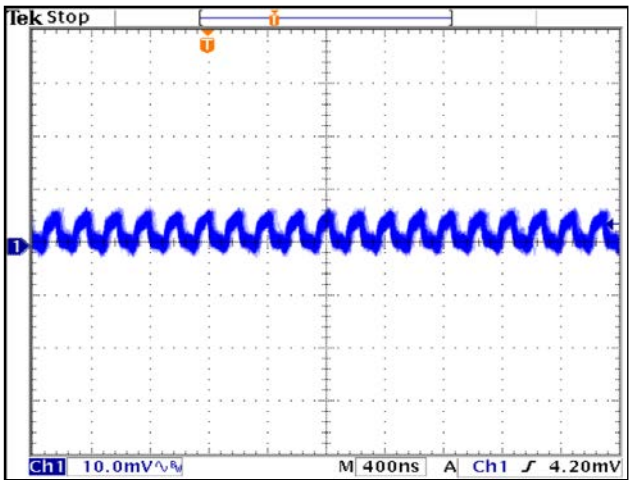
Top to Bottom: V_{OUT} = 2.5 V, 1.8 V, 1.5 V, 1.2 V, 0.8 V



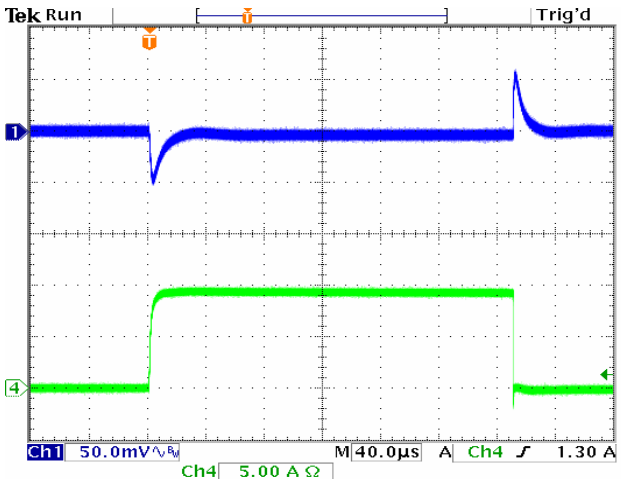
Top to Bottom: V_{OUT} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 0.8 V



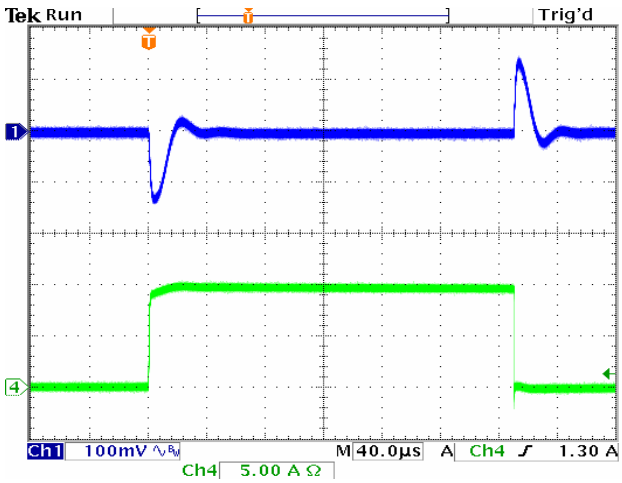
Ripple Voltage, 5.5V_{IN}/1.2V_{OUT}, I_{OUT}=9A, C_{OUT} = 5x22uF.



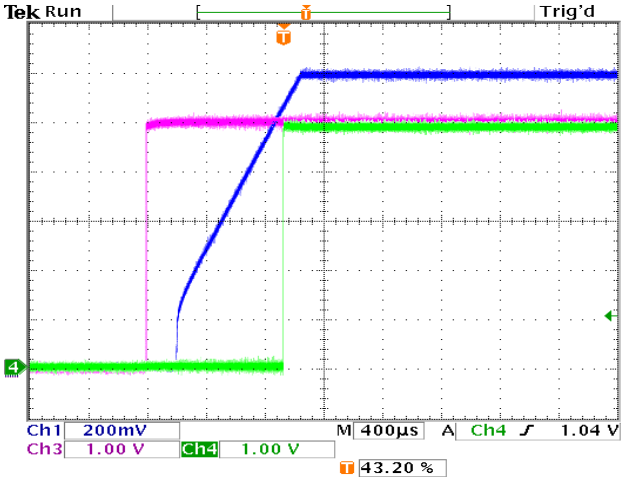
Ripple Voltage, 3.3V_{IN}/1.2V_{OUT}, I_{OUT}=9A, C_{OUT} = 5x22uF.



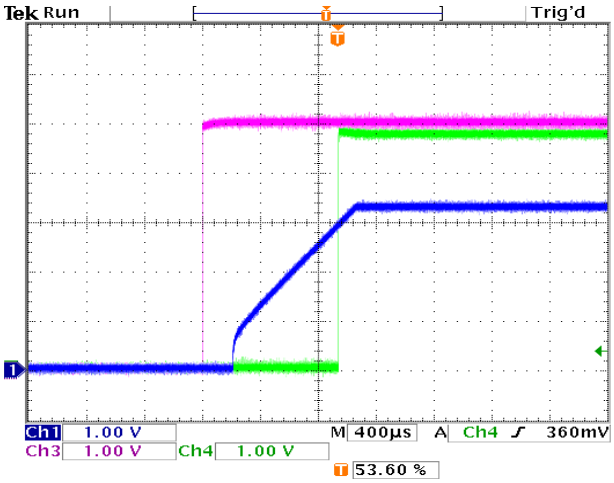
Transient Response: 5V_{IN}/1.2V_{OUT}, 0-9A, 7A/uS. C_{OUT} = 5x22uF.



Transient Response: 5V_{IN}/3.3V_{OUT}, 0-9A, 7A/uS. C_{OUT} = 5x22uF



Start up waveforms V_{IN}=5.0V, V_{OUT}=1.2V, C_{SS}=15nF, Ch 1 = V_{OUT}, Ch 3 = ENABLE, Ch 4 = POK.



Start up waveforms V_{IN}=5.0V, V_{OUT}=3.3V, C_{SS}=15nF, Ch 1 = V_{OUT}, Ch 3 = ENABLE, Ch 4 = POK.

Functional Description

The EN5395QI is a synchronous, pin programmable power supply with integrated power MOSFET switches and integrated inductor. The nominal input voltage range is 2.375-5.5V. The output can be set to common pre-set voltages by connecting appropriate combinations of 3 voltage selection pins to ground. The feedback control loop is a type III voltage-mode and the part uses a low-noise PWM topology. Up to 9A of output current can be drawn from this converter. The 5MHz operating frequency enables the use of small-size output capacitors.

The power supply has the following protection features:

- Programmable over-current protection (to protect the IC from excessive load current)
- Thermal shutdown with hysteresis.
- Over-voltage protection
- Under-voltage lockout circuit to disable the converter output when the input voltage is less than approximately 2.2V

Additional features include:

- Soft-start circuit, limiting the in-rush current when the converter is powered up.
- Power good circuit indicating whether the output voltage is within 90%-120% of the programmed voltage.

Output Voltage Programming

The EN5395QI output voltage is programmed using a 3-pin voltage-ID or VID selector. Three binary VID pins allow the user to choose one of seven pre-set voltages. Refer to table 1 for the proper VID pin settings to program V_{OUT}.

The voltage select pins, VS0, VS1, and VS2, are pulled-up internally and so will default to a logic high, or “1”, if left “open”. Connecting the voltage select pin to ground will result in a logic “0”.

Table 1: Output Voltage Select Table

VS2*	VS1*	VS0*	Output Voltage
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V
1	1	1	Reserved

Input Capacitor Selection

The EN5395QI requires between 40-80uF of input capacitance. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these lose capacitance with frequency, temperature and bias voltage.

In some applications, lower value capacitors are needed in parallel with the larger, capacitors in order to provide high frequency decoupling.

Table 2. Recommended input capacitors.

Description	MFG	P/N
22uF, 10V, X7R, 1210	Murata	GRM32ER71A226KE20L
	Taiyo Yuden	LMK325B7226KM-T
47uF, 10V, X5R, 1210	Murata	GRM32ER61A476KE20L
	Taiyo Yuden	LMK325BJ476KM-T

Output Capacitor Selection

The EN5395QI has been optimized for use with approximately 100µF of output capacitance. Low ESR ceramic capacitors are required with X5R or X7R rated dielectric formulation. Y5V or equivalent dielectric formulations must not be used as these loose capacitance with frequency, temperature and bias voltage.

Table 3. Recommended output capacitors.

Description	MFG	P/N
10uF, 10V, X7R, 1206	Murata	GRM31CR71A106KA01L
	Taiyo Yuden	LMK316B7106KL-T
22uF, 6.3V, X5R, 1206	Murata	GRM31CR60J226KE19L
	Taiyo Yuden	LMK316BJ226KL-T
47uF, 6.3V, X5R, 1206	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK316BJ476ML-T

Output ripple voltage is determined by the aggregate output capacitor impedance. Output impedance, denoted as Z, is comprised of effective series resistance, ESR, and effective series inductance, ESL:

Z = ESR + ESL.

Placing output capacitors in parallel reduces the impedance and will hence result in lower ripple voltage.

$$\frac{1}{Z_{Total}} = \frac{1}{Z_1} + \frac{1}{Z_2} + ... + \frac{1}{Z_n}$$

Typical ripple versus capacitor arrangement is given below ($5.5V_{IN}/1.2V_{OUT}$):

Output Capacitor Configuration	Typical Output Ripple (mVp-p) (as measured on EN5395QI Evaluation Board)
2 x 47uF	20
5 x 22 uF	12

Enable Operation

The ENABLE pin provides a means to shut down the device, or enable normal operation. A logic low will disable the converter and cause it to shut down. A logic high will enable the converter into normal operation. When the ENABLE pin is asserted high, the device will undergo a normal soft start.

Soft-Start Operation

Soft start is a method to reduce in-rush current when the device is enabled. The output voltage is ramped up slowly upon start-up. The output rise time is controlled by choice of a soft-start capacitor, which is placed between the SS pin (pin 48) and the AGND pin (pin 40).

Rise Time: $T_R = C_{ss} * 80K\Omega$

During start-up of the converter, the reference voltage to the error amplifier is gradually increased to its final level by an internal current source of typically 10uA. Typical soft-start rise time is 1mS to 3mS. Typical SS capacitor values are in the range of 15nF to 30 nF.

Startup into Pre-Bias

The EN5395QI supports startup into a pre-biased output of up to 1.5V. The output of the EN5395QI can be pre-biased with a voltage up to 1.5V when it is first enabled.

POK Operation

The POK signal is an open drain signal from the converter indicating the output voltage is within the specified range. The POK signal will be a logic high when the output voltage is within 90% - 120% of the programmed output voltage. If the output voltage goes outside of this range, the POK signal will be a logic low until the output voltage has returned to within this range. In the event of an over-voltage condition the POK signal will go low and will remain in this condition until the output voltage has dropped to 95% of the programmed output voltage before returning to the high state.

The internal POK FET is designed to tolerate up to 4mA. The pull-up resistor value should be chosen to limit the current from exceeding this value when POK is logic low.

Over-Current Protection

When an over current condition occurs, V_{OUT} is pulled low. This condition is maintained for a period of 1.2 ms and then a normal soft start cycle is initiated. If the over current condition still persists, this cycle will repeat.

The OCP trip point is nominally set to 150% of maximum rated load. It is possible to increase the OCP trip point to 200% of the maximum rated load by connecting a 5kΩ resistor between the ROCP pin (pin 38) and AGND (pin 40). This

option is intended for startup into capacitive loads such as certain FPGAs and ASICs.

Over-Voltage Protection

When the output voltage exceeds 120% of the programmed output voltage, the PWM operation stops, the lower N-MOSFET is turned on and the

POK signal goes low. When the output voltage drops below 95% of the programmed output voltage, normal PWM operation resumes and POK returns to its high state.

Thermal Overload Protection

Thermal shutdown will disable operation once the Junction temperature exceeds approximately 150ºC. Once the junction temperature drops by approx. 20ºC, the converter will re-start with a normal soft-start.

Input Under-voltage Lock-out

Circuitry is provided to ensure that when the input voltage is below the specified voltage range, the converter will not start-up. Circuits for hysteresis, input de-glitch and output leading edge blanking are included to ensure high noise immunity and prevent false tripping.

Compensation

The EN5395 is internally compensated through the use of a type 3 compensation network and is optimized for use with about 100µF of output capacitance and will provide excellent loop bandwidth and transient performance for most applications. (See the section on Capacitor Selection for details on recommended capacitor types.) Voltage mode operation provides high noise immunity at light load.

In some cases modifications to the compensation may be required. The EN5395QI provides access to the internal compensation network to allow for customization. For more information, contact Power Applications support.

Parallel Device Operation

In order to power a load that is higher than the rated 9A of the EN5395, from 2 to 4 devices can be placed in parallel for providing a single load with up to 36A of output current.

Paralleling more than 1 device is accomplished by selecting a master device and tying that M/S pin to AGND. All slave devices should have their M/S pin tied to AVIN. The PWM pin from the master device is connected to all slave device PWM pins. The PWM signal is a 5 MHz drive signal and must be routed appropriately. (See Figure 4.)

1. All master and slave devices should have identical placement and values of input, output and soft-start capacitors.
2. All master and slave devices should have their ENABLE pins tied together and should be operated simultaneously with a fast rising edge of 10 uSec or less, to ensure that devices start up at the same time. Startup imbalance could lead to OCP condition on first device to startup.
3. The maximum board trace resistance between any 2 devices VOUT pins should be less than 10mΩ.
4. The maximum difference of PVIN between any 2 devices should be less than 50mV.

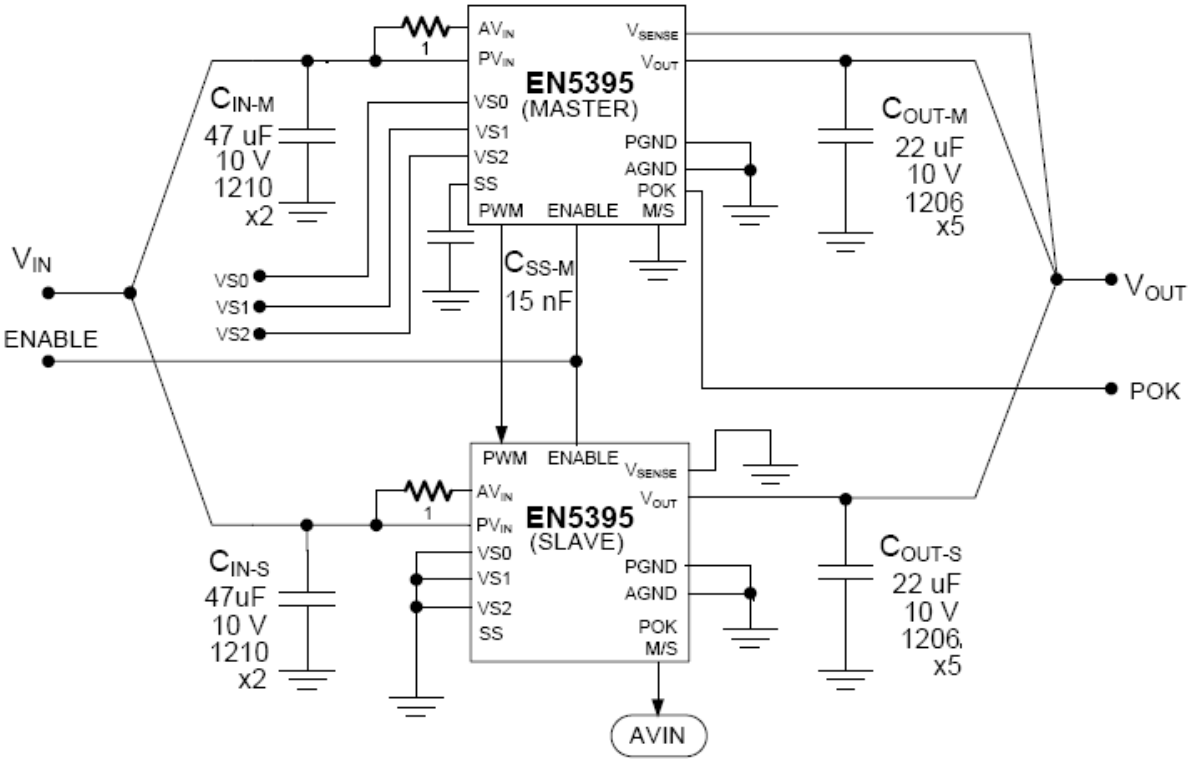


Figure 4 . Paralleling of two devices.

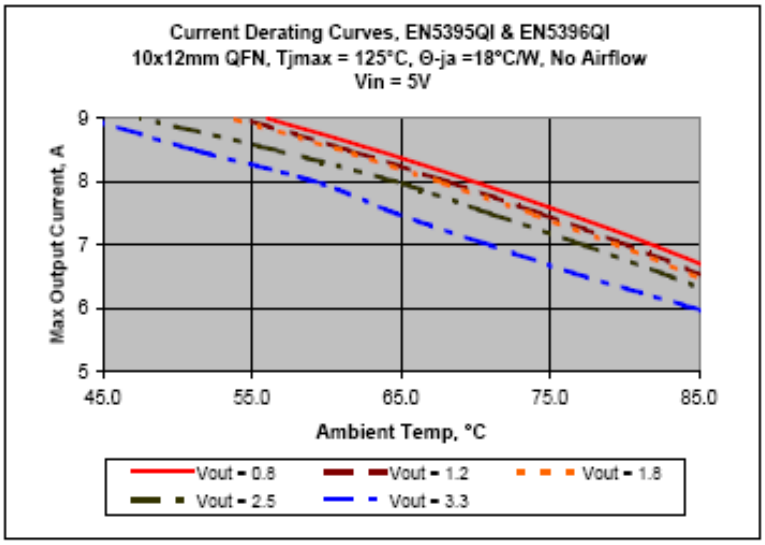


Figure 5. Output Current Derating Curve, V_{IN} = 5.0V

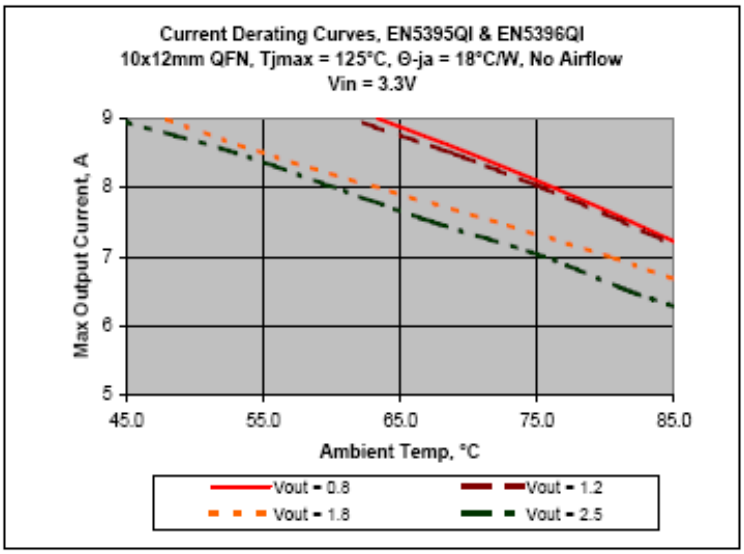


Figure 6 . Output Current De-rating Curve, V_{IN} = 3.3V

Layout Recommendations

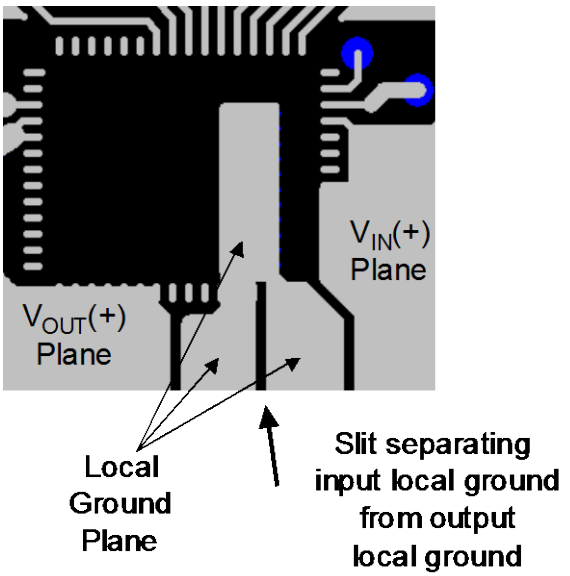


Figure 7. Layout of power and ground planes.

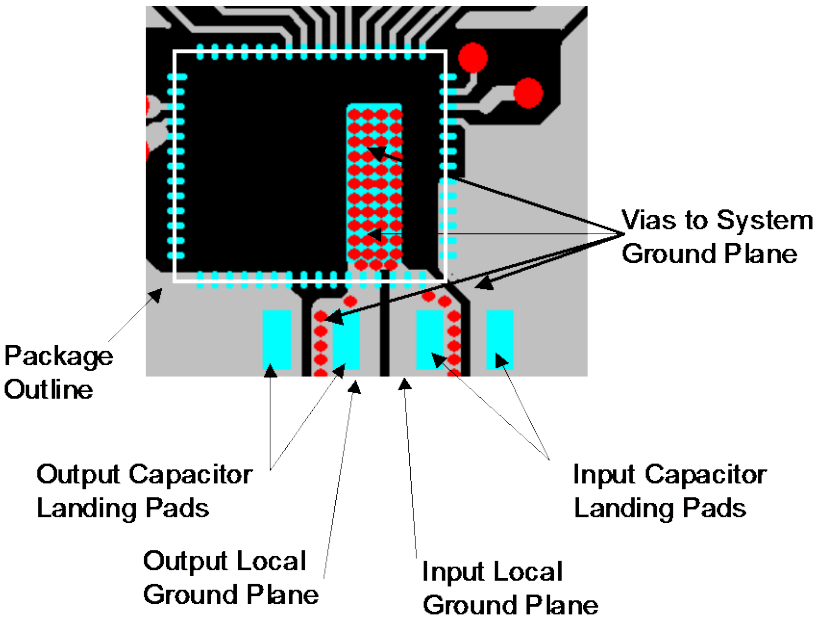


Figure 8. Use of vias connecting local and system ground.

Recommendation 1: Input and output capacitors should be placed as close to the EN5395QI package as possible to reduce EMI from input and output loop currents. This reduces the physical area of the Input and Output AC current loops.

Recommendation 2: Place a slit in the input/output capacitor ground plane just beyond the common connection point of the GND pins of the device as shown in figure 7.

Recommendation 3: Multiple small (0.25mm) vias should be used to connect ground terminal of the Input capacitor and the output capacitor to the system ground plane as shown in figure 8.

Recommendation 4: The large thermal pad underneath the component must be connected to the system ground plane through as many vias as possible. The diameter of the vias should be less than 0.3mm. This provides the quiet, or analog ground for the converter and also provides the path for heat dissipation from the converter. A later section of this note makes a recommendation on the PCB footprint.

Recommendation 5: The system ground plane referred to in recommendations 3 and 4 should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input and output capacitors that carry large AC currents.

Recommendation 6: As with any switch-mode DC/DC converter, do not run sensitive signal or control lines underneath the converter package.

Design Considerations for Lead-Frame Based Modules

Exposed Metal on Bottom of Package

Lead frame offers many advantages in thermal performance, in reduced electrical lead resistance, , and in overall foot print. However, they do require some special considerations.

In the assembly process lead frame construction requires that, for mechanical support, some of the lead-frame cantilevers be exposed at the point where wire-bond or internal passives are attached. This results in several small pads being exposed on the bottom of the package.

Only the large thermal pad and the perimeter pads are to be mechanically or electrically connected to the PC board. The PCB top layer under the EN5395QI should be clear of any metal except for the large thermal pad. The “grayed-out” area in Figure 9 represents the area that should be clear of any metal (traces, vias, or planes), on the top layer of the PCB.

Figure 10 demonstrates the recommended PCB footprint for the EN5395QI. Figure 11 shows the shape and location of the exposed metal pads as well as the mechanical dimension of the large thermal pad and the pins.

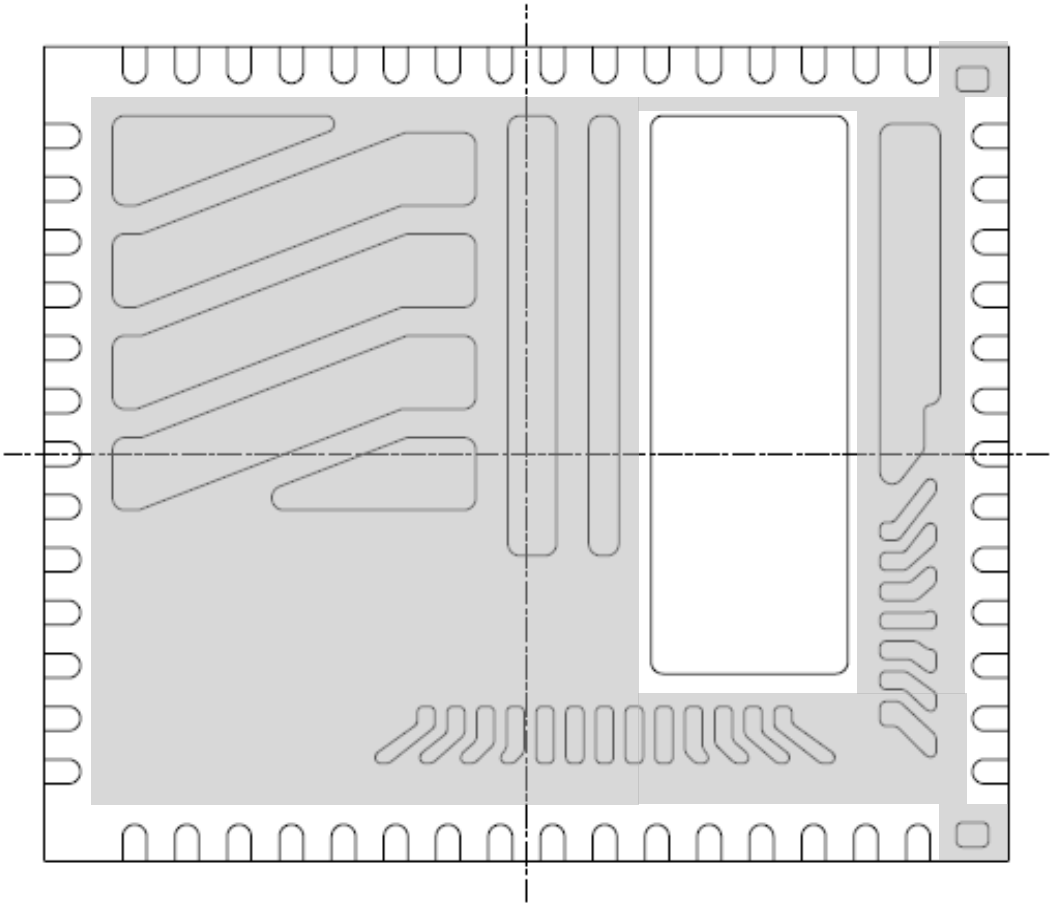


Figure 9. Lead-Frame exposed metal. Grey area highlights exposed metal that is not to be mechanically or electrically connected to the PCB.

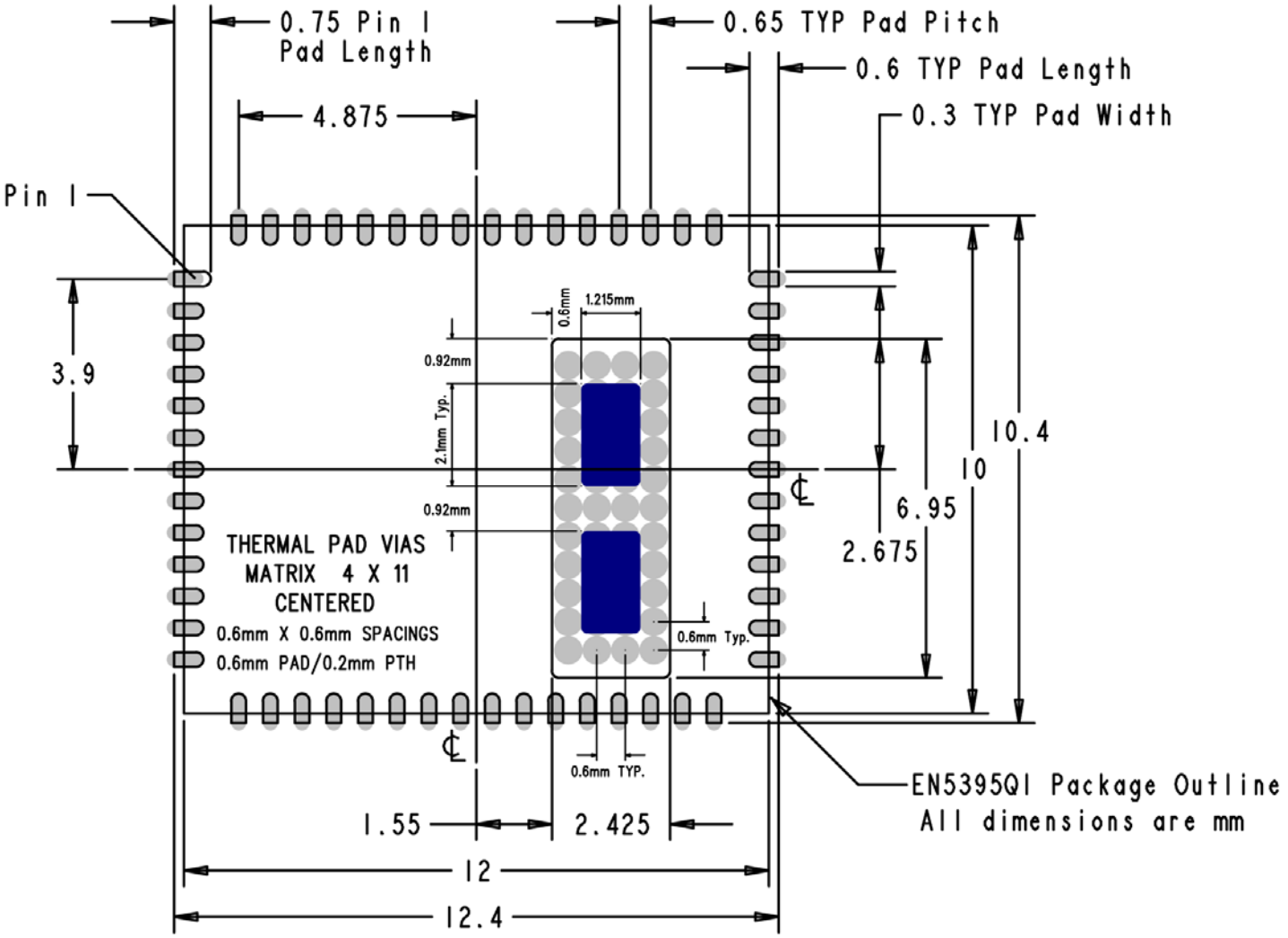


Figure 10. EN5395QI PCB Footprint (Top View)

The solder stencil aperture for the thermal pad is shown in blue and is based on Enpirion power product manufacturing specifications.

Package Dimensions

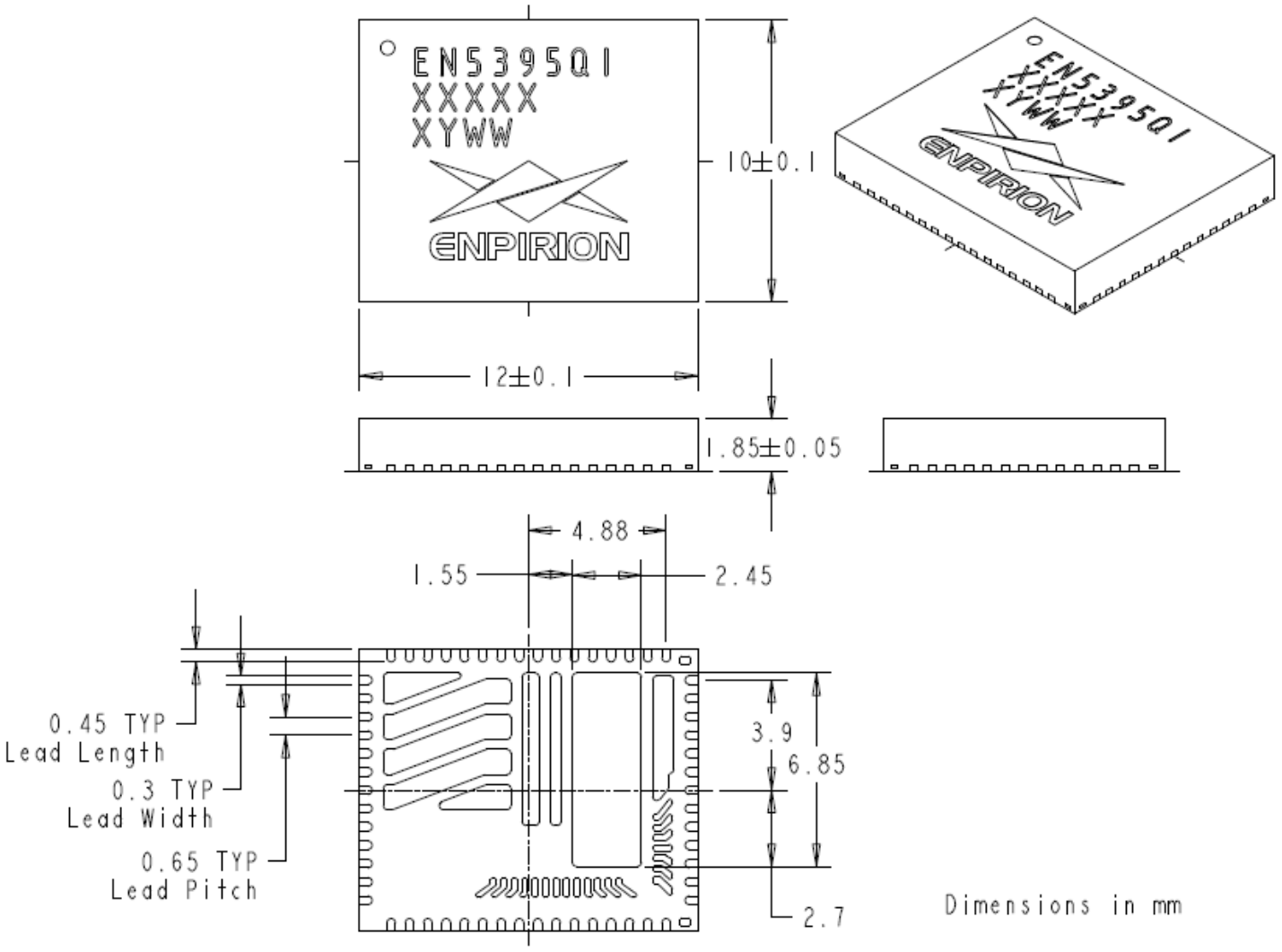


Figure 11. Package dimensions.

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