

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

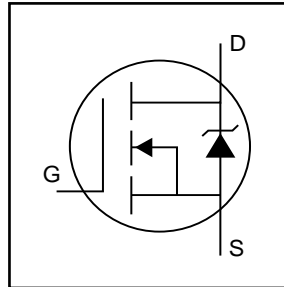
The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---------------------------------|---|--------------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 140 ^⑤ | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 98 ^⑤ | |
| I_{DM} | Pulsed Drain Current ^① | 470 | |
| $P_D @ T_C = 25^\circ\text{C}$ | Power Dissipation | 200 | W |
| | Linear Derating Factor | 1.3 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ±16 | V |
| E_{AS} | Single Pulse Avalanche Energy ^② | 610 | mJ |
| I_{AR} | Avalanche Current ^④ | 71 | A |
| E_{AR} | Repetitive Avalanche Energy ^④ | 20 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ^③ | 5.0 | V/ns |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | | |
| | Mounting torque, 6-32 or M3 screw. | 10 lbf•in (1.1N•m) | |

Thermal Resistance

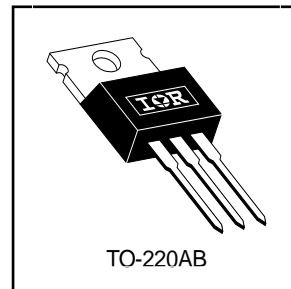
| | Parameter | Min. | Typ. | Max. | Units |
|-----------------|-------------------------------------|------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | — | 0.75 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | — | 0.50 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | — | 62 | |



$$V_{DSS} = 30\text{V}$$

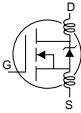
$$R_{DS(on)} = 0.006\Omega$$

$$I_D = 140\text{A}^{\text{⑤}}$$



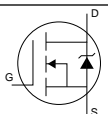
Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|-------|-------|---------------------|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 30 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.052 | — | V/ $^\circ\text{C}$ | Reference to 25°C , $I_D = 1\text{mA}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.006 | Ω | $V_{GS} = 10V, I_D = 71A$ ④ |
| | | — | — | 0.009 | | $V_{GS} = 4.5V, I_D = 59A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | — | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| g_{fs} | Forward Transconductance | 55 | — | — | S | $V_{DS} = 25V, I_D = 71A$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | $V_{DS} = 30V, V_{GS} = 0V$ |
| | | — | — | 250 | | $V_{DS} = 24V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 16V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS} = -16V$ |
| Q_g | Total Gate Charge | — | — | 140 | nC | $I_D = 71A$ |
| Q_{gs} | Gate-to-Source Charge | — | — | 41 | | $V_{DS} = 24V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 78 | | $V_{GS} = 4.5V$, See Fig. 6 and 13 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 14 | — | ns | $V_{DD} = 15V$ |
| t_r | Rise Time | — | 230 | — | | $I_D = 71A$ |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 29 | — | | $R_G = 1.3\Omega, V_{GS} = 4.5V$ |
| t_f | Fall Time | — | 35 | — | | $R_D = 0.20\Omega$, See Fig. 10 ④ |
| L_D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L_S | Internal Source Inductance | — | 7.5 | — | | |
| C_{iss} | Input Capacitance | — | 5000 | — | pF | $V_{DS} = 0V$ |
| C_{oss} | Output Capacitance | — | 1800 | — | | $V_{DS} = 25V$ |
| C_{rss} | Reverse Transfer Capacitance | — | 880 | — | | $f = 1.0\text{MHz}$, See Fig. 5 |



Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|---|------|------|-------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 140 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 470 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 71A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 120 | 180 | ns | $T_J = 25^\circ\text{C}, I_F = 71A$ |
| Q_{rr} | Reverse Recovery Charge | — | 450 | 680 | nC | $di/dt = 100A/\mu s$ ④ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$) | | | | |



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 15V$, starting $T_J = 25^\circ\text{C}$, $L = 180\mu H$
 $R_G = 25\Omega$, $I_{AS} = 71A$. (See Figure 12)
- ③ $I_{SD} \leq 71A$, $di/dt \leq 130A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

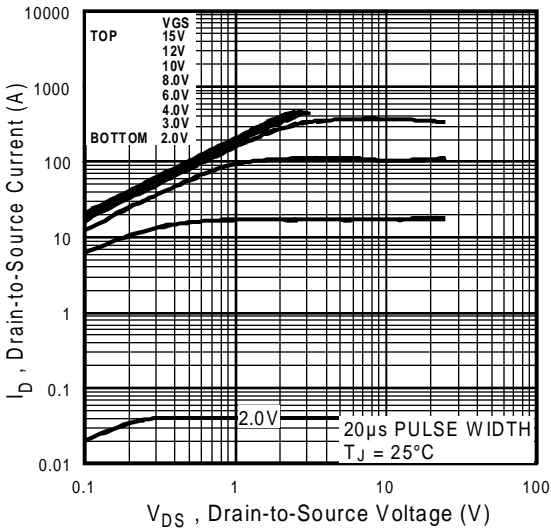


Fig 1. Typical Output Characteristics

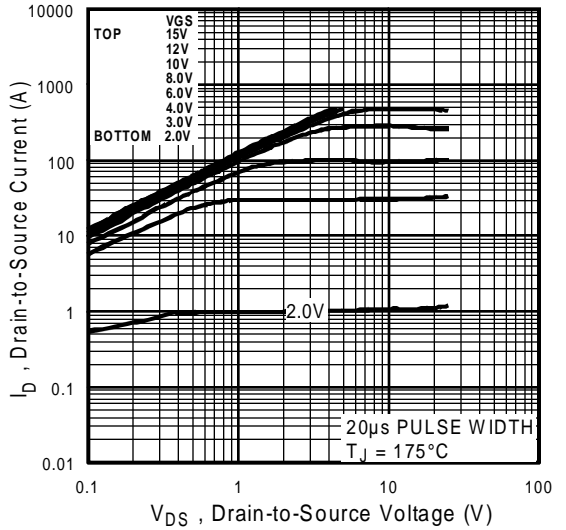


Fig 2. Typical Output Characteristics

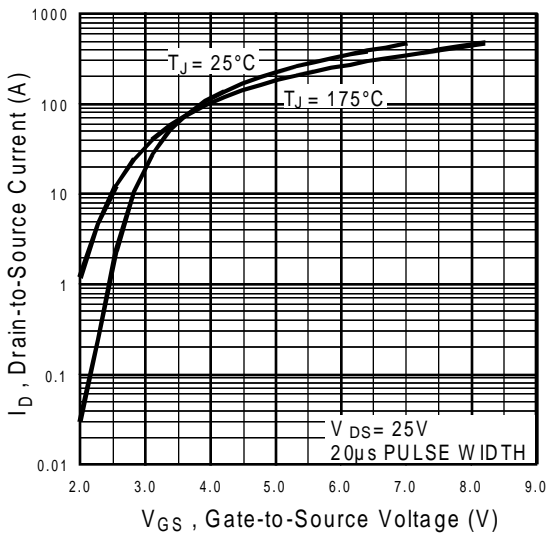


Fig 3. Typical Transfer Characteristics

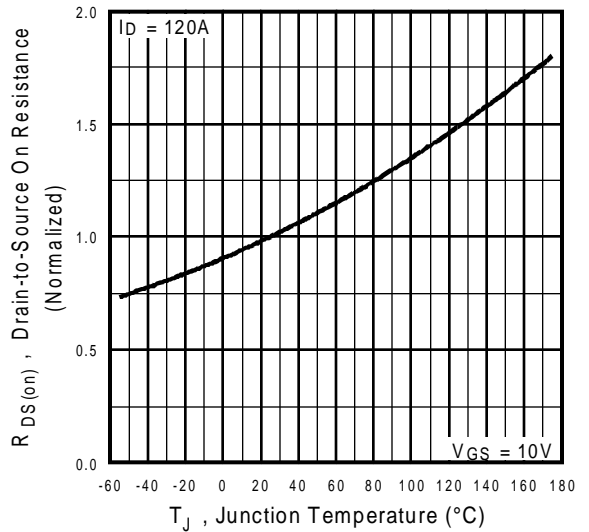


Fig 4. Normalized On-Resistance Vs. Temperature

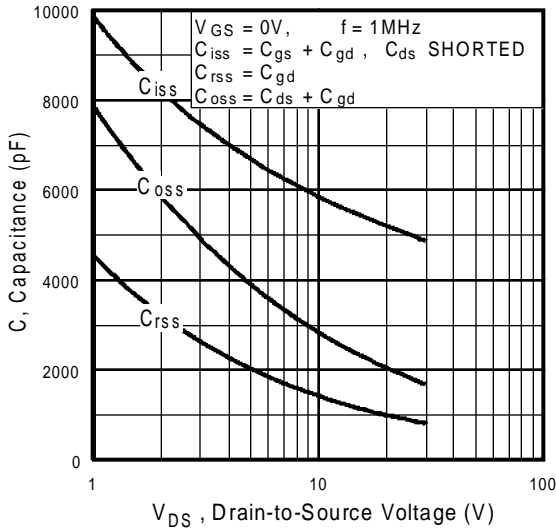


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

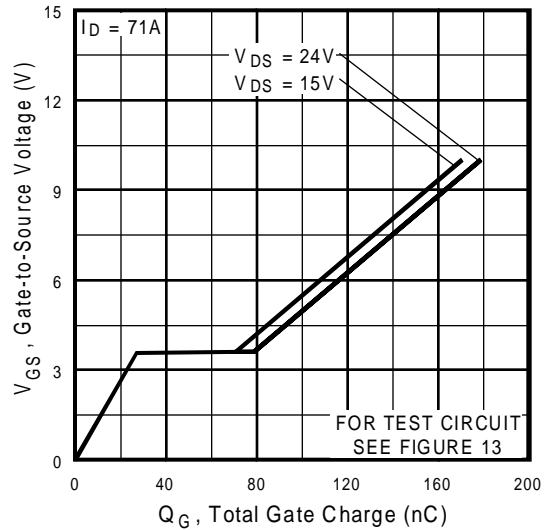


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

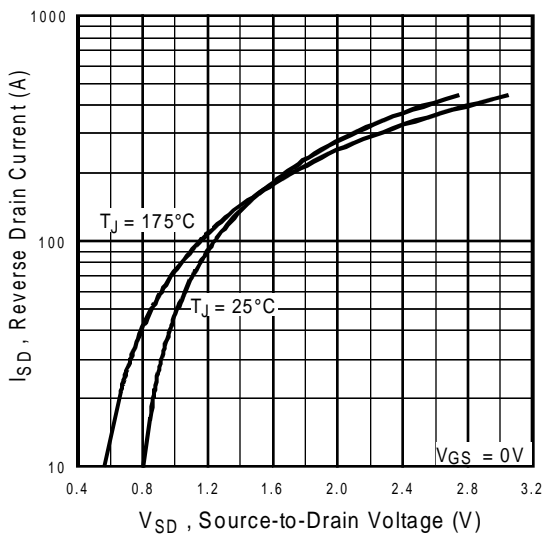


Fig 7. Typical Source-Drain Diode Forward Voltage

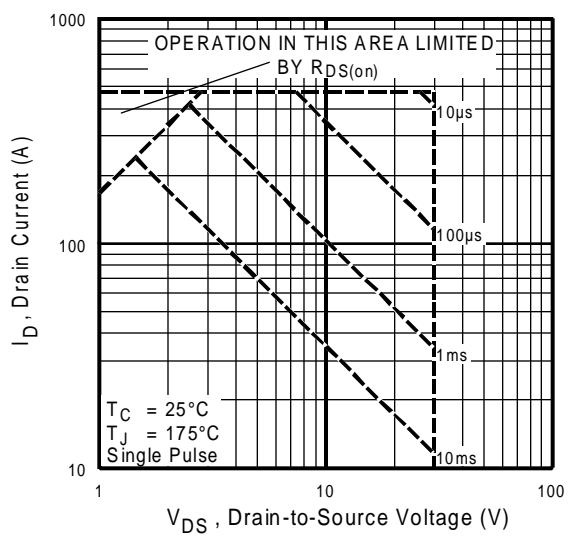


Fig 8. Maximum Safe Operating Area

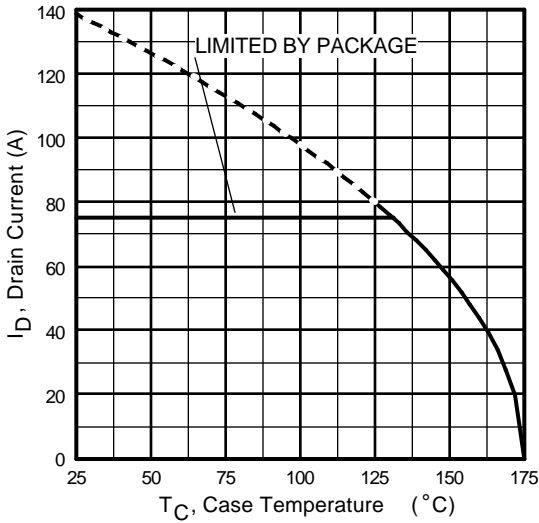


Fig 9. Maximum Drain Current Vs. Case Temperature

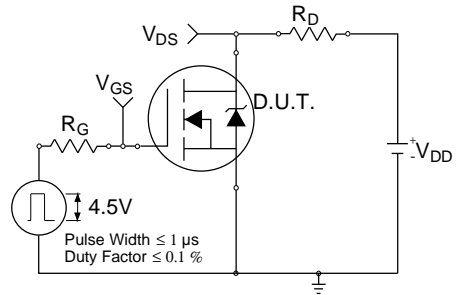


Fig 10a. Switching Time Test Circuit

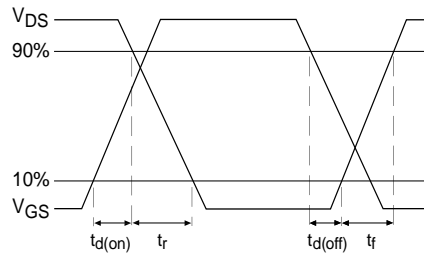


Fig 10b. Switching Time Waveforms

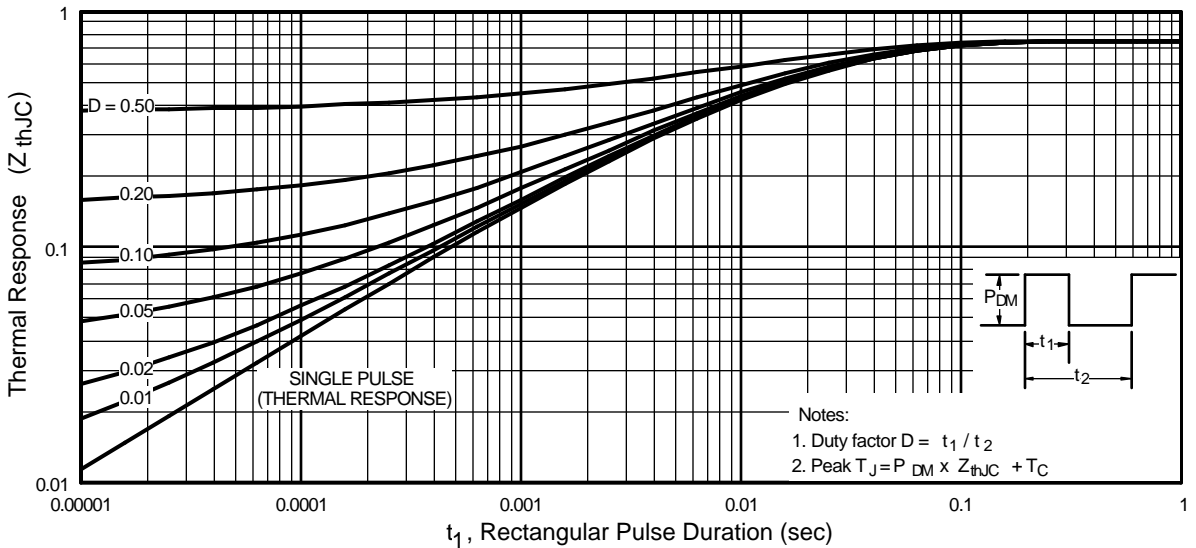


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

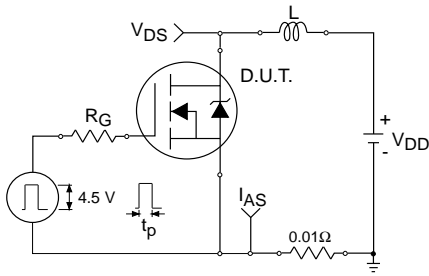


Fig 12a. Unclamped Inductive Test Circuit

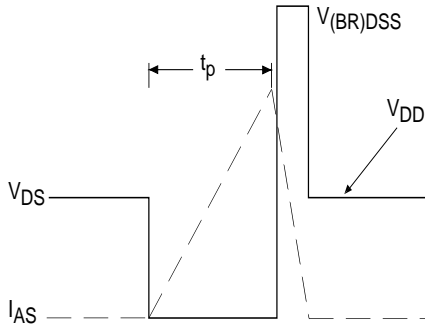


Fig 12b. Unclamped Inductive Waveforms

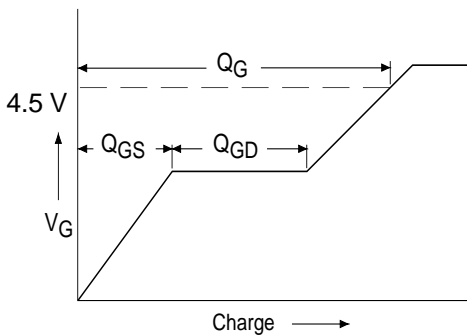


Fig 13a. Basic Gate Charge Waveform

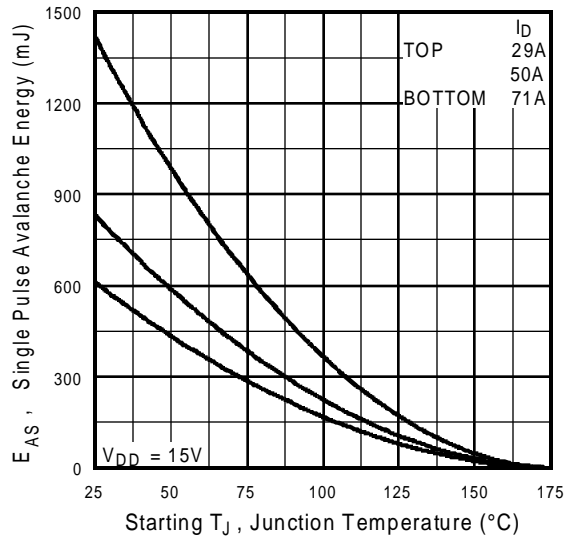


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

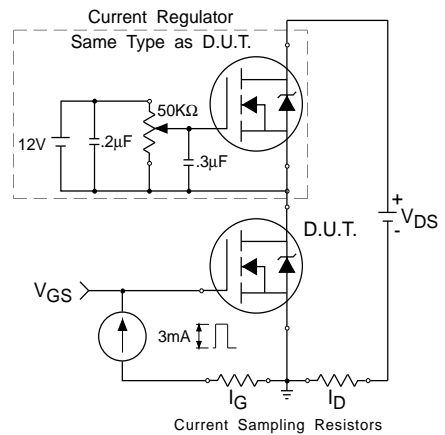
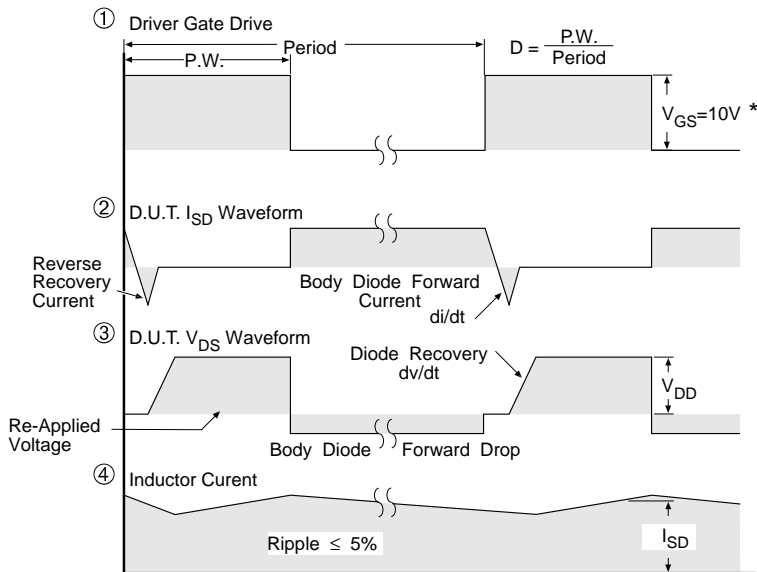
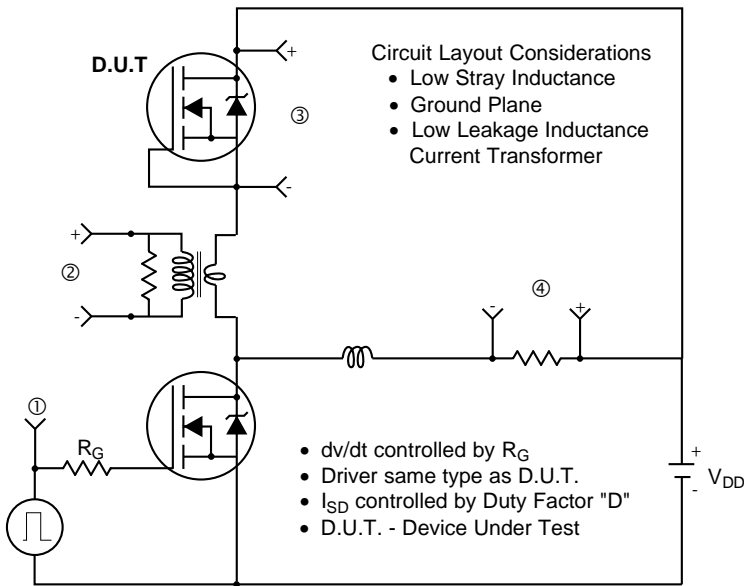


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



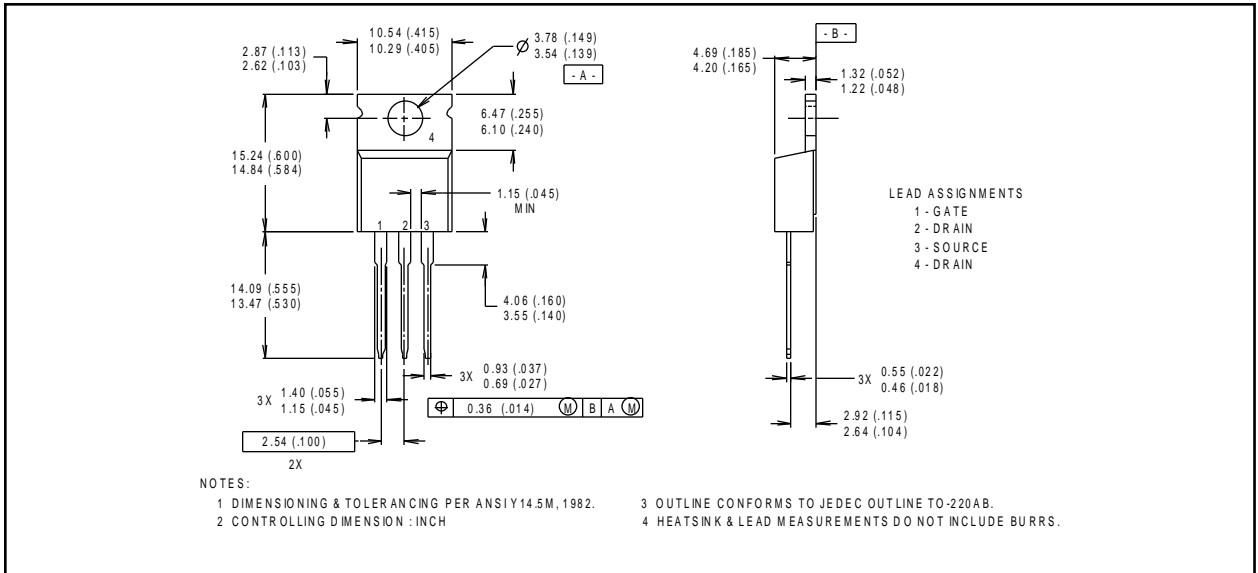
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-220AB Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M

