High and Low Side Driver

PRODUCT SUMMARY

- **V_{OFFSET}** 600 V max.
- **I_O+/-** 450mA/950mA
- **V_{OUT}** 10 V - 20 V
- **$t_{on/off}$ (typ.)** 160 ns/220 ns
- **Delay matching** 30ns

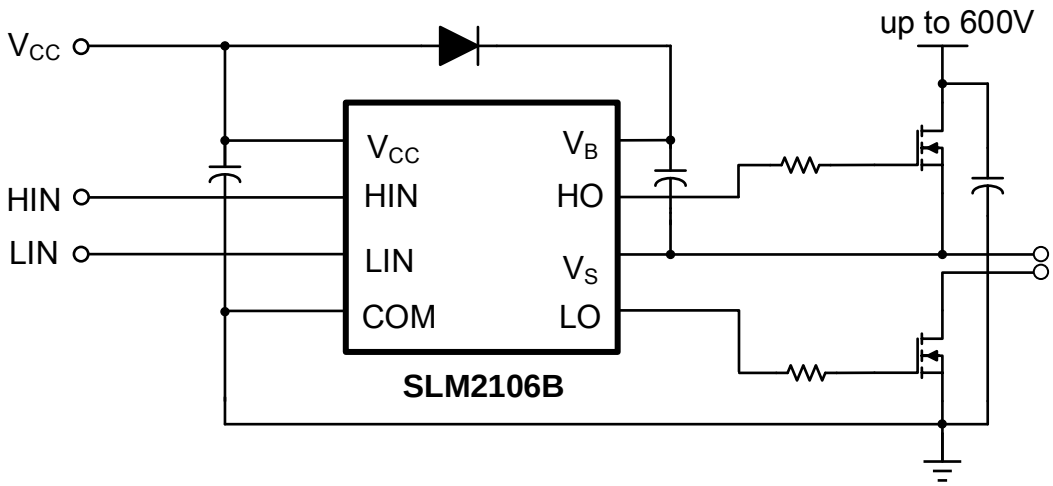
GENERAL DESCRIPTION

The SLM2106B is a high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

FEATURES

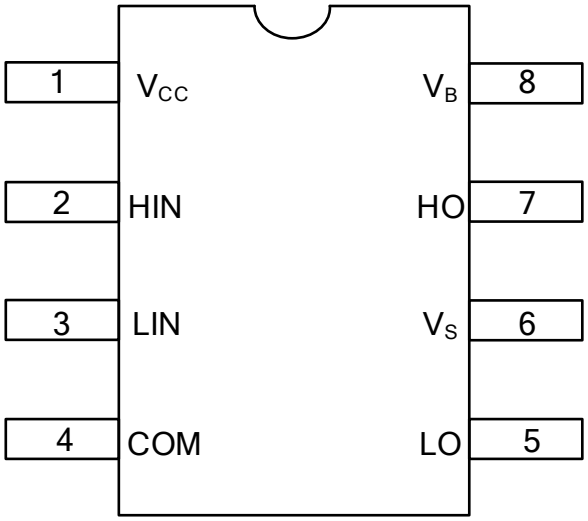
- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V logic compatible
- Matched propagation delay for both channels
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- RoHS compliant
- SOP8 package

TYPICAL APPLICATION CIRCUIT



Refer to Lead Assignments for correct configuration. This diagram shows electrical connections only.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
SOP8	

PIN DESCRIPTION

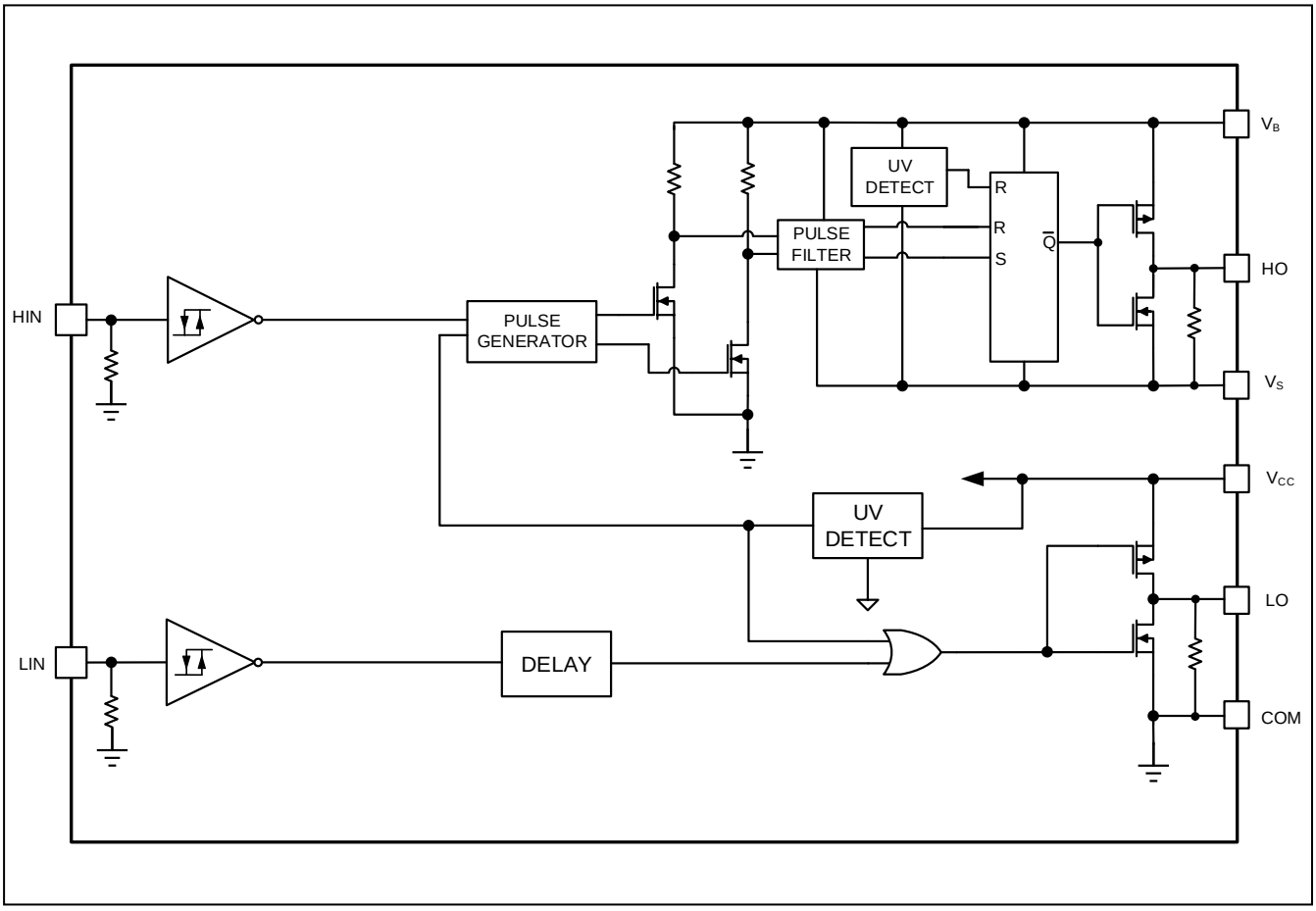
No.	Pin	Description
1	V_{CC}	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	LIN	Logic input for low-side gate driver output (LO), in phase
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	VB	High-side floating supply

ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM2106BCA-13GTR	SOP8, Pb-Free	2500/Reel

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	-0.3	625	V
V_S	High-side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side and logic fixed supply voltage	-0.3	25	
V_{LO}	Low-side output voltage	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient	---	50	V/ns
P_D	Package power dissipation @ $T_A \leqslant +25°C$	---	0.625	W
θ_{JA}	Thermal resistance, junction to ambient	---	200	°C/W
T_J	Junction temperature	---	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	---	300	

Note: Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATION CONDITIONS

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating absolute voltage	V_S + 10	V_S + 20	V
V_S	High-side floating supply offset voltage		600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side and logic fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	V_{SS}	V_{CC}	
T_A	Ambient temperature	- 40	125	°C

Note: The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	---	160	220	ns
t_{off}	Turn-off propagation delay	V_S = 0 V or 600 V	---	220	270	
t_r	Turn-on rise time	V_S = 0 V	---	45	100	
t_f	Turn-off fall time		---	18	40	
MT	Delay matching, HS & LS turn-on/off		---	---	30	

STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM and are applicable to all logic input leads: HIN and LIN. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH}	Logic “1” input voltage	V_{CC} = 10 V to 20V	2.5	---	---	V
V_{IL}	Logic “0” input voltage		---	---	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2 mA	---	0.04	0.1	
V_{OL}	Low level output voltage, V_O		---	0.01	0.08	
I_{LK}	Offset supply leakage current	V_B = V_S = 600 V	---	---	50	µA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V		60	78	
I_{QCC}	Quiescent V_{CC} supply current			230	305	
I_{IN+}	Logic “1” input bias current V_{IN} = 5 V		---	8	15	
I_{IN-}	Logic “0” input bias current V_{IN} = 0 V		---	---	5	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		7.2	8.0	8.9	V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		6.4	7.4	8.0	
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold		6.4	7.2	8.0	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold		5.8	6.6	7.4	
I_{O+}	Output high short circuit pulsed current	V_O = 0 V, PW ⩽ 10 µs	320	450		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15 V, PW ⩽ 10 µs	680	950		

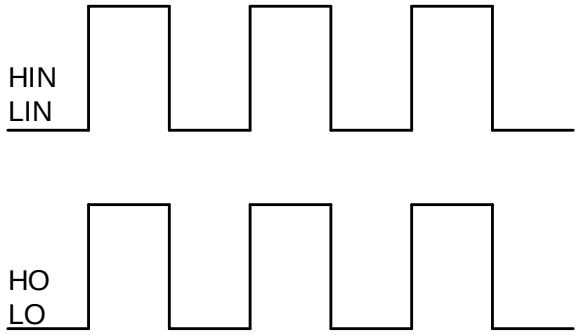


Figure 1. Input/Output Timing Diagram

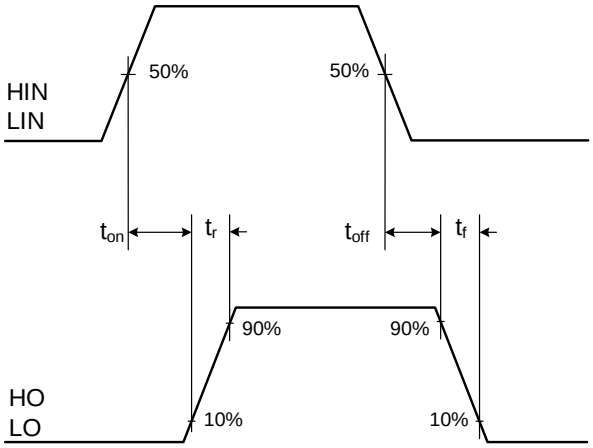


Figure 2. Switching Time Waveform

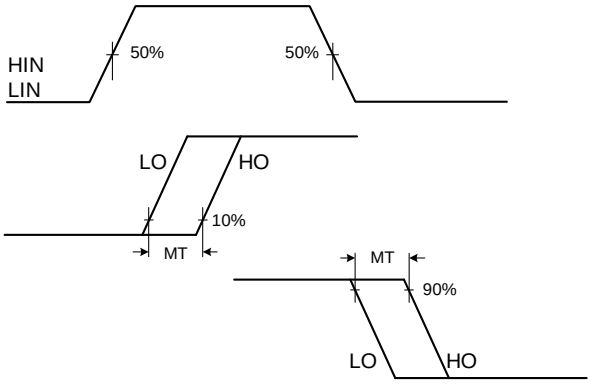
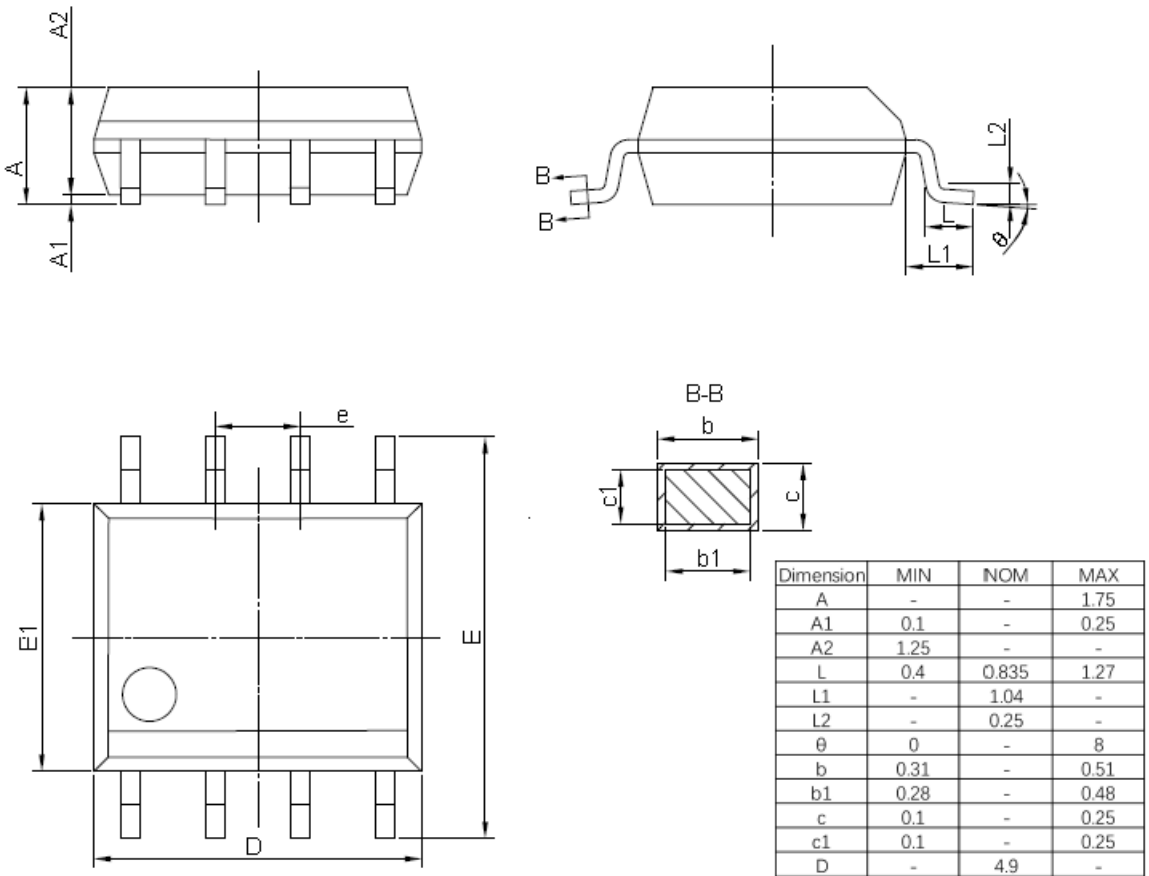


Figure 3. Delay Matching Waveform

PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
L2	-	0.25	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	-	4.9	-
E	-	6	-
E1	-	3.9	-
e	1.27 BSC		
Unit : mm			

Figure 4. SOP8 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2019-8-29	
Whole document	Change company logo
Page 1	Remove “Fig 1.” and update the typical application circuit Remove “November 2015”
Page 3	Update the internal function block
Page 2	Update package configuration
Rev 1.0 datasheet, 2020-6-24	
Page 3	Update the internal function block
Rev 1.2datasheet, 2020-12-20	
Page 3	Update the internal function block
Page 7-9	Update parameters chart
Rev 1.3 datasheet, 2021-10-29	
Whole datasheet	Update the Logo and format
Page 1	Remove PDIP-8 package
Page 2	Remove SLM2106BCA-GT and SLM2106BDA-GT in ordering information
Page 3	Updated the functional block diagram
Page 5	Updated the I_{QCC}, I_{IN+} , V_{CCUV-}, I_{O+} and I_{O-} in the static electrical characteristics
Rev 1.4 datasheet, 2022-8-29	
Whole datasheet	Change package name from SOIC-8 to SOP8 and update the package case outlines.
Rev 1.5 datasheet, 2022-9-20	
Page 5	Change the I_{QCC} max value from 280uA to 305uA in the static electrical characteristics